RCA Solid State

DATABOOK

High-Reliability Integrated Circuits

RCA Compliance to MIL-STD-883, Rev. C

RCA MIL-M-38510 qualified devices comply with MIL-STD-883, Rev. C, Paragraph 1.2.

The following RCA slash series (/...) comply with MIL-STD-883, Rev. C, Paragraph 1.2.1 when optional Group B conformance testing is performed.

Slash MS (.../MS)	CD4XXX Series Class S

The following RCA slash series (/...) comply with MIL-STD-883, Rev. C, Paragraph 1.2.1.

Slash Series	**Description**
Slash 3A (.../3A)	CD4XXX Series, Class B
Slash 3A (.../3A)	CD54HC/HCTXXX Series, Class B

The following RCA slash series (/...) are governed by MIL-STD-883, Rev. C, Paragraph 1.2.2. Specific process and screening performed are delineated in Tables provided in this publication.

Slash Series	**Description**
Slash 3 (.../3)	CD4XXX Series, Modified Class B
Slash 3 (.../3)	CDP18XX Series, Modified Class B
Slash 3 (.../3)	CDMXXXX Series, Modified Class B
Slash 3 (.../3)	GPXXX Series, Modified Class B
Slash 3 (.../3)	CA3XXX Series, Modified Class B
Slash 3W (.../3W)	CA3XXX Series, Modified Class B
Slash 3 (.../3)	CD54HC/HCTXXX Series, Modified Class B
Slash 1 (.../1)	CA3XXX Series, Modified Class S
Slash 1R (.../1R)	CMMXXXX, Modified Class S
Slash 1R (.../1R)	GPXXX Series, Modified Class S

The Cover . . .

About 150 days before arriving at Jupiter, the Galileo probe separates from its companion orbiter and begins its descent toward the planet, in this artist's concept.

The spacecraft will arrive at Jupiter in December 1988, after launch from a space shuttle in May 1986.

The orbiter will study Jupiter, its magnetosphere, and its major satellites during a 20 month's reconnaissance.

The detachable probe will conduct a detailed investigation of the turbulent atmosphere as it descends on a parachute to its ultimate destruction.

Photo courtesy of NASA/JPL

RCA High-Reliability Products

This DATABOOK contains detailed technical information on high-reliability integrated circuits available from RCA. RCA offers an extensive line of high-reliability integrated circuits that are processed and screened in accordance with military, RCA standard, or special custom specifications to meet the needs of modern military, aerospace, and critical industrial and scientific applications. These integrated circuits include several basic product series that encompass a wide range of circuit functions and several different technologies, as follows:

- CD4000-series CMOS digital logic circuits
- 8-Bit CMOS microprocessor family
- CA3000-series linear (bipolar and BiMOS) circuits and MOSFETs
- QMOS 54HC/HCT circuits
- Semicustom gate arrays and standard cells
- CMOS/SOS LSI ICs
- Radiation-hardened versions of selected types listed above

This DATABOOK is intended as a guide to circuit and system engineers in the selection of the optimum IC product for a particular high-reliability application. It points out RCA's capability with respect to both standard-product high-reliability ICs and high-reliability custom ICs. It describes the screening levels to which the types in each product series are supplied and includes product flow charts, detailed screening procedures, and test limits that precisely define each level. In addition, the DATABOOK provides a comprehensive listing of RCA high-reliability integrated circuits and shows photographs and dimensional outlines of the variety of packages in which these integrated circuits are supplied.

RCA also provides a broad line of high-reliability discrete solid-state power devices (power transistors, triacs, and silicon controlled rectifiers). These devices include types qualified as JAN or JANTX devices in accordance with MIL-STD-19500 General Specifications and MIL-STD-750 Test Methods, types that are not yet covered by military specifications but that are processed and screened to specifications patterned after the military standards, and types that are specially designed and processed to withstand high radiation environments. The DATABOOK also describes the preconditioning and screening of RCA high-reliability power devices.

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When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

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Printed in USA/12-85

Products, Packages, and Ordering Information

This section contains an index of RCA high-reliability products categorized by technology. The types are listed in alphanumeric order in each category together with their descriptive titles. Additional information on individual types may be found on the pages specified. Packages and ordering information are also included.

Index to RCA High-Reliability Products

High-Voltage CD4000B-Series CMOS ICs

(See pages 27 through 74 for technical data)

Type No.	Description	No. of Leads
CD4000B	Dual 3-input NOR gate plus inverter	14
CD4000UB	Dual 3-input NOR gate plus inverter	14
CD4001B	Quad 2-input NOR gate	14
CD4001UB	Quad 2-input NOR gate	14
CD4002B	Dual 4-input NOR gate	14
CD4002UB	Dual 4-input NOR gate	14
CD4006B	18-stage static shift register	14
CD4007UB	Dual complementary pair plus inverter	14
CD4008B	4-bit full adder with parallel carry-out	16
CD4009UB	Hex buffer/converter (inverting)	16
CD4010B	Hex buffer/converter (non-inverting)	16
CD4011B	Quad 2-input NAND gate	14
CD4011UB	Quad 2-input NAND gate	14
CD4012B	Dual 4-input NAND gate	14
CD4012UB	Dual 4-input NAND gate	14
CD4013B	Dual "D" flip-flop with set/reset capability	14
CD4014B	8-stage static shift register	16
CD4015B	Dual 4-stage static shift register	16
CD4016B	Quad bilateral switch	14
CD4017B	Decade counter/divider	16
CD4018B	Presettable divide-by "N" counter	16
CD4019B	Quad AND/OR select gate	16
CD4020B	14-stage Binary Ripple Counter	16
CD4021B	8-stage static shift register	16
CD4022B	Divide-by-8 counter/divider	16
CD4023B	Triple 3-input NAND gate	14
CD4023UB	Triple 3-input NAND gate	14
CD4024B	7-stage binary ripple counter	14
CD4025B	Triple 3-input NOR gate	14
CD4025UB	Triple 3-input NOR gate	14
CD4026B	Decade counter/divider	16
CD4027B	Dual "J-K" flip-flop with set/reset capability	16
CD4028B	BCD-to-decimal decoder	16
CD4029B	Presettable up/down counter	16
CD4030B	Quad exclusive-OR gate	14
CD4031B	64-stage static shift register	16
CD4032B	Triple serial adder (positive logic adder)	16
CD4033B	Decade counter/divider	16
CD4034B	8-stage static shift register	24
CD4035B	4-stage parallel-in/parallel-out shift register	16
CD4038B	Triple serial adder (negative logic adder)	16
CD4040B	12-stage binary ripple counter	16
CD4041UB	Quad true/complement buffer	14
CD4042B	Quad clocked "D" latch	16
CD4043B	Quad NOR R/S latch (3-state outputs)	16
CD4044B	Quad NAND R/S latch (3-state outputs)	16
CD4045B	21-stage timer	14
CD4046B	Micropower phase-locked loop	16
CD4047B	Monostable/astable multivibrator	14
CD4048B	Multifunctional expandable 8-input gate (3-state output)	16
CD4049UB	Hex buffer/converter (inverting)	16
CD4050B	Hex buffer/converter (non-inverting)	16
CD4051B	8-channel analog multiplexer/ demultiplexer	16
CD4052B	4-channel analog multiplexer/ demultiplexer	16
CD4053B	Triple 2-channel analog multiplexer/ demultiplexer	16
CD4054B	4-Segment display driver	16
CD4055B	BCD-to-7-segment decoder/driver with "display frequency" output	16
CD4056B	BCD-to-7-segment decoder driver with strobed-latch function	16
CD4060B	14-stage binary ripple counter/ divider and oscillator	16
CD4063B	4-bit magnitude comparator	16
CD4066B	Quad bilateral switch	14
CD4067B	16-channel analog multiplexers/ demultiplexers	24
CD4068B	8-input NAND/AND gate	14
CD4069UB	Hex inverter	14
CD4070B	Quad exclusive-OR gate	14
CD4071B	Quad 2-input OR gate	14
CD4072B	Dual 4-input OR gate	14
CD4073B	Triple 3-input AND gate	14
CD4075B	Triple 3-input OR gate	14
CD4076B	4-bit "D" flip-flop (3-state outputs)	16
CD4077B	Quad exclusive-NOR gate	14
CD4078B	8-bit NOR/OR gate	14
CD4081B	Quad 2-input AND gate	14
CD4082B	Dual 4-input AND gate	14
CD4085B	Dual 2-wide, 2-input AND/OR/ INVERT (AOI) gate	14
CD4086B	Expandable 4-wide, 2-input AND/OR/INVERT (AOI) gate	14
CD4089B	Binary rate multiplier	16
CD4093B	Quad 2-input NAND Schmitt Trigger	14
CD4094B	8-stage shift-and-store bus register	16
CD4095B	Gated "J-K" flip-flop (non-inverting)	14
CD4096B	Gated "J-K" flip-flop (inverting) and non-inverting)	14
CD4097B	8-channel analog multiplexer/ demultiplexer	24
CD4098B	Dual monostable multivibrator	16
CD4099B	8-bit addressable latch	16
CD4502B	Strobed hex inverter/buffer	16
CD4503B	Hex buffer (non-inverting)	16
CD4508B	Dual 4-bit latch	24
CD4510B	Presettable 4-bit BCD up/down counter	16
CD4511B	BCD-to-7-segment latch decoder/ driver	16
CD4512B	8-channel data selector (3-state output)	16
CD4514B	4-bit latch/4-to-16-line decoder (outputs low)	24
CD4515B	4-bit latch/4-to-16-line decoder (outputs low)	24
CD4516B	Presettable 4-bit binary up/down counter	16
CD4517B	Dual 64-bit shift register	16
CD4518B	Dual BCD up counter	16
CD4520B	Dual binary up counter	16
CD4527B	BCD rate multiplier	16
CD4532B	8-input priority encoder	16
CD4536B	Programmable timer	16
CD4538B	Dual precision monostable multivibrator	16
CD4541B	CMOS programmable timer	14
CD4543B	CMOS BCD-to-seven-segment latch/ decoder/driver for liquid-crystal displays	16
CD4555B	Dual 1-of-4 decoder/demultiplexer (outputs high)	16

Index to RCA High-Reliability Products

High-Voltage CD4000B-Series CMOS ICs (Cont'd.)

(See pages 27 through 74 for technical data)

Type No.	Description	No. of Leads
CD4556B	Dual 1-of-4 decoder/demultiplexer (outputs low)	16
CD4585B	4-bit magnitude comparator	16
CD4724B	8-bit addressable latch	16
CD40100B	32-bit left/right shift register	16
CD40101B	9-bit parity generator/checker	14
CD40102B	Presettable 2-decade BCD down counter	16
CD40103B	Presettable 8-bit binary down counter	16
CD40104B	4-bit bidirectional universal shift register	16
CD40105B	4-bit x 16 word FiFo buffer register	16
CD40106B	Hex Schmitt Trigger	14
CD40107B	Dual 2-input NAND buffer/driver	14
CD40108B	4 x 4 multiport register	24
CD40109B	Quad low-to-high voltage interface	16
CD40110B	Decade up-down counter/decoder/latch/display driver	16
CD40116B	CMOS high-speed 8-bit bidirectional CMOS/TTL interface level converter	22
CD40147B	10-line to 4-line BCD priority encoder	16
CD40160B	Decade counter with asynchronous clear	16
CD40161B	Binary counter with asynchronous clear	16
CD40162B	Decade counter with synchronous clear	16
CD40163B	Binary counter with synchronous clear	16
CD40174B	Hex "D" flip-flop	16
CD40175B	CMOS Quad 'D'-type flip-flop	16
CD40181B	4-bit arithmetic logic unit	24
CF40182B	Look-ahead-carry block	16
CD40192B	Presettable 4-bit BCD up/down counter	16
CD40193B	Presettable 4-bit binary up/down counter	16
CD40194B	4-bit bidirectional universal shift register	16
CD40208B	4 x 4 multiport register	24
CD40257B	Quad 2-line-to-1-line data selector	16

NOTES:

RCA also offers high-reliability versions of a number of the A-series (3 to 12V) counterparts (CD4000A through CD4050A and CD4066A) of the high-voltage B-series types listed above and of several A-series types for which there are no corresponding B-series types (i.e., CD4036A and CD4039A RAM's, and CD4059A programmable divide-by-N counter).

Contact your RCA authorized distributor or sales office for specific availability.

The above lead counts are for flat packages and dual-in-line packages only.

CD54HC, CD54HCT, and CD54HCU QMOS ICs

(See pages 75 through 114 for technical data)

Type No.		Description	No. of Leads
CMOS Logic	TTL Logic		
CD54HC00	CD54HCT00	Quad 2-Input NAND Gate	14
CD54HC02	CD54HCT02	Quad 2-Input NOR Gate	14
CD54HC03	CD54HCT03	Quad 2-Input NAND Gate with Open Collector	14
CD54HC04	CD54HCT04	Hex Inverter	14
CD54HC08	CD54HCT08	Quad 2-Input AND Gate	14
CD54HC10	CD54HCT10	Triple 3-Input NAND Gate	14
CD54HC11	CD54HCT11	Triple 3-Input AND Gate	14
CD54HC14	CD54HCT14	Hex Inverting Schmitt Trigger	14
CD54HC20	CD54HCT20	Dual 4-Input NAND Gate	14
CD54HC21	CD54HCT21	Dual 4-Input AND Gate	14
CD54HC27	CD54HCT27	Triple 3-Input NOR Gate	14
CD54HC30	CD54HCT30	8-Input NAND Gate	14
CD54HC32	CD54HCT32	Quad 2-Input OR Gate	14
CD54HC42	CD54HCT42	BCD-to-Decimal Decoder (1-to-10)	16
CD54HC73	CD54HCT73	Dual J-K Flip-Flop w/RESET	14
CD54HC74	CD54HCT74	Dual D Flip-Flop w/SET and RESET	14
CD54HC75	CD54HCT75	Quad Bistable Transparent Latch	16
CD54HC85	CD54HCT85	4-Bit Magnitude Comparator	16
CD54HC86	CD54HCT86	Quad 2-Input EXCLUSIVE-OR Gate	14
CD54HC93	CD54HCT93	4-Bit Binary Ripple Counter	14

Contact your authorized RCA distributor or sales office for current availability.
The above lead counts are for dual-in-line packages only.

Index to RCA High-Reliability Products

CD54HC, CD54HCT, and CD54HCU QMOS ICs (Cont'd.)

(See pages 75 through 114 for technical data)

Type No.		Description	No. of Leads
CMOS Logic	TTL Logic		
CD54HC107	CD54HCT107	Dual J-K Flip-Flop w/RESET	14
CD54HC109	CD54HCT109	Dual J-K Flip-Flop w/SET and RESET	16
CD54HC112	CD54HCT112	Dual J-K Flip-Flop w/SET and RESET	16
CD54HC123	CD54HCT123	Dual Retriggerable Monostable Multivibrator w/RESET	16
CD54HC125	CD54HCT125	Quad 3-State Buffer	14
CD54HC126	CD54HCT126	Quad 3-State Buffer	14
CD54HC132	CD54HCT132	Quad 2-input NAND Schmitt Trigger	14
CD54HC137	CD54HCT137	3-to-8-Line Decoder w/Latch, Inverting	16
CD54HC138	CD54HCT138	3-to-8-Line Decoder/Demultiplexer, Inverting	16
CD54HC139	CD54HCT139	Dual 2-of-4-Line Decoder/Demultiplexer	16
CD54HC147	CD54HCT147	10-to-4-Line Priority Encoder	16
CD54HC151	CD54HCT151	8-Input Multiplexer	16
CD54HC153	CD54HCT153	Dual 4-Input Multiplexer	16
CD54HC154	CD54HCT154	4-to-16-Line Decoder/Demultiplexer	24
CD54HC157	CD54HCT157	Quad 2-Input Multiplexer	16
CD54HC158	CD54HCT158	Quad 2-Input Multiplexer, Inverting	16
CD54HC160	CD54HCT160	Synchronous BCD Decade Counter, Asynchronous Reset	16
CD54HC161	CD54HCT161	Synchronous 4-Bit Binary Counter, Asynchronous Reset	16
CD54HC162	CD54HCT162	Synchronous BCD Decade Counter, Synchronous Reset	16
CD54HC163	CD54HCT163	Synchronous 4-Bit Binary Counter, Synchronous Reset	16
CD54HC164	CD54HCT164	8-Bit Serial-In Parallel-Out Shift Register	14
CD54HC165	CD54HCT165	8-Bit Parallel-In Serial-Out Shift Register	16
CD54HC166	CD54HCT166	8-Bit Parallel-In Serial-Out Shift Register	16
CD54HC173	CD54HCT173	Quad D-Type Flip-Flop, 3-State	16
CD54HC174	CD54HCT174	Hex D-Type Flip-Flop w/RESET	16
CD54HC175	CD54HCT175	Quad D-Type Flip-Flop w/RESET	16
CD54HC181	CD54HCT181	ALU	24
CD54HC182	CD54HCT182	Carry Generator	16
CD54HC190	CD54HCT190	Presettable Synchronous BCD Decade Up/Down Counter	16
CD54HC191	CD54HCT191	Synchronous 4-Bit Binary Up/Down Counter	16
CD54HC192	CD54HCT192	Synchronous BCD Decade Up/Down Counter	16
CD54HC193	CD54HCT193	Synchronous 4-Bit Binary Up/Down Counter	16
CD54HC194	CD54HCT194	4-Bit Bidirectional Universal Shift Register	16
CD54HC195	CD54HCT195	4-Bit Parallel Access Shift Register	16
CD54HC221	CD54HCT221	Dual Monostable Multivibrator w/RESET	16
CD54HC237	CD54HCT237	3-to-8-Line Decoder	16
CD54HC238	CD54HCT238	3-to-8-Line Decoder/Demultiplexer	16
CD54HC240	CD54HCT240	Octal Buffer/Line Driver, 3-State, Inverting	20
CD54HC241	CD54HCT241	Octal Buffer/Line Driver, 3-State	20
CD54HC242	CD54HCT242	Quad Bus Transceiver, 3-State, Inverting	14
CD54HC243	CD54HCT243	Quad Bus Transceiver, 3-State	14
CD54HC244	CD54HCT244	Octal Buffer/Line Driver, 3-State	20
CD54HC245	CD54HCT245	Octal Bus Transceiver, 3-State	20
CD54HC251	CD54HCT251	8-Input Multiplexer, 3-State	16
CD54HC253	CD54HCT253	Dual 4-Input Multiplexer, 3-State	16
CD54HC257	CD54HCT257	Quad 2-Input Multiplexer, 3-State	16
CD54HC258	CD54HCT258	Quad 2-Line-to-4-Line Data Selector	16
CD54HC259	CD54HCT259	8-Bit Addressable Latch	16
CD54HC273	CD54HCT273	Octal D-Type Flip-Flop w/RESET	20
CD54HC280	CD54HCT280	9-Bit Odd/Even Parity Generator/Checker	14
CD54HC283	CD54HCT283	4-Bit Full Adder w/Fast Carry	16
CD54HC297	CD54HCT297	Digital Phase-Locked-Loop Filter	16
CD54HC299	CD54HCT299	8-Bit Universal Shift Register, 3-State	20
CD54HC354	CD54HCT354	8-Input Multiplexer/Register, 3-State	20
CD54HC356	CD54HCT356	8-Input Multiplexer/Register, 3-State	20

Contact your authorized RCA distributor or sales office for current availability.
The above lead counts are for dual-in-line packages only.

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CD54HC, CD54HCT, and CD54HCU QMOS ICs

(See pages 75 through 114 for technical data)

Type No.		Description	No. of Leads
CMOS Logic	TTL Logic		
CD54HC365	CD54HCT365	Hex Buffer/Line Driver, 3-State	16
CD54HC366	CD54HCT366	Hex Buffer/Line Driver, 3-State, Inverting	16
CD54HC367	CD54HCT367	Hex Buffer/Line Driver, 3-State	16
CD54HC368	CD54HCT368	Hex Buffer/Line Driver, 3-State, Inverting	16
CD54HC373	CD54HCT373	Octal Transparent Latch, 3-State	20
CD54HC374	CD54HCT374	Octal D-Type Flip-Flop, 3-State	20
CD54HC377	CD54HCT377	Octal D-Type Flip-Flop with Data Enable	20
CD54HC390	CD54HCT390	Dual Decade Ripple Counter	16
CD54HC393	CD54HCT393	Dual 4-Bit Binary Ripple Counter	14
CD54HC423	CD54HCT423	Dual Retriggerable Monostable Multivibrator with Reset	16
CD54HC533	CD54HCT533	Octal Transparent Latch, 3-State, Inverting	20
CD54HC534	CD54HCT534	Octal D-Type Flip-Flop, 3-State, Inverting	20
CD54HC540	CD54HCT540	Octal Buffer/Line Driver, 3-State, Inverting	20
CD54HC541	CD54HCT541	Octal Buffer/Line Driver, 3-State	20
CD54HC563	CD54HCT563	Octal Transparent Latch, 3-State, Inverting	20
CD54HC564	CD54HCT564	Octal D-Type Flip-Flop, 3-State, Inverting	20
CD54HC573	CD54HCT573	Octal Transparent Latch, 3-State	20
CD54HC574	CD54HCT574	Octal D-Type Flip-Flop, 3-State	20
CD54HC583	CD54HCT583	4-Bit Full Adder w/Fast Carry	16
CD54HC597	CD54HCT597	8-Bit Shift Register with I/P Latch	16
CD54HC640	CD54HCT640	Octal Bus Transceiver, 3-State, Inverting	20
CD54HC643	CD54HCT643	Octal Bus Transceiver, 3-State, True/Inverting	20
CD54HC646	CD54HCT646	Octal Bus Transceiver/Register, 3-State	24
CD54HC648	CD54HCT648	Octal Bus Transceiver/Register, 3-State, Inverting	24
CD54HC670	CD54HCT670	4 x 4 Register File, 3-State	16
CD54HC688	CD54HCT688	8-Bit Magnitude Comparator	20
CD54HC4002	CD54HCT4002	Dual 4-Input NOR Gate	14
CD54HC4015	CD54HCT4015	Dual 4-Bit Serial-In/Parallel-Out Shift Register	16
CD54HC4016	CD54HCT4016	Quad Bilateral Switch	14
CD54HC4017	CD54HCT4017	Johnson Decade Counter w/10 Decoded Outputs	16
CD54HC4020	CD54HCT4020	14-Stage Binary Ripple Counter	16
CD54HC4024	CD54HCT4024	7-Stage Binary Ripple Counter	14
CD54HC4040	CD54HCT4040	12-Bit Binary Ripple Counter	16
CD54HC4046	CD54HCT4046	Phase-Locked Loop with VCO	16
CD54HC4049	—	Hex Inverting HIGH-to-LOW Level Shifter	16
CD54HC4050	—	Hex HIGH-to-LOW Level Shifter	16
CD54HC4051	CD54HCT4051	8-Channel Analog Multiplexer/Demultiplexer	16
CD54HC4052	CD54HCT4052	Dual 4-Channel Analog Multiplexer/Demultiplexer	16
CD54HC4053	CD54HCT4053	Triple 2-Channel Analog Multiplexer/Demultiplexer	16
CD54HC4059	CD54HCT4059	Programmable Divided-by-"N" Counter	24
CD54HC4060	CD54HCT4060	14-Stage Binary Ripple Counter w/Oscillator	16
CD54HC4066	CD54HCT4066	Quad Bilateral Switch	14
CD54HC4067	CD54HCT4067	16-Channel Analog Multiplexer/Demultiplexer	24
CD54HC4075	CD54HCT4075	Triple 3-Input OR Gate	14
CD54HC4094	CD54HCT4094	8-Stage Shift-and-Store Bus Register	16
CD54HC4316	CD54HCT4316	Quad Analog Switch	16
CD54HC4351	CD54HCT4351	Analog Multiplexer w/Latch	20
CD54HC4352	CD54HCT4352	Analog Multiplexer w/Latch	20
CD54HC4353	CD54HCT4353	Analog Multiplexer w/Latch	20
CD54HC4510	CD54HCT4510	Up/Down Counter, BCD	16
CD54HC4511	CD54HCT4511	BCD-to-7-Segment Latch/Decoder/Driver	16
CD54HC4514	CD54HCT4514	4-to-16-Line Decoder/Demultiplexer w/Input Latches	24
CD54HC4515	CD54HCT4515	4-to-16-Line Decoder with Input Latches	24
CD54HC4516	CD54HCT4516	Up/Down Counter, Binary	16
CD54HC4518	CD54HCT4518	Dual Synchronous BCD Counter	16
CD54HC4520	CD54HCT4520	Dual 4-Bit Synchronous Binary Counter	16
CD54HC4538	CD54HCT4538	Dual Precision Monostable Multivibrator	16
CD54HC4543	CD54HCT4543	BCD-to-7-Segment Latch/Decoder/Driver for LCDs	16
CD54HC7046	CD54HCT7046	Phase-Locked Loop with In-Lock Detection	16
CD54HC7266	CD54HCT7266	Quad Exclusive NOR	16
CD54HC40102	CD54HCT40102	8-Bit Synchronous BCD Down Counter	16
CD54HC40103	CD54HCT40103	8-Bit Binary Down Counter	16
CD54HC40104	CD54HCT40104	4-Bit Bidirectional Universal Shift Register, 3-State	16
CD54HC40105	CD54HCT40105	4 Bits x 16 Words FIFO Register	16
CD54HCU04	—	Hex Inverter (Unbuffered)	14

Contact your authorized RCA distributor or sales office for current availability.
The above lead counts are for dual-in-line packages only.

Index to RCA High-Reliability Products

CA3000-Series Linear ICs and MOSFETs

(See pages 115 through 224 for technical data)

Type No.	Description	No. of Leads
CA723	Voltage Regulator	10
CA741	Operational Amplifier	8
CA747	Dual Operational Amplifier	10
CA748	Operational Amplifier	8
CA1558	Dual Operational Amplifier	8
CA3000	Differential Amplifier	10
CA3001	Differential Amplifier	12
CA3002	Differential Amplifier	10
CA3006	Differential Amplifier (RF)	12
CA3015	Operational Amplifier	12
CA3015A	Operational Amplifier	12
CA3018	Transistor Array	12
CA3018A	Transistor Array	12
CA3019	Diode Array	10
CA3020	Wide-Band Power Amplifier	12
CA3020A	Wide-Band Power Amplifier	12
CA3026	Dual Differential Amplifier Array	12
CA3028B	Differential Amplifier (RF)	8
CA3038A	Operational Amplifier	14
CA3039	Diode Array	12
CA3040	Video and Wide-band Amplifier	12
CA3045	Transistor Array	14
CA3049	Dual Differential Amplifier Array	12
CA3058	Zero-Voltage Switch	14
CA3078	Micropower Operational Amplifier	8
CA3078A	Micropower Operational Amplifier	8
CA3080	Variable Operational Amplifier	8
CA3080A	High Slew Rate OTA	8
CA3081	Transistor Array	16
CA3082	Transistor Array	16
CA3083	Transistor Array	16
CA3085	Voltage Regulator	8
CA3085A	Voltage Regulator	8
CA3085B	Voltage Regulator	8
CA3089	FM IF System	16
CA3094	Programmable Power Switch/ Amplifier	8
CA3094A	Programmable Power Switch/ Amplifier	8
CA3100	BiMOS Operational Amplifier	8
CA3118A	Transistor Array	12
CA3130	BiMOS Operational Amplifier	8
CA3130A	BiMOS Operational Amplifier	8
CA3140	BiMOS Operational Amplifier	8
CA3140A	BiMOS Operational Amplifier	8
CA3146A	Transistor Array	14
CA3160	BiMOS Operational Amplifier	8
CA3160A	BiMOS Operational Amplifier	8
CA3193*	BiMOS Precision Operational Amplifier	8
CA3193A*	BiMOS Precision Operational Amplifier	8
CA3260*	BiMOS Operational Amplifier	8
CA3260A*	BiMOS Operational Amplifier	8
CA3290A	BiMOS Dual Voltage Comparator	8
CA3300	6-Bit Flash A/D Converter	18
CA3306*	6-Bit Precision A/D Converter	18
CA6741	Operational Amplifier	8
MOSFETs		
HR3N187	Dual-Gate MOS Field-Effect Transistor	4
HR3N200	Dual-Gate MOS Field-Effect Transistor	4

*Types to be introduced as high-reliability devices in 1985.

8-Bit CMOS Microprocessor Family

(See pages 225 through 328 for technical data)

Type No.	Description	No. of Leads
CDM5114†	1024-Word x 4-Bit Static RAM	18
CDM6116A	2048-Word x 8-Bit Static RAM	24
CDM6264	8192-Word x 8-Bit Static RAM	28
CDP1802A	CMOS 8-Bit Microprocessor	40
CDP1821†	1024-Word x 1-Bit Static RAM	16
CDP1822†	256-Word x 1-Bit Static RAM	22
CDP1823†	128-Word x 8-Bit Static RAM	24
CDP1824	32-Word x 8-Bit Static RAM	18
CDP1831	512-Word x 8-Bit Static ROM	24
CDP1832	512-Word x 8-Bit Static ROM	24
CDP1833	1024-Word x 8-Bit Static ROM	24
CDP1834	1024-Word x 8-Bit Static ROM	24
CDP1837C	4096-Word x 8-Bit Static ROM[1]	24
CDP1852	8-Bit Input/Output Port	24
CDP1853	N-Bit 1 of 8 Decoder	16
CDP1854A	UART	40
CDP1856	4-Bit Bus Buffer/Separator	16
CDP1857	4-Bit Bus Buffer/Separator	16
CDP1858	4-Bit Latch and Memory Interface	16
CDP1859	4-Bit Latch and Decoder Memory Interface	16

†CMOS/SOS Technology — Transient-Radiation Resistant

The above lead counts are for dual-in-line packages.

Index to RCA High-Reliability Products

Radiation-Hardened ICs for Aerospace

(See pages 329 through 392 for technical data)

Type No.	Description
RAMs	
CMM5114	1024-Word x 4-Bit Static RAM
CMM5104	4096-Word x 1-Bit Static RAM
CMM6167*	16384-Word x 1-Bit Static RAM
EPIC Chip Set	
GP001	8-Bit General Processor Unit (GPU)
GP301	512-Word x 8-Bit ROM
GP302	256-Word x 16-Bit ROM
GP305	512-Word x 16-Bit ROM with pipeline register
GP501	Emulating Controller
GP502	Microprogram Sequencer '2910'
GP503	8-Bit x 8-Bit Multiplier
GP511	Voltage-Level Converter and Buffer
Planned Additions to the EPIC Chip Set	
GP514	Double Address Select Unit
GP515	Double Register Select Unit
GP516	Bus Interface Unit
GP517	Interrupt Control and Timing Unit

*Preliminary data information is not included in this DATABOOK.

Semicustom Gate Arrays and Standard Cells

(See pages 393 through 400 for technical data)

Type	Description
PA40000 Series	CMOS Automated Gate Arrays
PA60000-Series	CMOS/SOS Automated Gate Arrays
PaCMOS I Family	Standard Cells
PaCMOS II/IID Family	Standard Cells

High-Reliability Power Devices

(See pages 401 through 410 for information on RCA high-reliability power devices)

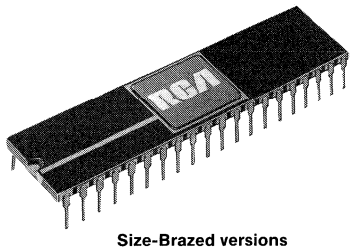
Packages, Chips, and Ordering Information

IC Packages

RCA high-reliability integrated circuits are supplied in hermetically sealed packages that are specially engineered and developed to meet the requirements of military, aerospace, and critical industrial applications. Most CMOS devices are supplied in either dual-in-line ceramic packages (D and F suffixes), ceramic flat packs (K suffix), or leadless-chip-carrier ceramic packages (J suffix). CD4000-series and CDP1800-series parts will be available in the leadless-chip-carrier packages, in either 20-, 28-, or 44-contact versions.

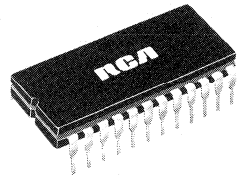
Many RCA high-reliability linear integrated circuits are supplied in TO-5-style hermetic packages (T, S, and V1 suffixes). RCA high-reliability small-signal MOS field-effect transistors (MOSFET's) are all supplied in JEDEC TO-72 hermetic packages.

D SUFFIX — DUAL-IN-LINE CERAMIC PACKAGES



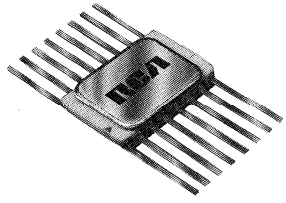
Size-Brazed versions
14-, 16-, 18-, 22-, 24-, 28-, and 40-lead

F SUFFIX — DUAL-IN-LINE CERAMIC PACKAGES



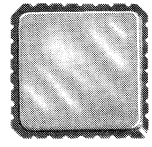
CERDIP
14-, 16-, 18-, 20-, 22-, 24-, 28-, and 40-Lead Versions

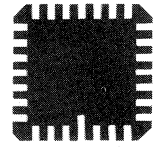
K SUFFIX — CERAMIC FLAT PACK



14-, 16-, 24-, 28-, and 42-Lead Versions

J SUFFIX — LEADLESS-CHIP-CARRIER CERAMIC PACKAGE





20-, 28-, and 44-terminal (0.050-inch centers)
24-, 32-, 48-, and 64-terminal (0.040-inch centers)

TO-5 STYLE PACKAGES

S SUFFIX — WITH FORMED LEADS (DIL-CAN)

JFDEC TO-72 PACKAGE

T SUFFIX — WITH STRAIGHT LEADS

8-, 10-, and
12-Lead Versions

VI SUFFIX — WITH RADIAL FORMED LEADS

10-Lead Version Only

MOSFETs only

Packages, Chips, and Ordering Information

Package Lead Finishes

The different RCA high-reliability IC packages employ a variety of lead finishes, as follows:

Package	Lead Finish	MIL-M-38510 Lead Finish
D	Solder-dipped nickel plate	A
F	Reflowed tin plate	B
K	Solder-dipped nickel plate	A
S	Solder-dipped nickel plate	A
T	Solder-dipped nickel plate	A
V	Solder-dipped nickel plate	A
TO-72	Solder-dipped nickel plate	A
J	Gold-plated contacts	C

Custom Packages

RCA also offers other packages for use in custom orders.

RCA High-Reliability ICs in Leadless-Chip-Carrier Packages

The RCA CD4000B series of CMOS digital logic integrated circuits and CDP1800 series of CMOS-LSI microprocessor, memory, and peripheral integrated circuits are offered in the leadless-chip-carrier packages. Leadless-chip-carrier packaged IC's can be supplied as high-reliability (slash-series) products that are processed and screened to military Classes S and B.

The RCA CMM5104/CMM5114 and the EPIC Chip Set are also offered in the leadless chip-carrier packages. They can be supplied as high-reliability (slash-series) products that conform to JEDEC product outlines.

Leadless-chip-carrier packaging offers the equipment designer and manufacturer a number of advantages over conventional leaded dual-in-line or flat-pack packages. These advantages can be summarized as follows:

- Smaller package outline
- Reduced PC board complexity by eliminating need for mounting holes
- Enhanced PC board density: often results in fewer total boards
- Lower cost for high-pin-count LSI circuits
- Often simplified device-to-board soldering

For hybrid manufacturers, the use of leadless-chip-carrier packaging instead of multichip hybrids will result in improved yields and enhanced reliability because individual devices can be screened to MIL specifications prior to board assembly.

Package Information

- 0.050-inch terminal centers
  0.040-inch terminal centers (EPIC Family)
- Conformity to MIL-M-38510 outlines
  Conformity to JEDEC Product Outlines (EPIC Family)
- Leadless-chip carriers use standard terminal conversions from leaded pin outs
- Square 3-layer ceramic packages
  — 20-, 28-, and 44-terminal
  — 24-, 32-, 48-, and 64-terminal (EPIC Family)
- Hermitically sealed
- Solderable terminals

Branding

Top branding of RCA high-reliability IC's in "D", "F", "K", or "J" packages consists of two or three lines that provide the following information:

1. Manufacturer's logo
2. Part number (e.g. CD4001BF/3)
3. Four-digit date code

The number of brand characters per line is limited.

Chips

RCA also offers a broad line of logic (CD4000B, CD54HC/HCT) high-reliability integrated-circuit chips (H/M suffix) for use in hybrid circuits. These chips are normally to MIL-STD-883, Method 2010, Condition B Visual. Chips subjected to the more critical Condition A Visual and to SEM (scanning-electron-microscope) inspections (H/S suffix) are also available. Radiation-hardened to 10^5 (R) and 10^6 (H) rad (Si) are also available.

Ordering Information

When ordering RCA high-reliability integrated circuits, it is important that the appropriate package suffix letter be affixed to the type number. The photographs on the next page show the suffix-letter codes for the various package options. The screening level desired for the integrated circuits must also be specified. Refer to the appropriate section of this Product Guide for information on the available screening levels for each product series.

Packaging in Readiness for Shipment

Package Style	Type of Packaging
Dual-in-Line Ceramic (Both D- and F-Suffix Types)	Anti-static plastic magazine (25 devices per magazine) in static shielding sleeve or box.
Leadless Ceramic Chip Carrier (J-Suffix)	Conductive tray with individual compartments
Ceramic Flat Pack	Conductive paper-board carrier (1 or 10 devices per carrier) in static shielding boxes.
TO-5 (S-, T- and V1-Suffix Types)	Partition cell (100 devices per box) in static shielding box with anti-static foam.
TO-72	Partition cell (400 devices per box) in static shielding box with anti-static foam.

Packages, Chips, and Ordering Information

Power Device Packages

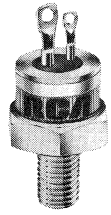
RCA high-reliability power devices are supplied in a variety of hermetically sealed packages.

JEDEC TO-204AA

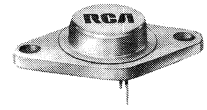
(0.060-In. Dia. Pins)
JEDEC TO-204AE/

Low-Profile
JEDEC TO-205AF

TO-39



TO-48



TO-66

RADIAL

Reliability Classes and Testing

RCA High-Reliability IC Capability

RCA Solid State is a leading supplier of high-reliability integrated circuits to the military and aerospace community. Years of commitment, dedication, experience, and know-how make possible shipment of hundreds of thousands of quality high-reliability microcircuits annually.

RCA specialists fully understand the needs of component and systems engineers in the design of high-reliability equipment, are thoroughly familiar with the objective and requirements of MIL-STD-883 and MIL-M-38510, and work closely with governmental agencies in the establishment of detailed specifications for high-reliability microcircuits. Moreover, RCA provides complete facilities for processing and testing integrated circuits to these specifications. RCA is justly proud of its many significant accomplishments with respect to the development, production, and shipment of high-reliability integrated circuits, including:

- First supplier of MIL-M-38510 to attain QPL Class S Part One Radiation-Hardness Listing
- First supplier of MIL-M-38510 CMOS integrated circuits
- Leader in the production of radiation-resistant CMOS microcircuits [to JAN $1x10^5$ rad (Si) and $1 x 10^6$ rad (Si)]
- Initiator of scanning-electron-microscope (SEM) inspections in the production of high-reliability microcircuits — in use at RCA since 1972
- Initiator of MIL-STD-883, Condition A inspections — in use at RCA since 1972

Reliability Classes

The term *high reliability* as applied to integrated circuits covers a broad spectrum of reliability classes. These classes were originally defined by device manufacturers based on test methods described in MIL-STD-883, a compendium of quality and conformance tests, and later were standardized by the government. MIL-STD-883 establishes uniform methods and procedures for testing microcircuits including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military and space operations and physical and electrical tests.

Today, there are both in-house and government-defined reliability classes. The contents of the in-house programs vary with the manufacturer. The government program, referred to as JAN M38510, consists of a General Specification and a Device (detailed) Specification. The General Specification, MIL-M-38510, establishes the general requirements for microcircuits and the quality and reliability assurance requirements that must be met in the procurement of JAN microcircuits. The Device (detailed) Specification establishes the detailed test requirements and inspections and any specific characteristics unique to the particular device. The General Specification applies to all technologies, such as TTL, ECL, Linear, and CMOS; the Device (detailed) Specification delineates the requirements for a circuit function within a device technology.

Military JAN and DESC Product

RCA is committed to provide JAN product as a first option to a customer, where available. The CD4000B series is offered in a number of JAN Class S and Class B MIL-M-38510 slash-sheet types, see section 3 for types. RCA also offers CD54HC-series parts to DESC specifications. These types are identical to the CD54HC/HCT-series /3A product described in section 5 of this DATABOOK. RCA is in the process of qualifying CD54HC types to the MIL-M-38510/650 series and these types should be available in 1986 and 1987.

Standard-Product High-Reliability ICs

RCA offers high-reliability versions of virtually its entire line of standard-product integrated circuits from the CD4000 series of CMOS digital logic types, the CD54HC and CD54HCT high-speed CMOS types, the CDP1800 series of microprocessor and associated memory and input/output (I/O) types, and the CA3000 series of bipolar linear types. These integrated circuits are processed and screened to Class B requirements.

RCA also offers high-reliability versions of standard-product types that are processed and screened to special customized specifications, especially for the aerospace user and others who procure types to Class S specifications.

RCA maintains an extensive computer file of customer specifications and has the methodology required to translate these customized specifications into internal RCA standards and factory operating procedures. In addition to the detailed device specifications, the computer file lists the customer specification number, any revision number, and the RCA custom number assigned to a specific device type.

High-Reliability Custom and Semicustom ICs

RCA has complete custom- and semi custom-circuit capabilities for various CMOS and bipolar integrated-circuit technologies. Custom circuits are offered whenever this approach to integrated-circuit design is determined to be economically feasible. RCA high-reliability custom integrated circuits can be processed and screened to Class S or Class B specifications. These custom circuits, which are described in detail in later sections of this booklet include:

- EPIC 8-bit slice microcomputer family and associated memory (RAM) complement
- Semicustom products —
  Automated gate arrays
  Automated standard cells (PaCMOS®)
  Aegis antenna phase array
  Bipolar SPARROW ICs
  COMSEC digital CMOS arrays
  FUSE digital CMOS timing ICs

Radiation-Hardened High-Reliability ICs

RCA also offers radiation-hardened versions of high-reliability (Class S and Class MS) CD4000-series CMOS integrated circuits. Radiation-hardened types, which are identified by addition of an "R" or "H" suffix to the device type number, are electrically and mechanically identical to their prototype with the exception that they are processed and screened to withstand a total gamma-radiation dosage of 10^5 rads(Si) for R-suffix types or 10^6 rads(Si) for H-suffix types. RCA also offers CD4000B-series types (H suffix) that are resistant to neutron irradiation and exhibit improved latch-up protection.

RCA also offers a broad line of radiation-hardened integrated circuits that utilize CMOS/SOS technology and provide exceptional tolerance for withstanding transient radiation, total-dose radiation, and single-event-upset (SEU). The device complement includes the EPIC 8-bit-slice microcomputer chip-set family, which contains an 8-bit slice, RAMs, ROMs, controllers, and semicustom gate arrays for customizing computer architecture or emulating existing software. Rad-hard RAMs are available for stand-alone memory systems. These devices are screened to Class S-type specifications.

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Quality Conformance Testing

The following tables list and describe the conformance testing performed by RCA on JAN and compliant product manufactured to the requirements of MIL-STD-883, Rev. 3, Paragraph 1.2.1. Conformance testing is performed to the sampling requirements of Group A, B, C, and D tests as described. Specific group testing is performed according to whether the product is manufactured to Class S or B or screening level /MS, /1, /3, /3A, or /3W requirements.

Group A Electrical Tests for JAN Classes S and B and Levels /MS, /1, /3, and /3A[1]

Subgroup[2]	LTPD	Subgroup[2]	LTPD
Subgroup 1 Static tests at 25°C	2	**Subgroup 8** Functional tests at maximum and minimum operating temperatures	5
Subgroup 2 Static tests at maximum rated operating temperature	3	**Subgroup 9** Switching tests at 25°C	2
Subgroup 3 Static tests at minimum rated operating temperature	5	**Subgroup 10** Switching tests at maximum rated operating temperature[4]	3
Subgroup 4 Dynamic tests at 25°C[3]	2		
Subgroup 7 Functional tests at 25°C	2	**Subgroup 11** Switching tests at minimum rated operating temperature[4]	5

Notes:
1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable specification.
2. Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.
3. Performed at Qualification only.
4. Performed for JAN Class S only.

Group B Tests for Class S and Level /MS and /1 Devices

Test	MIL-STD-883 Method	MIL-STD-883 Condition	Quantity/(accept no.) or LTPD
Subgroup 1			
(a) Physical dimensions	2016		2(0)
(b) Internal water-vapor content	1018	5,000 ppm maximum water content at 100°C	3(0) or 5(1)
Subgroup 2[2]			
(a) Resistance to solvents	2015		4(0)
(b) Internal visual and mechanical	2013 & 2014	Failure criteria from design and construction requirements of applicable procurement document	2(0)
(c) Bond strength	2011		LTPD[4] = 10
(1) Thermo compression		(1) Test condition C or D	
(2) Ultrasonic		(2) Test condition C or D	
(3) Flip-chip		(3) Test condition F	
(4) Beam lead		(4) Test condition H	
(d) Die shear test		Per method 2019 for the applicable die size	3(0)
Subgroup 3			
Solderability	2003 or 2022	Soldering temperature of 245°C ±5°C	LTPD =15
Subgroup 4			
(a) Lead integrity[7]	2004	Test condition B_2, lead fatigue	2(0)
(b) Seal	1014	As applicable	
(a) Fine			
(b) Gross			
(c) Lid torque[5]	2024	As applicable	
Subgroup 5			
(a) Electrical parameters[6]		Group A, subgroups 1, 2, 3: Read and record Group A, subgroups 4-11: Attributes	
(b) Steady state life[3]	1005	Test condition C, D, or E	LTPD = 5
(c) Electrical parameters		Group A, subgroups 1, 2, 3: Read and record (including Deltas) Group A, subgroups 4-11: Attributes	

Quality Conformance Testing

Group B Tests for Class S and Level /MS and /1 Devices — Continued

Test	MIL-STD-883 Method	MIL-STD-883 Condition	Quantity/(accept no.) or LTPD
Subgroup 6[2]			
(a) Electrical parameters[6]		Group A, subgroups 1, 2, 3: Read and record	LTPD = 15
(b) Temperature cycling	1010	Condition C, 100 cycles min.	
(c) Constant acceleration	2001	Test condition E: Y_1 orientation only	
(d) Seal	1014		
(a) Fine			
(b) Gross			
(e) Electrical parameters		Group A, subgroups 1, 2, 3: Read and record	
Subgroup 7[9]			
(a) Electrical parameters		Group A, subgroup 1	
(b) Electrostatic discharge sensitivity	3015		15(0)
(c) Electrical parameters		Group A, subgroup 1	

Notes:

[1]This test is required only if it is a glass-frit-sealed package.
[2]For Class S and Level /MS lot quality conformance and qualification testing, all samples for subgroups B_2 must have been through the complete sequence of subgroup B_6 tests.
[3]The same test temperature that was used for burn-in shall be used for the steady state life test.
[4]Unless otherwise specified, the LTPD sample size for conditions C and D is the number of bond pulls selected from a minimum number of four devices, and for condition F or H is the number of dice (not bonds).
[5]Lid torque test shall apply only to glass-frit-sealed packages.
[6]Read and record data from Group A for qualification is acceptable and additional testing is not required.
[7]For leadless-chip-carrier packages only, use test condition D.
[8]Group B for Level /MS is performed by customer order only.
[9]Required for JAN CD54HC-series product as modified in the applicable Detail Specifications.

Group B Tests for Class B and Level /3 and /3A Devices

Test	MIL-STD-883 Method	MIL-STD-883 Condition	Quantity/(accept no.) or LTPD
Subgroup 1			
(a) Physical dimensions	2016		2 devices (no failures)
Subgroup 2			
(a) Resistance to solvents	2015		4 devices (no failures)
Subgroup 3			
(a) Solderability	2022 or 2003	Soldering temperature of 245 ±5°C	15
Subgroup 4			
(a) Internal visual and mechanical	2014	Failure criteria from design and construction requirements of applicable procurement document	1 device (no failures)
Subgroup 5			
(a) Bond strength	2011		15
(1) Thermocompression		(1) Test condition C or D	
(2) Ultrasonic or wedge		(2) Test condition C or D	
(3) Flip-chip		(3) Test condition F	
(4) Beam lead		(4) Test condition H	
Subgroup 6[1]			
(a) Internal water-vapor content	1018	1,000 PPM Maximum water content at 100°C	3 devices (0 failures) or 5 devices (1 failure)
Subgroup 7			
(a) Seal	1014	As applicable	5
(1) Fine			
(2) Gross			

Quality Conformance Testing

Group B Tests for Class B and Level /3 and /3A Devices — Continued

Test	MIL-STD-883 Method	MIL-STD-883 Condition	Quantity/(accept no.) or LTPD
Subgroup 8 (QMOS only)[2]			
(a) Electrical parameters		Group A, subgroup 1	
(b) Electrostatic discharge sensitivity classification	3015		15(0)
(c) Electrical parameters		Group A, subgroup 1	

Notes:
[1]Subgroup 6 is required only if package contains a desiccant.
[2]Subgroup 8 is required if device meets category B of method 3015.

Group C (die-related tests) for Class B and Level /3 and /3A Devices Only

Test	MIL-STD-883 Method	MIL-STD-883 Condition	Quantity/(accept no.) or LTPD
Subgroup 1			
(a) Steady state life	1005	Test condition to be specified (504 hours at 135°C)	5
(b) End-point electrical parameters		As specified in the applicable device specification for JAN and Group A subgroups 1, 2 and 3 including 25°C deltas for Levels /3 and /3A.	
Subgroup 2			
(a) Temperature cycling	1010	Test condition C	15
(b) Constant acceleration	2001	Test condition E min. (for large packages, see 3) Y_1 orientation only	
(c) Seal	1014	As applicable	
(1) Fine			
(2) Gross			
(d) Visual examination*			
(e) End-point electrical parameters		As specified in the applicable device specification for JAN and Group A subgroups 1, 2 and 3 for Levels /3 and /3A	

*Visual examination in accordance with MIL-STD-883C, Method 1010 or 1011.

Group D (package-related tests) (for all classes)

Test	MIL-STD-883 Method	MIL-STD-883 Condition	Quantity/(accept no.) or LTPD
Subgroup 1			
(a) Physical dimensions	2016		15
Subgroup 2			
(a) Lead integrity	2004	Test condition B_2 (lead fatigue)	15
(b) Seal			
(1) Fine	1014	As applicable	
(2) Gross			
Subgroup 3			
(a) Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum.	15
(b) Temperature cycling	1010	Test condition C, 100 cycles minimum.	
(c) Moisture resistance	1004		
(d) Seal	1014	As applicable	
(1) Fine			
(2) Gross			
(e) Visual examination		Per visual criteria of method 1004 and 1010	
(f) End-point electrical parameters		As specified in the applicable device specification for JAN and Group A subgroups 1, 2 and 3 for Levels /3 and /3A	

Quality Conformance Testing

Group D (package-related tests) (for all classes) — Continued

Test	MIL-STD-883 Method	MIL-STD-883 Condition	Quantity/(accept no.) or LTPD
Subgroup 4			
(a) Mechanical shock	2002	Test condition B minimum	15
(b) Vibration, variable frequency	2007	Test condition A minimum	
(c) Constant acceleration	2001	Test condition E minimum Y_1 orientation only	
(d) Seal	1014	As applicable	
(1) Fine			
(2) Gross			
(e) Visual examination[1]			
(f) End-point electrical parameters		As specified in the applicable device specification for JAN and Group A Subgroups 1, 2 and 3 for Levels /3 and /3A	
Subgroup 5			
(a) Salt atmosphere	1009	Test condition A minimum	15
(b) Seal	1014	As applicable	
(1) Fine			
(2) Gross			
(c) Visual examination		Per visual criteria of method 1009	
Subgroup 6			
(a) Internal water-vapor content	1018	5,000 ppm maximum water content at 100°C	3 devices (0) failures or 5 devices (1 failure)
Subgroup 7			
(a) Adhesion of lead finish[3]	2025		15
Subgroup 8			
(a) Lid torque[4]	2024		5(0)

Notes:
[1]Visual examination shall be in accordance with method 1010 or 1011.
[2]The adhesion of lead finish test shall not apply for leadless-chip-carrier packages.
[3]LTPD based on number of leads.
[4]For glass-frit-sealed packages.

Group E (radiation-hardness assurance tests)

Test	MIL-STD-883 Method	MIL-STD-883 Condition	Class S Quantity/ accept number	Class S Notes	Class B Quantity/ accept number	Class B Notes
Subgroup 2						
Steady-state total dose irradiation	1019	25°C 10V for all levels Standard CMOS Product	4/0	4, 5	11/0	1
Endpoint electrical parameters		As specified per detail specification or DATABOOK	2/0			

NOTES:
[1]Per wafer lot.
[2]Per wafer for device types with less than or equal to 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius, and spaced uniformly around this radius.
[3]Per wafer for device types with greater than 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius and spaced uniformly around this radius.
[4]Subgroup 1: RCA does not perform neutron irradiation per MIL-STD-883, Method 1017.
[5]Testing may be performed on wafer-packaged devices prior to screening Method 5004.

Quality Conformance Testing

LTPD sampling plans

Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent-defective equal to the specified LTPD will not be accepted (single sample).

Max. Percent Defective (LTPD) or λ	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3
Acceptance Number (c) (r = c + 1)	**Minimum Sample Sizes** (For device-hours required for life test, multiply by 1000)											
0	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)
1	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)
2	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)	266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)
3	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)
4	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)
5	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)
6	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)
7	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)
8	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)
9	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)
10	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)

Note #1. Sample sizes are based upon the Poisson exponential binomial limit. **Note #2.** The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only. **Note #3.** This sampling plan is derived from Table C-1 in Appendix C of MIL-S-19500.

RCA High-Reliability Power Devices Capability

RCA also offers a broad line of high-reliability power devices for military, aerospace, and commerical equipment applications. Types qualified as JAN, JANTX, and JANTXV devices include power transistors, power MOSFETs, and SCRs. All RCA high-reliability solid-state power devices are processed in accordance with the provisions of MIL-S-19500 General Specifications and tested in accordance with MIL-STD-750 Test Methods.

Additional RCA high-reliability power devices include types that are not yet covered by Military specifications but that are processed and screened to specifications patterned after the military standards; types that are designed and processed to be resistant to neutron and gamma radiation; and types that can be supplied to custom specifications.

JAN M38510 CD4000-Series CMOS ICs

Reliability Classes

The purpose of the JAN M38510 program is to achieve standardization among integrated-circuit suppliers and to assure delivery of devices whose long-term life will satisfy the requirements of the system for which they were intended.

Two reliability classes — S and B — are described in MIL-M-38510; the screening classes are performed according to MIL-STD-883, method 5004. Class S devices are of the highest reliability level and are intended for critical applications where replacement of components is not practical.

The Qualification and Quality Conformance Inspection tests delineated in MIL-STD-883 Method 5005 consist of:

Groups A and B — device electrical and mechanical construction evaluation tests respectively.

Groups C and D — accelerated stress tests that subject devices to stress levels greater than those normally experienced in a typical application.

Group A consists of electrical tests defined by the Device specification. (MIL-STD-883 Method 5005)

Group B (Class B) consists of Package and Internal Mechanical Strength tests. (MIL-STD-883 Method 5005)

Group B (Class S) consists of Package and Internal Mechanical Strength and Long-Term Reliability tests. (MIL-STD-883 Method 5005)

Group C (Class B only) consists of Chip-Related Long-Term Reliability tests. (MIL-STD-883 Method 5005)

Group D consists of Package and Construction Environmental tests. (MIL-STD-883 Method 5005)

Group E Radiation-Hardness Verification Testing. (MIL-STD-883 Method 5005)

Qualification Inspection Tests (QI) are those tests defined by MIL-M-38510 as required for initial qualification of a device or package type to a given reliability class. Quality Conformance Inspection (QCI) Tests are those tests defined by MIL-M-38510 to evaluate production line quality of qualified devices. QCI tests are an on-going inspection process performed at periodic intervals defined by MIL-M-38510. QCI testing is the foundation of statistical process evaluation. Electrical end-point test limits are defined by MIL-M-38510 and are more demanding of CMOS than of TTL in areas of quiescent current and input leakage current. DC and AC parameters are measured at -55°C, +25°C and +125°C.

In summary, then, devices are manufactured and tested in accordance with the MIL-M-38510 (detailed and general) specification, which includes methods and procedures of the Military Standard MIL-STD-883.

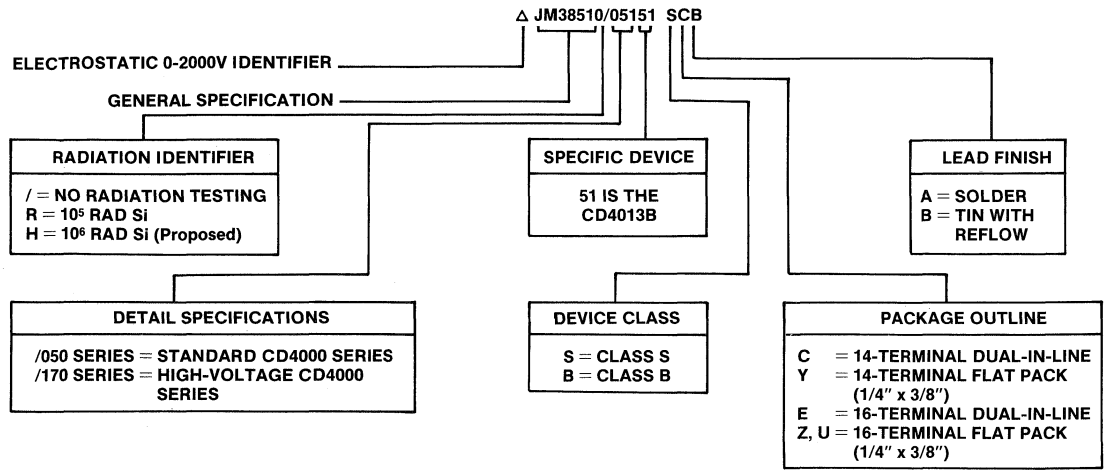
CMOS integrated circuits are supplied to MIL-M-38510 under a series of /050 and /170 numbers. Detailed ratings and characteristics for these integrated circuits are given in the /050 and /170 detailed electrical specifications. MIL-M-38510 specifications can be obtained from the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA, 19120.

Nomenclature

The MIL-M-38510 type number is a guide to the detailed electrical specification, the basic device type, the reliability class, and lead finish.

The chart below explains the nomenclature structure for the MIL-M-38510 products.

Guide to the reliability class, package, lead finish, radiation-hardness assurance level, and electrostatic sensitivity of RCA high-reliability CMOS integrated circuits processed in accordance with MIL-M-38510.



Index to RCA JAN M38510 CD4000 Series

RCA JAN Qualified-Parts Listing and MIL-M-38510 Detail Specifications (Slash Sheets) as of May 1985.

Detail Specification	RCA Type	Available JAN Devices S	B	1×10^5 Rad Si
MIL-M-38510/5001	CD4011A		A	A
02	CD4012A		A	A
03	CD4023A		A	A
51	CD4011B	A	A	A
52	CD4012B	A	A	A
53	CD4023B	A	A	A
MIL-M-38510/5101	CD4013A		A	A
02	CD4027A		A	I
03	CD4043A			
51	CD4013B	A	A	A
52	CD4027B	I	A	I
53	CD4043B			
MIL-M-38510/5201	CD4000A		A	
02	CD4001A		A	A
03	CD4002A		A	A
04	CD4025A		A	I
51	CD4000B			
52	CD4001B	A	A	A
53	CD4002B	A	A	A
54	CD4025B	I	A	I
MIL-M-38510/5301	CD4007A		A	I
02	CD4019A		A	I
03	CD4030A			
04	CD4048A			
51	CD4007UB	I	I	I
52	CD4019B	I	I	I
53	CD4030B	I	A	A
54	CD4048B			
MIL-M-38510/5401	CD4008A			
51	CD4008B	I	I	I
MIL-M-38510/5501	CD4009A			
02	CD4010A			
03	CD4049A		A	A
04	CD4050A		A	A
05	CD4041A			
51	CD4009UB			
52	CD4010B			
53	CD4049UB	A	A	A
54	CD4050B	A	A	A
55	CD4041UB	I	I	I
MIL-M-38510/5601	CD4017A		A	I
02	CD4018A			
03	CD4020A		A	I
04	CD4022A		A	I
05	CD4024A		A	I
51	CD4017B	A	A	A
52	CD4018B	I	A	I
53	CD4020B	A	A	A
54	CD4022B	I	I	I
55	CD4024B	I	A	I

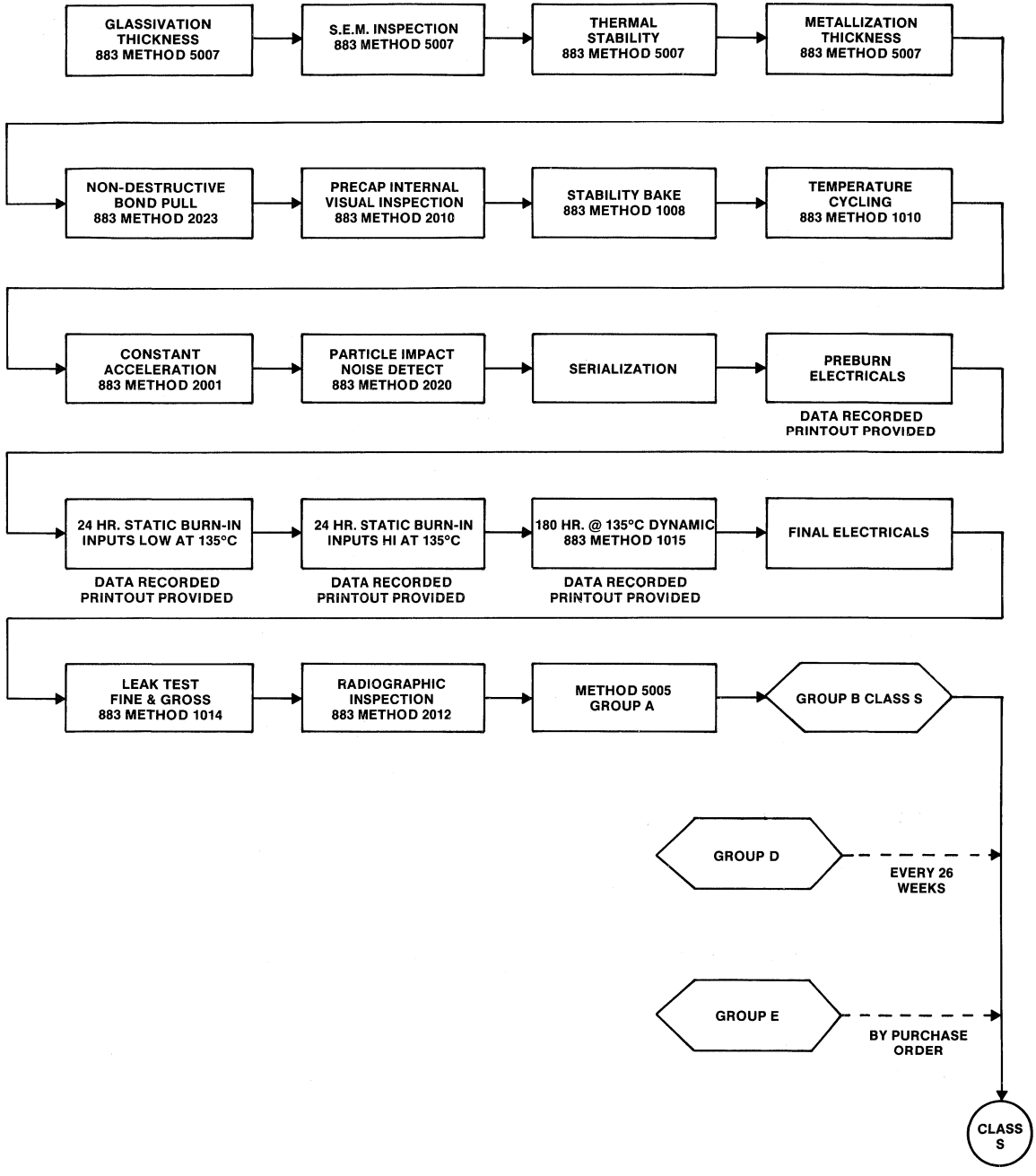
Detail Specification	RCA Type	Available JAN Devices S	B	1×10^5 Rad Si
MIL-M-38510/5701	CD4006A		A	
02	CD4014A		A	I
03	CD4015A		A	I
04	CD4021A		A	I
05	CD4031A		A	
06	CD4034A			
51	CD4006B			
52	CD4014B	I	A	I
53	CD4015B	I	I	I
54	CD4021B	I	A	I
55	CD4031B			
56	CD4034B			
MIL-M-38510/5801	CD4016A			
02	CD4066A			
51	CD4016B			
52	CD4066B	I	I	I
MIL-M-38510/5901	CD4028A			
51	CD4028B	I	I	I
MIL-M-38510/17001	CD4081B	A	A	A
02	CD4082B	A	A	A
03	CD4073B	A	A	A
MIL-M-38510/17101	CD4071B	A	A	A
02	CD4072B	A	A	A
03	CD4075B	A	A	A
MIL-M-38510/17201	CD4085B	A	A	A
02	CD4086B	A	A	A
03	CD4070B	A	A	A
04	CD4077B	A	A	A
MIL-M-38510/17301	CD4514B			
02	CD4515B			
03	CD4532B			
04	CD4555B			
05	CD4556B			
MIL-M-38510/17401	CD4069UB	A	A	A
02	CD40107B			
03	CD4502B	A	A	A
04	CD40109B			
MIL-M-38510/17501	CD4076B			
02	CD4095B			
03	CD4096B			
04	CD4098B	A	A	A
05	CD40174B			
MIL-M-38510/17601	CD4099B	A	A	A
02	CD4508B			
MIL-M-38510/17701	CD4093B			
02	CD40106B			
MIL-M-38510/17801	CD4067B			
02	CD4097B			
03	CD40257B			

A = available P = proposed qual. I = in process 1985 (MIL-M-38510 detailed electrical test programs are available.)

For current availability, call your RCA authorized distributor or nearest sales office.

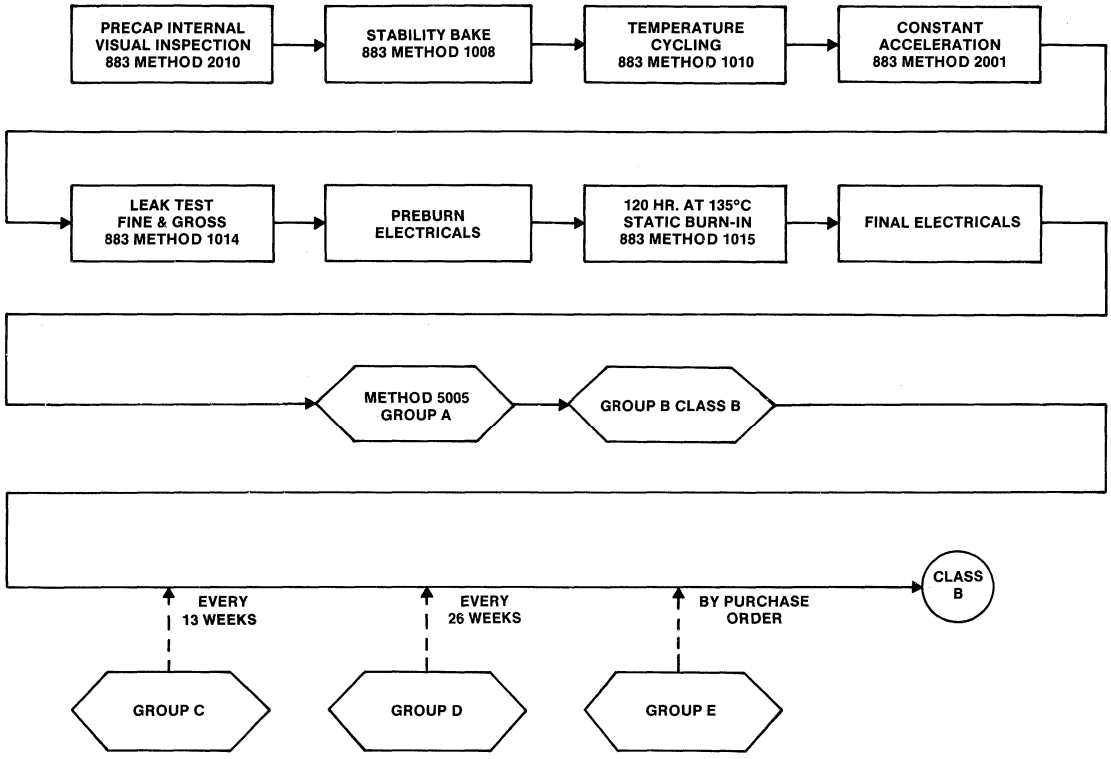
Product Flow Charts

JAN CLASS S CMOS ICs PRODUCT FLOW CHART



Product Flow Charts

JAN CLASS B CMOS ICs PRODUCT FLOW CHART



Comparison of Class S/Class B Screening Tests

Screening Test	Class S	Class B	Screening Test	Class S	Class B
Glassivation Thickness	Yes	—	Preburn Electrical	Yes	Yes
SEM Inspection	Yes	—	24-Hr. Static Burn-In,		
Thermal Stability	Yes	—	Inputs Low @ 135°C	Yes	—
Metallization Thickness	Yes	—	24-Hr. Static Burn-In,		
Non-Destructive Bond Pull	Yes	—	Inputs High @ 135°C	Yes	—
Precap Visual Inspection	Yes	Yes	120-Hr. Static Burn-In @ 135°C	—	Yes
Stability Bake	Yes	Yes	180-Hr Dynamic Burn-In @ 135°C	Yes	—
Temperature Cycling	Yes	Yes	Final Electricals	Yes	Yes
Constant Acceleration	Yes	Yes	Fine & Gross Leak Tests	Yes	—
Serialization	Yes	—	Radiographic Inspection	Yes	—
Fine & Gross Leak Tests	—	Yes			

High-Reliability CD4000B Slash-Series CMOS ICs

High-Reliability CD4000B-Series High-Voltage CMOS ICs

The RCA high-reliability CD4000B series of high-voltage CMOS integrated circuits consists of a broad range of SSI, MSI-1, and MSI-2 (LSI) functions from simple gates to complex counters, registers, and arithmetic circuits. Specific design features for CMOS devices and the performance advantages of CMOS technology — low power consumption, high noise immunity, high speed, high fanout, TTL and DTL logic compatibility, excellent temperature stability, and fully protected inputs and outputs — provide the logic system designer with a capability to achieve outstanding performance, high reliability, and simplified circuitry in a wide variety of equipment designs.

Features

- 100% tested for quiescent current at 20V
- Maximum input current (leakage) of 1μA at 18 V over full package-temperature range; 100 nA at 18 V at 25°C
- Standardized symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V, 2 V at V_{DD} =10 V, 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for description of 'B' Series CMOS Devices"

Buffered Vs. Unbuffered Gates

The new industry standard establishes a suffix "UB" for CMOS products that meet all B-series specifications except that the logical outputs of the devices are not buffered and the V_{IL} and V_{IH} specifications are 20% and 80% of V_{DD}, respectively. The suffix "B" defines high-voltage buffered-output devices in which the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present.

RCA will supply both buffered ("B") and unbuffered ("UB") versions of the popular NOR and NAND gates to make available to designers the advantages of both. The following table briefly compares the features of the two versions.

Characteristic	Buffered Version ("B")	Unbuffered Version ("UB")
Propagation Delay (Speed)	Moderate	Fast
Noise Immunity/Margin	Excellent	Good
Output Impedance and Output Transition Time	Constant	Variable
AC Gain	High	Low
Output Oscillation for Slow Inputs	Yes	No
Input Capacitance	Low	High

RCA Compliance to MIL-STD-883, Rev. C

RCA provides CD4000-series parts that are in full compliance with MIL-STD-883C, Paragraph 1.2.1. Two different types of product are provided to meet the requirements of this paragraph, Class S and Class B.

Slash MS (.../MS) meets Class S requirements when the optional Group B life conformance test is performed. Electrical tests are performed to black-dot parameters described in this section.

Slash 3A (.../3A) meets Class B requirements. Electrical tests are performed to black-dot parameters described in this section.

RCA also provides CD4000-series parts that meet the requirements of MIL-STD-883C, Paragraph 1.2.2. This family of parts has the following designation.

Slash 3 (.../3) meets most of the requirements of a Class B part as described in details presented in the table entitled "Manufacturing and Conformance Testing for the High-Reliability CD4000-Series ICs."

Screening Levels for RCA High-Reliability Slash-Series CMOS Integrated Circuits

Screening Levels†		Application	Description
Packaged Devices (D, F, K, or J Suffix)			
/MS	Class S with SEM Inspection and Condition A Precap Visual Inspection	Aerospace and Missiles	For devices intended for use where maintenance and replacement are difficult and reliability is imperative
/MSR	Same as /MS + Radiation Hardened to 10^5 rads(Si)		
/MSH	Same as /MS + Radiation Hardened to 10^6 rads(Si)		
/3A	Class B	Military and Industrial For example, in Airborne Electronics	For devices intended for use where maintenance and replacement can be performed but are difficult and expensive
/3	Class B, modified		
Chips (H Suffix)			
/S	SEM Inspection and Condition A Visual Inspection	Aerospace and Missiles	For hybrid applications where maintenance and replacement are extremely difficult and reliability is imperative
/SR	Same as /S + Radiation Hardened to 10^5 rads(Si)		
/SH	Same as /S + Radiation Hardened to 10^6 rads(Si)		
/M	Condition B Precap Visual Inspection	Military and Industrial	For general applications

†For screening details refer to Total Lot Screening chart.

Function Selection Chart

Function	Type No.	No. of Pins
Gates		
NOR/NAND		
Dual 4-input NOR	**CD4002B**	14
	CD4002UB	14
Dual 4-input NAND	**CD4012B**	14
	CD4012UB	14
Triple 3-input NOR	**CD4025B**	14
	CD4025UB	14
Triple 3-input NAND	**CD4023B**	14
	CD4023UB	14
Quad 2-input NOR	**CD4001B**	14
	CD4001UB	14
Quad 2-input NAND	**CD4011B**	14
	CD4011UB	14
8-input NOR/OR	**CD4078B**	14
8-input NAND/AND	**CD4068B**	14
Dual 3-input NOR plus inverter	**CD4000B**	14
	CD4000UB	14
Dual 2-input NAND buffer/driver	**CD40107B**	14
OR/AND		
Dual 4-input OR	**CD4072B**	14
Dual 4-input AND	**CD4082B**	14
Triple 3-input OR	**CD4075B**	14
Triple 3-input AND	**CD4073B**	14
Quad 2-input OR	**CD4071B**	14
Quad 2-input AND	**CD4081B**	14
Buffers and Inverters		
Dual complementary pair plus inverter	**CD4007UB**	14
Hex inverter	**CD4069UB**	14
Hex inverter/buffer (3-state)	**CD4502B**	16
Hex buffer (3-state non-inverting)	**CD4503B**	16
Hex buffer/converter (inverting)	**CD4009UB**	16
	CD4049UB	16
Hex buffer/converter (non-inverting)	**CD4010B**	16
	CD4050B	16
Quad true/complement buffer	**CD4041UB**	14
Dual 2-input NAND buffer/driver	**CD40107B**	14
Multifunction/AOI		
Quad exclusive-OR	**CD4030B**	14
	CD4070B	14
Quad exclusive-NOR	**CD4077B**	14
Quad AND/OR Select	**CD4019B**	16
Dual 2-wide, 2-input AND/OR invert (AOI)	**CD4085B**	14
Expandable 4-wide, 2-input AND/OR invert (AOI)	**CD4086B**	14
Multifunctional expandable 8-input (3-state output)	**CD4048B**	16
Decoders/Encoders		
BCD-to-decimal decoder	**CD4028B**	16
8-input priority encoder	**CD4532B**	16
10-line to 4-line BCD priority encoder	**CD40147B**	16
4-bit latch/4-to-16 line decoder (outputs high)	**CD4514B**	24
4-bit latch/4-to-16 line decoder (outputs low)	**CD4515B**	24
Dual 1-of-4 decoder/demultiplexer (outputs high)	**CD4555B**	16
Dual 1-of-4 decoder/demultiplexer (outputs low)	**CD4556B**	16
Schmitt Trigger		
Quad 2-input NAND	**CD4093B**	14
Hex	**CD40106B**	14
Interface		
Quad low-to-high voltage	**CD40109B**	16
Hex high-to-low voltage (inverting)	**CD4009UB**	16
	CD4049UB	16
Hex high-to-low voltage (non-inverting)	**CD4010B**	16
	CD4050B	16
Dual 2-input NAND buffer/driver	**CD40107B**	14
8-bit bidirectional CMOS-to-TTL level converter	**CD40116**	22
Multivibrators		
Monostable/astable	**CD4047B**	14
Dual monostable	**CD4098B**	16
Dual precision monostable	**CD4538B**	16
Flip-Flops		
Dual "D" with set/reset capability	**CD4013B**	14
Dual "J-K" with set/reset capability	**CD4027B**	16
Gated "J-K" (non-inverting)	**CD4095B**	14
Gated "J-K" (inverting and non-inverting)	**CD4096B**	14
Hex "D"	**CD40174B**	16
4-bit "D" with 3-state outputs	**CD4076B**	16
Quad "D"	**CD40175B**	16
Latches		
Quad clocked "D"	**CD4042B**	16
Quad NOR R/S (3-state outputs)	**CD4043B**	16
Quad NAND R/S (3-state outputs)	**CD4044B**	16
Dual 4-bit	**CD4508B**	24
8-bit addressable	**CD4099B**	16
	CD4724B	16
Registers		
Shift Registers-Static		
Dual 4-stage with serial input/parallel output	**CD4015B**	16
18-stage	**CD4006B**	14
64-stage	**CD4031B**	16
Dual 64-bit	**CD4517B**	16
8-stage with synchronous parallel or serial input/serial output	**CD4014B**	16
8-stage with asynchronous parallel input or synchronous serial input/serial output	**CD4021B**	16
4-stage parallel-in/parallel-out with J-K input and true/complement output	**CD4035B**	16
4-bit universal bidirectional with 3-state outputs	**CD40104B**	16
4-bit universal bidirectional with asynchronous master reset	**CD40194B**	16
8-stage bidirectional parallel or serial input/parallel output	**CD4034B**	24
32-bit left/right	**CD40100B**	16
8-stage shift-and-store bus	**CD4094B**	16
Storage Registers		
8-bit addressable latch	**CD4099B**	16
	CD4724B	16
4-bit "D"-type with 3-state outputs	**CD4076B**	16
4 x 4 Multiport	**CD40108B**	24
4 x 4 Multiport	**CD40208B**	24
FIFO Buffer Registers		
4-bit x 16 word	**CD40105B**	16
Counters		
Binary Ripple		
7-stage	**CD4024B**	14
12-stage	**CD4040B**	16
14-stage	**CD4020B**	16
14-stage counter/divider and oscillator	**CD4060B**	16
Timers		
21-stage	**CD4045B**	14
Programmable	**CD4536B**	16
	CD4541B	14
Synchronous		
Decade counter/divider plus 10 decoded decimal outputs	**CD4017B**	16
Divide-by-8 counter/divider with 8 decimal outputs	**CD4022B**	16

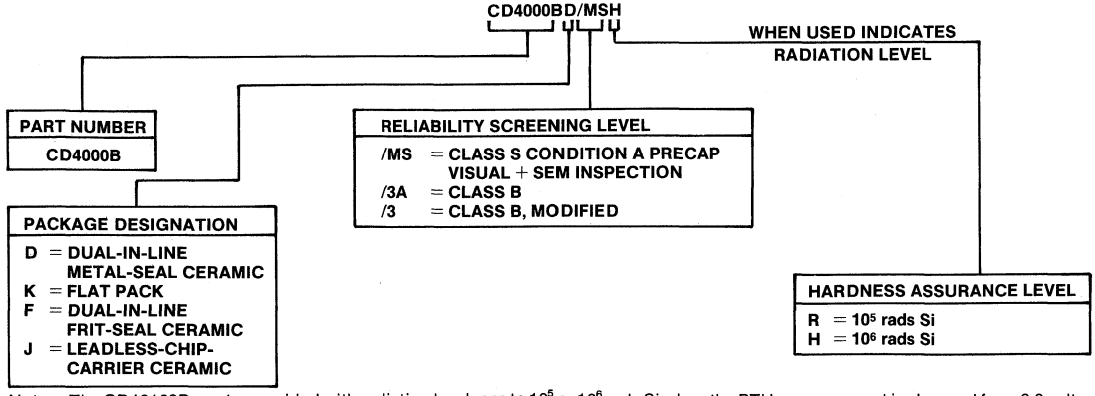
Function Selection Chart

Function	Type No.	No. of Pins
Presettable divide-by-"N" counter, fixed or programmable	**CD4018B**	16
Presettable up/down counter, binary or BCD-decade	**CD4029B**	16
Presettable 4-bit BCD up/down counter	**CD4510B**	16
Presettable 4-bit binary up/down counter	**CD4516B**	16
Presettable 2-decade BCD down counter	**CD40102B**	16
Presettable 8-bit binary down counter	**CD40103B**	16
Presettable 4-bit BCD up/down counter	**CD40192B**	16
Presettable 4-bit binary up/down counter	**CD40193B**	16
Dual BCD up counter	**CD4518B**	16
Dual binary up counter	**CD4520B**	16
Decade counter/asynchronous clear	**CD40160B**	16
Binary counter/asynchronous clear	**CD40161B**	16
Decade counter/synchronous clear	**CD40162B**	16
Binary counter/synchronous clear	**CD40163B**	16
Display Drivers		
With Counter		
Decade counter/divider with 7-segment display outputs and display enable	**CD4026B**	16
Decade counter/divider with 7-segment display outputs and ripple blanking	**CD4033B**	16
Up/Down Counter-Latch Decoder-Driver	**CD40110B**	16
For Liquid-Crystal-Display Drive		
4-segment display driver	**CD4054B**	16
BCD-to-7-segment decoder/driver with "display-frequency" output	**CD4055B**	16
BCD-to-7-segment decoder/driver with strobed-latch function	**CD4056B**	16
	CD4543B	16
For Light-Emitting-Diode Drive		
BCD-to-7-segment latch decoder/driver	**CD4511B**	16
Multiplexers/Demultiplexers		
Analog		
Triple 2-channel	**CD4053B**	16
Differential 4-channel	**CD4052B**	16
Single 8-channel	**CD4051B**	16
Differential 8-channel	**CD4097B**	24
Single 16-channel	**CD4067B**	24
Quad bilateral switch	**CD4016B**	14
Quad bilateral switch	**CD4066B**	14
Digital (Data Selectors)		
Quad AND/OR select	**CD4019B**	16
Dual 1-of-4 decoder/demultiplexer (outputs high)	**CD4555B**	16
Dual 1-of-4 decoder/demultiplexer (outputs low)	**CD4556B**	16
Quad 2-line-to-1-line	**CD40257B**	16
8-channel	**CD4512B**	16
Phase-Locked Loop		
Micropower	**CD4046B**	16
Arithmetic Circuits		
Adders/Comparators		
4-bit full adder with parallel carry out	**CD4008B**	16
Triple serial adder, positive logic	**CD4032B**	16
Triple serial adder, negative logic	**CD4038B**	16
4-bit magnitude comparator	**CD4063B**	16
	CD4585B	16
Quad exclusive-OR gate	**CD4030B**	14
Quad exclusive-OR gate	**CD4070B**	14
Quad exclusive-NOR gate	**CD4077B**	14
ALU/Rate Multipliers		
4-bit arithmetic logic unit	**CD40181B**	24
BCD rate multiplier	**CD4527B**	16
Binary rate multiplier	**CD4089B**	16
Look-ahead-carry block	**CD40182B**	16
Parity Generator/Checker		
9-bit	**CD40101B**	14
Multiport Register		
4 x 4	**CD40108B**	24
4 x 4	**CD40208B**	24
8 x 1	**CD4034B**	24
Quad Bilateral Switches		
For transmission or multiplexing of analog or digital signals	**CD4016B**	14
	CD4066B	14

Guide to the reliability class, package, and radiation-hardness assurance level of RCA high-reliability CD4000-series integrated circuits.

The type number for RCA slash-series integrated circuits identifies not only the basic device, but also the screening level, package, and lead finish.

The chart below explains the nomenclature structure for the RCA MIL-STD-883 slash-series CMOS integrated circuits.



Note: The CD40109B can be provided with radiation hardness to 10^5 or 10^6 rads Si when the PTH measurement is changed from 2.8 volts maximum to 3.5 volts maximum due to part design and wafer processing.

Manufacturing and Conformance Testing

The RCA slash-series of devices is intended to provide reliable IC's of an equivalent nature to JAN Class S or B where no JAN specification exists or RCA is not listed on QPL for the CD type desired. These slash-series of levels are CD4XXXB/MS and CD4XXXB/3 or /3A. The following table indicates which RCA package types are available, manufacturing location, manufacturing differences, conformance testing and data available.

This book is not intended to show complete electrical characteristics for every high-reliability device but is intended to be used in conjunction with the latest issue of the appropriate commercial CMOS Databook. For complete electrical characteristics, application notes and other general information regarding RCA CMOS, consult the latest RCA commercial CMOS Databook or Data Sheet. These may be obtained by contacting the RCA Sales Office nearest you.

Manufacturing and Conformance Testing for the High-Reliability CD4000-Series ICs[17]

Characteristic	MS[1]			/3A[2]	/3[3]		
Series	B	B	B	B	B[4]	B[4]	B
Package Options	F	D, K	J	F	F	D, K	J
Die Attach	Eutectic	Epoxy	Eutectic or Epoxy	Eutectic	Glass	Epoxy	Eutectic or Epoxy
Lead Finish	Matte Tin Reflowed	Solder Coat	Gold Contacts	Matte Tin Reflowed	Matte Tin	Solder Coat	Gold Contacts
Manufacturing Location	U.S.	U.S.	U.S.	Off Shore	Off Shore	Off Shore	U.S. or Off Shore
Screens	5004 Class S	5004 Class S	5004[15] Class S	5004 Class B	5004 Class B	5004 Class B	5004 Class B
Conformance Tests							
Group A	Yes	Yes	Yes	5005	Yes	Yes	Yes
Class S Group B	Yes[5]	Yes[5]	Yes[5]	5005	—	—	—
Class B Group B	—	—	—	5005[6]	Generic[7]	Generic[8]	Generic[8]
Class B Group C	—	—	—	5005	Generic[7]	Generic[8]	Generic[8]
Group D	Generic[7]	Generic[7]	Generic[7]	5005	Generic[7]	Generic[8]	Generic[8]
Group E Subgp2B[18]	Yes	Yes	Yes	5005	—	—	—
Data Supplied							
C of C[9]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Group A Attribute[10]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Variables — Burn-In[11]	Yes	Yes	Yes	—	—	—	—
Radiographic[12]	Yes	Yes	Yes	—	—	—	—
SEM[13]	Yes	Yes	Yes	—	—	—	—
Radiation C of C[14]	Yes	Yes	Yes	—	—	—	—
Conformance Test[16]	If Ordered	If Ordered	If Ordered	If Ordered	If Ordered	If Ordered	If Ordered

NOTES:

1. Slash MS is intended for aerospace applications for use where JAN Class S is not available. Device screening follows MIL-STD-883 Class S as described above.
2. Slash 3A meets MIL-STD-883 Class B.
3. Slash 3 meets MIL-STD-883 Class B as described above.
4. A series available upon special request.
5. Class S Group B can be ordered as an option.
6. For Slash 3A Series, Group B will conform to MIL-STD-883 run on each inspection sub-lot using the alternate Group B Method.
7. Conformance tests are run continually on selected device types and packages considered representative of entire series.
8. Conformance tests are not run on a continual basis but available generic data can be supplied.
9. Certificate of Compliance (C of C) signed by an RCA Representative provides identity, customer order number, lists and certifies tests, methods, and conditions per MIL-STD-883.
10. Group A subgroup summary of attributes data.
11. Variables data summary for pre burn-in and post burn-in with deltas.
12. Radiographic inspection (two views) film and film inspection record (No penatrameter images supplied).
13. SEM inspection Certificate of Compliance includes lot identification and three photos.
14. Certificate of Compliance for radiation assurance testing for 10^5 and 10^6 rad (Si) devices, suffix "R" or "H".
15. The note in method 2010 paragraph 3.1.5.1A is not applicable to these devices.
16. Attributes data summary.
17. See "Total Lot Screening for RCA High-Reliability CD4000B-Series ICs" chart for complete screening and testing.
18. For rad-hard devices only.

Screening Availability

The table below indicates the RCA screening performed on /MS, /3 and /3A devices. The /MS is equivalent to MIL-STD-883 Class S and the /3 and /3A are equivalent to MIL-STD-883 Class B screens to Method 5004. As shown in the Manufacturing and Conformance Testing table, the differences between a /3 and /3A is the lead finish and pellet mounting technique. It should be noted that all CD4XXXB-Series wafers are manufactured at the RCA JAN-certified plant in Findlay, Ohio and any type shown as U.S. manufactured is completely assembled and tested on our JAN-certified line.

Total Lot Screening for RCA High-Reliability CD4000B-Series ICs

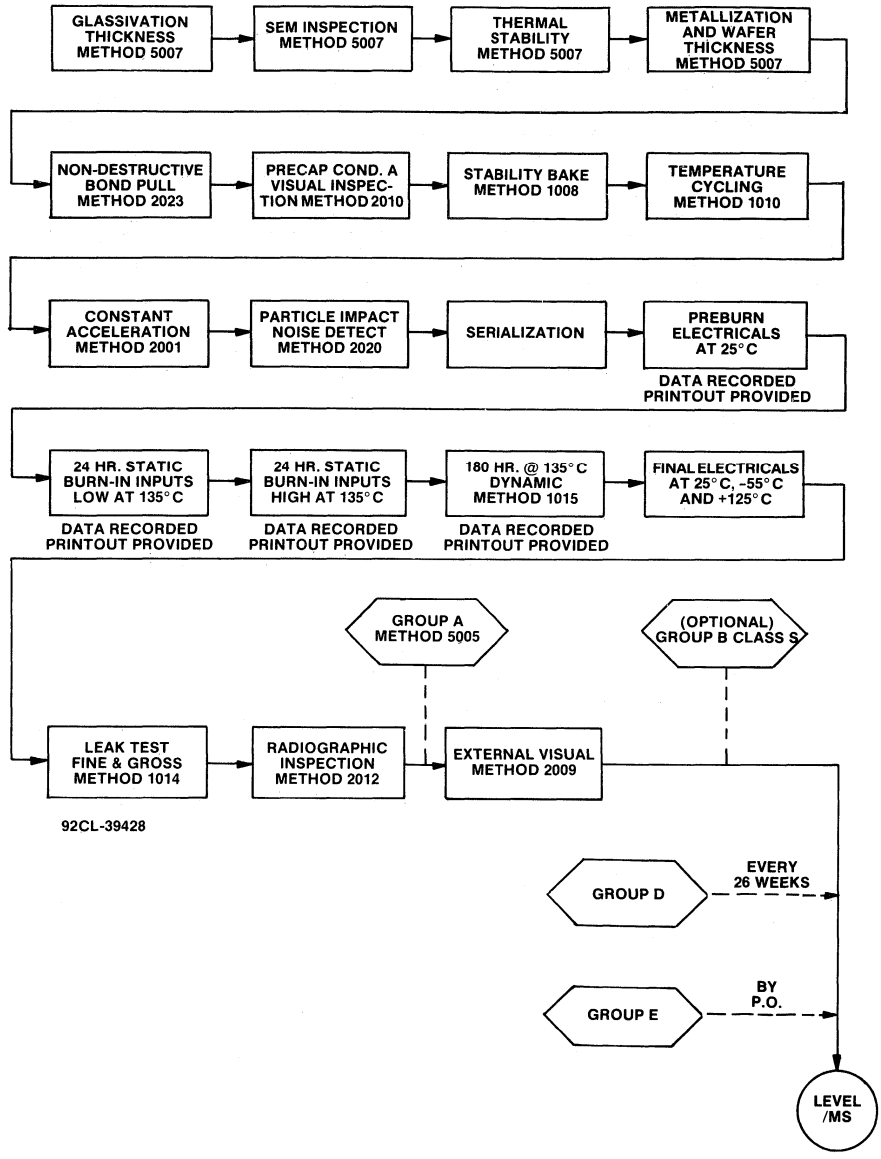
Screening Test	Conditions	Method	RCA/Level		Notes
			MS	3, 3A	
Wafer Acceptance Test (WAT)	—	5007	X	—	
Rad Vertification If Required	4 Chips Per Wafer	1019	X	—	
Assembly 100% Non-Dest Bond Pull	—	2023	X	—	
Pre-Cap Visual	Condition A	2010	X	—	
	Condition B	2010	—	X	
Preconditioning Stabilization Bake	Cond C	1008	X	X	
Temperature Cycle	Cond C	1010	X	X	
Centrifuge	Cond E, Y1 Only	2001	X	X	
Fine Leak	Cond B	1014	—	X	
Gross Leak	Cond C	1014	—	X	
Particle Noise Test	Cond A	2020	X	—	
Test and Burn-In Serialize	—	—	X	—	
Initial Test	—	—	X	X	1
Static Burn-In 1 24 Hrs w/Deltas	135°C Inputs at V_{SS}, Outputs Open	1015 Condition A	X	—	1, 3
Static Burn-In 2 24 Hrs w/Deltas	135°C Inputs at V_{DD}, Outputs Open	1015 Condition B	X	—	1, 3, 5
Dynamic Burn-In 180 Hrs w/Deltas	135°C	1015 Condition D	X	—	1, 2, 3, 5
Static Burn-in 2 120 Hrs	135°C Inputs at V_{DD}, Outputs Open	1015 Condition B	—	X	1, 2, 4, 5
Final Elec DC + 25°C	—	—	X	X	
Final Elec DC + 125°C	—	—	X	X	
Final Elec DC -55°C	—	—	X	X	
Final Elec AC + 25°C	—	—	X	X	
Fine Leak	Cond B	1014	X	—	
Gross Leak	Cond C	1014	X	—	
Final Inspection X-Ray Inspection	2 Views	2012	X	—	
Group A	—	—	X	X	
100% Visual Inspect	—	2009	X	X	

Notes:

1. See individual data bulletins for electrical testing of specific types.
2. Alt. time/temp regression used per method 1015.
3. PDA's for /MS is 5% cumulative for Static 1 and Static 2 and 5% for Dynamic. PDA for functional is 3%.
4. PDA for /3 and /3A is 5%, one reburn allowed at 3%.
5. PDA's are based on Group A subgroup 1.

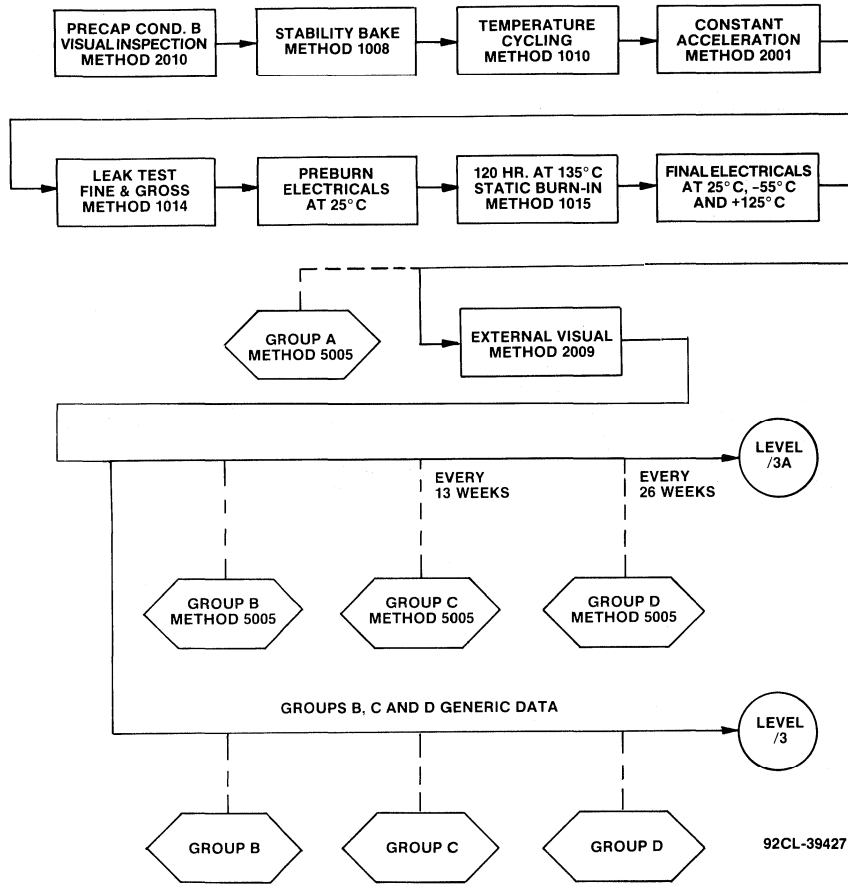
Screening Availability

Level /MS CMOS ICs Product Flow Chart



Screening Availability

Levels /3 and /3A CMOS ICs Product Flow Chart

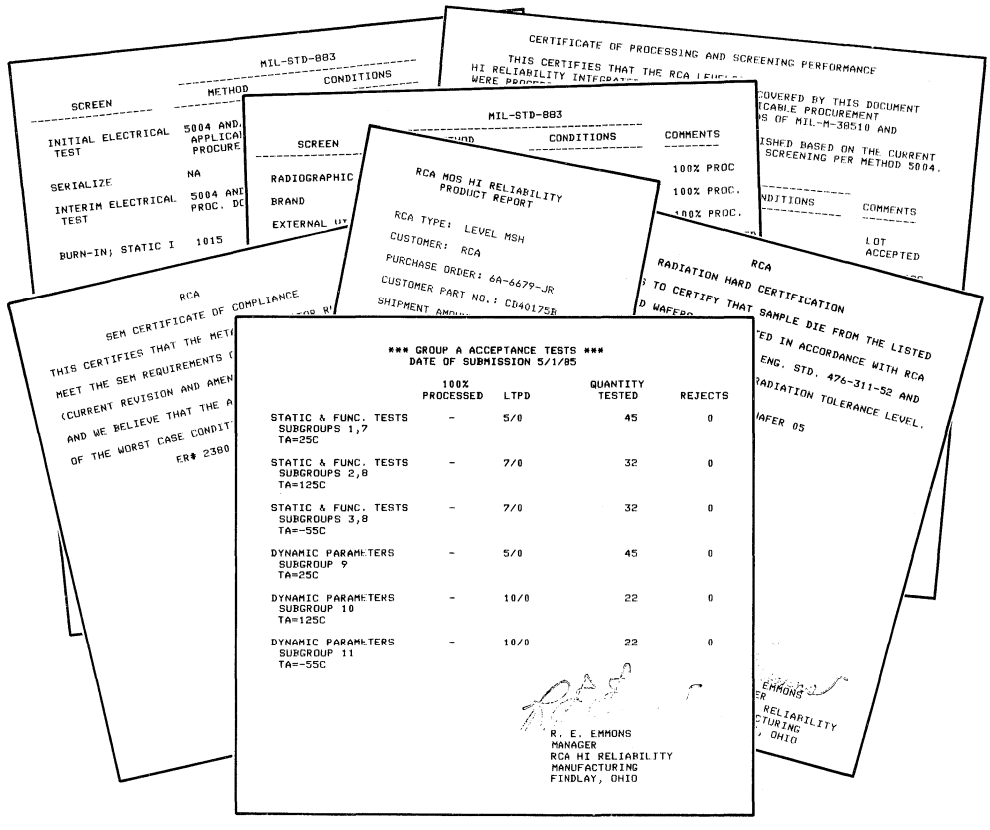


Data Supplied with Order for Packaged Devices

Product Screening Data	Levels
A. Certificate of Compliance* Signed by RCA Representative — Provides lot identity, customer order identity, lists and certifies tests, methods and conditions required	/MS, /3, /3A
B. Group A Subgroup — Test Summary Attributes Data	/MS
C. Variables Data, Pre Burn-In and Post Burn-In with Deltas	/MS
D. Radiographic Inspection Film and Film Inspection Record (no penatrameter images supplied)	/MS /MS
E. SEM Inspection Certificate of Compliance Includes lot identification and 3 photos	/MS
F. Certificate of Compliance for Radiation Assurance Testing	/MSR, /MSH

*RCA provides written certification for each class of product to verify that specified tests and inspections (e.g., SEM, Visual 2010, radiation, or special parameter tests) have been performed to special custom requirements or to Class S or B of MIL-STD-883 specifications.

Certificates of Compliance



RCA

SEM CERTIFICATE OF COMPLIANCE

THIS CERTIFIES THAT THE MET
MEET THE SEM REQUIREMENTS
(CURRENT REVISION AND AMEN
AND WE BELIEVE THAT THE A
OF THE WORST CASE CONDIT
ER# 2380

MIL-STD-883

SCREEN	METHOD	CONDITIONS
INITIAL ELECTRICAL TEST	5004 AND, APPLICA PROCURE	
SERIALIZE	NA	
INTERIM ELECTRICAL TEST	5004 ANI PROC. DC	
BURN-IN; STATIC I	1015	

MIL-STD-883

SCREEN	CONDITIONS	COMMENTS
RADIOGRAPHIC		100% PROC
BRAND		100% PROC.
EXTERNAL		100% PROC.

RCA MOS HI RELIABILITY
PRODUCT REPORT

RCA TYPE: LEVEL MSH
CUSTOMER: RCA
PURCHASE ORDER: 6A-6679-JR
CUSTOMER PART NO.: CD40175B
SHIPMENT AMOU

*** GROUP A ACCEPTANCE TESTS ***
DATE OF SUBMISSION 5/1/85

	100% PROCESSED	LTPD	QUANTITY TESTED	REJECTS
STATIC & FUNC. TESTS SUBGROUPS 1,7 TA=25C	-	5/0	45	0
STATIC & FUNC. TESTS SUBGROUPS 2,8 TA=125C	-	7/0	32	0
STATIC & FUNC. TESTS SUBGROUPS 3,8 TA=-55C	-	7/0	32	0
DYNAMIC PARAMETERS SUBGROUP 9 TA=25C	-	5/0	45	0
DYNAMIC PARAMETERS SUBGROUP 10 TA=125C	-	10/0	22	0
DYNAMIC PARAMETERS SUBGROUP 11 TA=-55C	-	10/0	22	0

R. E. EMMONS
MANAGER
RCA HI RELIABILITY
MANUFACTURING
FINDLAY, OHIO

CERTIFICATE OF PROCESSING AND SCREENING PERFORMANCE

THIS CERTIFIES THAT THE RCA LEVEL
HI RELIABILITY INTEGRATED
WERE PROCESSED

COVERED BY THIS DOCUMENT
ICABLE PROCUREMENT
S OF MIL-M-38510 AND

ISHED BASED ON THE CURRENT
SCREENING PER METHOD 5004.

CONDITIONS	COMMENTS
	LOT ACCEPTED

RCA

RADIATION HARD CERTIFICATION

TO CERTIFY THAT SAMPLE DIE FROM THE LISTED
D WAFER
ED IN ACCORDANCE WITH RCA
ENG. STD. 476-311-52 AND
RADIATION TOLERANCE LEVEL.
WAFER 05

EMMONS
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RELIABILITY
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, OHIO

Data Supplied with Order for Packaged Devices

QUALITY CONFORMANCE DATA
(Reference MIL-STD-883, Method 5005)
Group B, C and D Data

Attributes data summary of the latest Group B, C and/or D subgroups, when available, can be ordered at extra charge.

Special Group B, C and/or D quality conformance tests on samples from the specific lot of parts ordered will be considered on a custom basis only.

Source Inspections

Both customer and government (DCAS) source-inspection requirements are honored as appropriate. Source inspections for Class B integrated circuits are usually required prior to shipment or to verify Group A conformance tests. Source inspections for Class S parts are usually imposed at precap inspections and for verification of Group A tests.

Specific requirements for source inspections must be understood and mutually agreed upon by the customer and RCA prior to the placement of orders so that these requirements can be incorporated into the RCA internal specifications that are used to control the order.

Device Classification

The table below shows the levels of device leakage as SSI, MSI-1, and MSI-2. In order to determine the limits which apply to a specific device type, consult the dc electrical parameters chart which provides a breakdown of all high-reliability CD4000B-series devices by complexity classification.

Classification According to Circuit Complexity

Gates/ Inverters (SSI)	Buffers/Flip-Flops/ Latches/Multi-Level Gates (MSI-1)	Complex Logic (MSI-2)		
CD4000B	CD4009UB*	CD4006B	CD4060B	CD4555B
CD4000UB	CD4010B*	CD4008B	CD4063B	CD4556B
CD4001B	CD4013B	CD4014B	CD4067B*	CD4585B
CD4001UB	CD4019B	CD4015B	CD4076B	CD4724B
CD4002B	CD4027B	CD4017B	CD4089B	CD40100B
CD4002UB	CD4030B	CD4018B	CD4094B	CD40101B
CD4007UB	CD4041UB*	CD4020B	CD4097B*	CD40102B
CD4011B	CD4042B	CD4021B	CD4099B	CD40103B
CD4011UB	CD4043B	CD4022B	CD4508B	CD40104B
CD4012B	CD4044B	CD4024B	CD4510B	CD40105B
CD4012UB	CD4047B	CD4026B	CD4511B*	CD40108B
CD4016B*	CD4049UB*	CD4028B	CD4512B	CD40110B*
CD4023B	CD4050B*	CD4029B	CD4514B	CD40116*
CD4023UB	CD4070B	CD4031B*	CD4515B	CD40160B
CD4025B	CD4077B	CD4032B	CD4516B	CD40161B
CD4025UB	CD4085B	CD4033B	CD4517B	CD40162B
CD4048B	CD4086B	CD4034B	CD4518B	CD40163B
CD4066B*	CD4093B*	CD4035B	CD4520B	CD40181B
CD4068B	CD4095B	CD4038B	CD4527B	CD40182B
CD4069UB	CD4096B	CD4040B	CD4532B	CD40192B
CD4071B	CD4098B	CD4045B*	CD4536B	CD40193B
CD4072B	CD4502B*	CD4046B*	CD4538B	CD40194B
CD4073B	CD4503B*	CD4051B*	CD4541B*	CD40208B
CD4075B	CD40106B*	CD4052B*	CD4543B*	
CD4078B	CD40107B*	CD4053B*		
CD4081B	CD40109B*	CD4054B*		
CD4082B	CD40147B	CD4055B*		
	CD40174B	CD4056B*		
	CD40175B			
	CD40257B			

*Indicates type for which, because of design requirements, one or more static characteristics differ from the standardized data. These differences are defined in separate data charts on these types.

Ratings and Characteristics

Absolute Maximum Ratings

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100° C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... -55 to +125° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

Recommended Operating Conditions

For maximum realiability, nominal operating conditions should be selected so that operation is always within the following ranges:

Characteristic	Limits		Units
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

Delta Parameters

For the /MS level devices, certain parameters are data-logged and deltas are calculated from pre to post burn-in. These parameters are shown below.

Guide to Burn-In Delta Limits for Level /MS High-Voltage CD4000B-Series CMOS ICs

Critical Parameters	Symbols	Test Conditions V_O (V)	Test Conditions V_{IN} (V)	Test Conditions V_{DD} (V)	Delta (Δ) Limits
Quiescent Device Current					
Gates	I_{DD}	—	0,20	20	± 0.1 μA
MSI-1 Types	I_{DD}	—	0,20	20	± 0.2 μA
MSI-2 Types	I_{DD}	—	0,20	20	± 1.0 μA
Output Low (Sink) Current	I_{OL}	0.4	0,5	5	± 20% of initial value
Output High (Source) Current	I_{OH}	4.6	0,5	5	± 20% of initial value
Types with R_{ON} limits instead of I_{OL} and I_{OH}	R_{ON}	—	—	10V	± 20% of initial value

Ratings and Characteristics

Standard "B" Series Devices

The following table contains electrical characteristics for all CD4000B-series standard output CMOS Devices. The actual parameters which are 100% tested for final electrical and group A tests are indicated by a black dot next to the applicable parameters. All other parameters are applicable to RCA high-reliability devices but are warranteed and not tested.

Standard DC Electrical Characteristics

Static Electrical Parameters	Conditions			Limits at Indicated Temperatures						Units	Notes
				-55° C		+25° C		+125° C			
	V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	Min.	Max.		
Functional Test•	—	0,20	20	—	—	—	—	—	—		
Quiescent device current I_{DD} SSI	—	0,5	5	—	0.25	—	0.25	—	7.5	μA	1
	—	0,10	10	—	0.5	—	0.5	—	15		
	—	0,15	15	—	1	—	1	—	30		
	—	0,20	20	—	5•	—	5•	—	150•		
MSI-1	—	0,5	5	—	1	—	1	—	30	μA	1, 2
	—	0,10	10	—	2	—	2	—	60		
	—	0,15	15	—	4	—	4	—	120		
	—	0,20	20	—	20•	—	20•	—	600•		
MSI-2	—	0,5	5	—	5	—	5	—	150	μA	1
	—	0,10	10	—	10	—	10	—	300		
	—	0,15	15	—	20	—	20	—	600		
	—	0,20	20	—	100•	—	100•	—	3000•		
Output low drive current I_{OL} min.	0.4	0,5	5	0.64	—	0.51•	—	0.36	—	mA	
	0.5	0,10	10	1.6	—	1.3•	—	0.9	—		
	1.5	0,15	15	4.2	—	3.4•	—	2.4	—		
Output high drive current I_{OH} min.	4.6	0,5	5	-0.64	—	-0.51•	—	-0.36	—	mA	
	2.5	0,5	5	-2.0	—	-1.6•	—	-1.15	—		
	9.5	0,10	10	-1.6	—	-1.3•	—	-0.9	—		
	13.5	0,15	15	-4.2	—	-3.4•	—	-2.4	—		
Output voltage low-level V_{OL} max.	—	0,5	5	—	0.05	—	0.05	—	0.05	V	
	—	0,10	10	—	0.05	—	0.05	—	0.05		
	—	0,15	15	—	0.05•	—	0.05•	—	0.05•		
Output voltage high-level V_{OH} min.	—	0,5	5	4.95	—	4.95	—	4.95	—	V	
	—	0,10	10	9.95	—	9.95	—	9.95	—		
	—	0,15	15	14.95•	—	14.95•	—	14.95•	—		
Input low voltage V_{IL} max. Buffered (B)	4.5	—	5	—	1.5•	—	1.5•	—	1.5•	V	
	9	—	10	—	3	—	3	—	3		
	13.5	—	15	—	4•	—	4•	—	4•		
Unbuffered (UB)	4.5	—	5	—	1•	—	1•	—	1•	V	
	9	—	10	—	2	—	2	—	2		
	13.5	—	15	—	2.5•	—	2.5•	—	2.5•		
Input high voltage V_{IH} min. Buffered (B)	0.5, 4.5	—	5	3.5•	—	3.5•	—	3.5•	—	V	
	1.9	—	10	7	—	7	—	7	—		
	1.5, 13.5	—	15	11•	—	11•	—	11•	—		
Unbuffered (UB)	0.5,4.5	—	5	4•	—	4•	—	4•	—	V	
	1,9	—	10	8	—	8	—	8	—		
	1.5, 13.5	—	15	12.5•	—	12.5•	—	12.5•	—		
Input current I_{IN}	—	0,20	20	—	± 0.1•	—	± 0.1•	—	± 1•	μA	1
3-state output leakage current I_{OUT}	0,20	0,20	20	—	± 0.4•	—	± 0.4•	—	± 12•	μA	1, 3

Limits with black dots (•) are tested 100%. Refer to "Total Lot Screening for RCA High-Reliability CD4000B -Series ICs" table for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTES:

1. At -55° C test is performed with V_{DD} of 18 volts.
2. CD4047B — Maximum dc supply voltage (V_{DD}) is 13 volts for radiation-hardened version of this type when operating with RC network.
3. For applicable devices only.

Ratings and Characteristics

Non-Standard "B" Series Devices

The table below indicates all devices which are considered to be non-standard. Non-standard devices are types which exhibit non-standard outputs or special parameters such as bilateral switches (CD4066B), multiplexers (CD4051B), special sink or source currents (CD4049UB, CD4050B), and open-drain buffer/drivers (CD40107B). This table shows the 100% electrical tests that are performed on these specialized devices. These tests take the place of corresponding parameters in the Standard Electrical Characteristics table. For the types listed with R_{ON} tests, drive current and output voltage tests should be deleted from the Standard Electrical Characteristics table.

Non-Standard DC Electrical Characteristics

Static Electrical Parameters	Conditions			Limits at Indicated Temperatures				Units
				-55° C	+25° C		+125° C	
	V_O	V_{IN}	V_{DD}	Min./Max.	Min.	Max.	Min./Max.	
CD4009UB, CD401OB								
Output low drive current I_{OL} min.	0.4	0,5	4.5	3.2	2.6	—	1.8	mA
	0.4	0,5	5	3.75	3•	—	2.1	
	0.5	0,10	10	10.0	8•	—	5.6	
	1.5	0,15	15	30.0	24•	—	16.0	
Output high drive current I_{OH} min.	4.6	0,5	5	-0.25	-0.2•	—	-0.15	mA
	2.5	0,5	5	-1.0	-0.8•	—	-0.58	
	9.5	0,10	10	-0.55	-0.45•	—	-0.33	
	13.5	0,15	15	-1.65	-1.5•	—	-1.1	
CD4016B								
Control Input voltage low V_{IL} max.	$V_{IS}=V_{SS}$, $V_{OS}=V_{DD}$		5	0.9•	—	0.7•	0.4•	V
	$V_{IS}=V_{DD}$, $V_{OS}=V_{SS}$		10	0.9	—	0.7	0.4	
	$\lvert I_{IS} \rvert < 10\mu A$		15	0.9•	—	0.7•	0.4•	
Control Input voltage high V_{IH} min.	—		5	3.5•	3.5•	—	3.5•	V
			10	7.0	7.0	—	7.0	
			15	11.0•	11.0•	—	11.0•	
On-state resistance R_{ON} max. R_L = 10k returned to V_{DD}-V_{SS}/2	$V_{IS}=V_{DD}$ or V_{SS}		10	600•	—	660•	960•	ohms
	V_{IS} = 4.75 or 5.75		10	1870•	—	2000•	2600•	
	$V_{IS}=V_{DD}$ or V_{SS}		15	360•	—	400•	600•	
	V_{IS} = 7.25 or 7.75		15	775•	—	850•	1230•	
CD4031B								
Output low drive current I_{OL} min. Q	0.4	0,5	5	2.56	2.04•	—	1.44	mA
	0.5	0,10	10	6.4	5.2•	—	3.6	
	1.5	0,15	15	16.8	13.6•	—	9.6	
$\overline{Q}$, Q', CLd	0.4	0,5	5	0.64	0.51•	—	0.36	mA
	0.5	0,10	10	1.6	1.3•	—	0.9	
	1.5	0,15	15	4.2	3.4•	—	2.4	
Output high drive current I_{OH} min.	4.6	0,5	5	-0.64	-0.51•	—	-0.36	mA
	2.5	0,5	5	-2.0	-1.6•	—	-1.15	
	9.5	0,10	10	-1.6	-1.3•	—	-0.9	
Q, $\overline{Q}$, Q', CLd	13.5	0,15	15	-4.2	-3.4•	—	-2.4	
CD4041UB								
Output low drive current I_{OL} min.	0.4	0,5	5	2.1	1.6•	—	1.2	mA
	0.5	0,10	10	6.25	5•	—	3.5	
	1.5	0,15	15	24	19•	—	13	
Output high drive current I_{OH} min.	4.6	0,5	5	-2.1	-1.6•	—	-1.2	mA
	2.5	0,5	5	-8.4	-6.4•	—	-4.6	
	9.5	0,10	10	-6.25	-5.0•	—	-3.5	
	13.5	0,15	15	-24	-19•	—	-13	

Limits with black dots (•) are tested 100%.

Ratings and Characteristics

Non-Standard DC Electrical Characteristics

Static Electrical Parameters	Conditions			Limits at Indicated Temperatures				Units
				-55° C	+25° C		+125° C	
	V_O	V_{IN}	V_{DD}	Min./Max.	Min.	Max.	Min./Max.	
CD4045B								
Output low drive current I_{OL} min.	0.4	0,5	5	4.5	3.6•	—	2.5	mA
	0.5	0,10	10	11.2	9.1•	—	6.3	
	1.5	0,15	15	29.4	23.8•	—	16.8	
Output high drive current I_{OH} min.	4.6	0,5	5	-4.5	-3.6•	—	-2.5	mA
	9.5	0,10	10	-11.2	-9.1•	—	-6.3	
	13.5	0,15	15	-29.4	-23.8•	—	-16.8	
Pin 15 output low and high current I_{OL}, I_{OH}	0.4, 4.6	0,5	5	—	± 0.1•	—	—	mA
	0.5, 9.5	0,10	10	—	± 0.2•	—	—	
	1.5, 13.5	0,15	15	—	± 0.5•	—	—	
CD4046B								
Zener diode voltage (V_Z)	I_Z = 50 μA			—	4.45•	6.5•	—	V
Quiescent leakage phase comparator pin 14 open pin 5 = V_{DD}	—	0,5	5	0.2	—	0.2	—	mA
	—	0,10	10	1.0	—	1.0	—	
	—	0,15	15	1.5	—	1.5	—	
	—	0,20	20	4.0•	—	4.0•	—	
Quiescent leakage phase comparator pin 14 = V_{SS} or V_{DD} pin 5 = V_{DD}	—	0,5	5	20	—	20	—	μA
	—	0,10	10	40	—	40	—	
	—	0,15	15	80	—	80	—	
	—	0,20	20	160•	—	160•	—	
CD4049UB, CD4050B								
Output low drive current I_{OL} min.	0.4	0,5	4.5	3.3	2.6•	—	1.8	mA
	0.4	0,5	5	4.0	3.2•	—	2.4	
	0.5	0,10	10	10	8.0•	—	5.6	
	1.5	0,15	15	26	24•	—	18	
Output high drive current I_{OH} min.	4.6	0,5	5	-0.81	-0.8•	—	-0.48	mA
	2.5	0,5	5	-2.6	-3.2•	—	-1.55	
	9.5	0,10	10	-2.0	-1.8•	—	-1.18	
	13.5	0,15	15	-5.2	-6.0•	—	-3.1	
CD4051B, CD4052B, CD4053B, CD4067B, CD4097B								
On-state resistance R_{ON} max.	R_L = 10k returned to V_{DD}-V_{SS}/2 V_{IS} = V_{SS} to V_{DD}		5	800•	—	1050•	1300•	ohms
			10	310•	—	400•	500•	
			15	200•	—	240•	320•	
Input voltage low V_{IL} max.	V_{EE} = V_{SS} R_L = 1k to V_{SS} $\lvert I_{IS}\rvert$ < 2μA		5	1.5•	—	1.5•	1.5•	Volts
			10	3.0	—	3.0	3.0	
			15	4.0•	—	4.0•	4.0•	
Input voltage high V_{IH} min.	V_{EE} = V_{SS} R_L = 1k to V_{SS} $\lvert I_{IS}\rvert$ < 2μA		5	3.5•	3.5•	—	3.5•	Volts
			10	7.0	7.0	—	7.0	
			15	11.0•	11.0•	—	11.0•	
Off channel leakage current Any channel off max.	V_{SS}-V	V_{EE}-V						nA
All channels (common out/in) off max.	0	0	18	± 100	—	± 100	± 1000	
CD4054B, CD4055B, CD4056B								
	V_{EE}	V_{SS}						
Output low (sink) current I_{OL}	-5	0	-4.5	—	5	0.98	0.8•	—	0.55	mA
	0	0	0.5	—	10	0.98	0.8•	—	0.55	
	0	0	1.5	—	15	3.6	2.9•	—	2	
Output high (source) current I_{OH}	-5	0	4.5	—	5	-0.6	-0.45•	—	-0.3	mA
	0	0	9.5	—	10	-0.6	-0.45•	—	-0.3	
	0	0	13.5	—	15	-1.9	-1.5•	—	-1.1	

Limits with black dots (•) are tested 100%.

Ratings and Characteristics

Non-Standard DC Electrical Characteristics

Static Electrical Parameters	Conditions			Limits at Indicated Temperatures				Units
				-55° C	+25° C		+125° C	
	V_O	V_{IN}	V_{DD}	Min./Max.	Min.	Max.	Min./Max.	
CD4066B								
On-state resistance R_{ON} max.	R_L = 10k returned to V_{DD}-V_{SS}/2 V_{IS} = V_{SS} to V_{DD}		5	800•	—	1050•	1300•	ohms
			10	310•	—	400•	550•	
			15	200•	—	240•	320•	
Control Input Voltage Low V_{ILC} max.	V_{IS} = V_{SS}, V_{OS} = V_{DD} V_{IS} = V_{DD}, V_{OS} = V_{SS} $\lvert I_{IS}\rvert < 10\mu A$		5	1.0•	—	1.0•	1.0•	Volts
			10	2.0	—	2.0	2.0	
			15	2.0•	—	2.0•	2.0•	
Control Input Voltage High V_{IHC} min.	—		5	3.5•	3.5•	—	3.5•	Volts
			10	7.0	7.0	—	7.0	
			15	11.0•	11.0•	—	11.0•	
Input output leakage current (switch off) Effective off resistance V_C = V_{SS}	0	0	18	± 100	—	± 100	± 1000	nA
CD4093B								
Positive Trigger Threshold Voltage V_P min.	—	a	5	2.2•	2.2•	—	2.2•	V
	—	a	10	4.6	4.6	—	4.6	
	—	a	15	6.8•	6.8•	—	6.8•	
	—	b	5	2.6•	2.6•	—	2.6•	
	—	b	10	5.6	5.6	—	5.6	
	—	b	15	6.3	6.3	—	6.3	
V_P max.	—	a	5	3.6•	—	3.6•	3.6•	V
	—	a	10	7.1	—	7.1	7.1	
	—	a	15	10.8•	—	10.8•	10.8•	
	—	b	5	4•	—	4•	4•	
	—	b	10	8.2	—	8.2	8.2	
	—	b	15	12.7	—	12.7	12.7	
Negative Trigger Threshold Voltage V_N min.	—	a	5	0.9•	0.9•	—	0.9•	V
	—	a	10	2.5	2.5	—	2.5	
	—	a	15	4•	4•	—	4•	
	—	b	5	1.4•	1.4•	—	1.4•	
	—	b	10	3.4	3.4	—	3.4	
	—	b	15	4.8	4.8	—	4.8	
V_N	—	a	5	2.8•	—	2.8•	2.8•	V
	—	a	10	5.2	—	5.2	5.2	
	—	a	15	7.4•	—	7.4•	7.4•	
	—	b	5	3.2•	—	3.2•	3.2•	
	—	b	10	6.6	—	6.6	6.6	
	—	b	15	9.6	—	9.6	9.6	
Hysteresis Voltage V_H min.	—	a	5	0.3•	0.3•	—	0.3•	V
	—	a	10	1.2	1.2	—	1.2	
	—	a	15	1.6•	1.6•	—	1.6•	
	—	b	5	0.3•	0.3•	—	0.3•	
	—	b	10	1.2	1.2	—	1.2	
	—	b	15	1.6	1.6	—	1.6	
V_H max.	—	a	5	1.6•	—	1.6•	1.6•	V
	—	a	10	3.4	—	3.4	3.4	
	—	a	15	5•	—	5•	5•	
	—	b	5	1.6•	—	1.6•	1.6•	
	—	b	10	3.4	—	3.4	3.4	
	—	b	15	5	—	5	5	

*a Input on terminals 1, 5, 8, 12, or 2, 6, 9, 13; other inputs to V_{DD}.
b Input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to V_{DD}.

Limits with black dots (•) are tested 100%.

Ratings and Characteristics

Non-Standard DC Electrical Characteristics

Characteristic	Conditions			Limits at Indicated Temperatures				Units
				-55° C	+25° C		+125° C	
	V_O	V_{IN}	V_{DD}	Min./Max.	Min.	Max.	Min./Max.	
CD4502B								
Output low drive current I_{OL} min.	0.4	0,5	5	3.84	3.06•	—	2.16	mA
	0.5	0,10	10	9.6	7.8•	—	5.4	
	1.5	0,15	15	25.2	20.4•	—	14.4	
CD4503B								
Output low drive current I_{OL} min.	0.4	0	5	2.6	2.1•	—	1.3	mA
	0.5	0	10	6.5	5.5•	—	3.8	
	1.5	0	15	19.2	16.1•	—	11.2	
Output high drive current I_{OH} min.	4.6	5	5	-1.2	-1.02•	—	-0.7	mA
	2.5	5	5	-5.8	-4.8•	—	-3.0	
	9.5	10	10	-3.1	-2.6•	—	-1.8	
	13.5	15	15	-8.2	-6.8•	—	-4.8	
CD4511B								
Output Voltage High-Level V_{OH} min.	—	0.5	5	4	4.1	—	4.2	V
	—	0.10	10	9	9.1	—	9.2	
	—	0.15	15	14•	14.1•	—	14.2•	
Output Drive Voltage High Level V_{OH} min. — I_{OH} (mA) 0	—	—	5	4.0	4.10	—	4.20	V
5	—	—	5	—	—	—	—	
10	—	—	5	3.80	3.90	—	3.90	
15	—	—	5	—	—	—	3.50	
20	—	—	5	3.55	3.40•	—	—	
25	—	—	5	3.40	3.10	—	—	
0	—	—	10	9.0	9.10	—	9.20	V
5	—	—	10	—	—	—	—	
10	—	—	10	8.85	9.0	—	9.0	
15	—	—	10	—	—	—	—	
20	—	—	10	8.70	8.60•	—	8.40	
25	—	—	10	8.60	8.30	—	—	
0	—	—	15	14.0	14.10	—	14.20	V
5	—	—	15	—	—	—	—	
10	—	—	15	13.90	14.0	—	14.0	
15	—	—	15	—	—	—	—	
20	—	—	15	13.75	13.70•	—	13.50	
25	—	—	15	13.65	13.50	—	—	
CD4541B								
Output high drive current I_{OH} min.	4.6	0,5	5	-1.9	-1.55•	—	-1.08	mA
	2.5	0,5	5	-6.2	-5.0•	—	-3.0	
	9.5	0,10	10	-5.0	-4.0•	—	-2.8	
	13.5	0,15	15	-12.6	-10.0•	—	-7.2	
Output low drive current I_{OL} min.	0.4	0,5	5	1.9	1.55•	—	1.08	mA
	0.5	0,10	10	5.0	4.0•	—	2.8	
	1.5	0,15	15	12.6	10.0•	—	7.2	
CD4543B								
Output high drive current I_{OH} min.	4.6	0,5	5	-0.46	-0.37•	—	0.26	mA
	2.5	0,5	5	-1.6	-1.3•	—	-0.9	
	9.5	0,10	10	-0.98	-0.8•	—	-0.55	
	13.5	0,15	15	-3.33	-2.7•	—	-1.9	
CD40106B								
Positive trigger threshold voltage V_P min.	—	—	5	2.2•	2.2•	—	2.2•	V
	—	—	10	4.6•	4.6•	—	4.6•	
	—	—	15	6.8•	6.8•	—	6.8•	
V_P max.	—	—	5	3.6•	—	3.6•	3.6•	V
	—	—	10	7.1•	—	7.1•	7.1•	
	—	—	15	10.8•	—	10.8•	10.8•	

Limits with black dots (•) are tested 100%.

Ratings and Characteristics

Non-Standard DC Electrical Characteristics

Static Electrical Parameters	Conditions			Limits at Indicated Temperatures				Units
				-55° C	+25° C		+125° C	
	V_O	V_{IN}	V_{DD}	Min./Max.	Min.	Max.	Min./Max.	
CD40106B (Cont'd)								
Negative Trigger Threshold Voltage V_N min.	—	—	5	0.9•	0.9•	—	0.9•	V
	—	—	10	2.5•	2.5•	—	2.5•	
	—	—	15	4•	4•	—	4•	
V_N max.	—	—	5	2.8•	—	2.8•	2.8•	V
	—	—	10	5.2•	—	5.2•	5.2•	
	—	—	15	7.4•	—	7.4•	7.4•	
Hysteresis Voltage V_H min.	—	—	5	0.3•	0.3•	—	0.3•	V
	—	—	10	1.2•	1.2•	—	1.2•	
	—	—	15	1.6•	1.6•	—	1.6•	
V_H max.	—	—	5	1.6•	—	1.6•	1.6•	V
	—	—	10	3.4•	—	3.4•	3.4•	
	—	—	15	5•	—	5•	5•	
CD40107B								
Output low current I_{OL} min.	0.4	0,5	5	21	16•	—	12	mA
	1	0,5	5	44	34•	—	25	
	0.5	0,10	10	49	37•	—	28	
	1	0,10	10	89	68•	—	51	
	0.5	0,15	15	66	50•	—	38	
Output high current I_{OH} min.	NO INTERNAL PULL-UP DEVICE							
Input low voltage V_{IL} max. *	4.5	—	5	1.5•	—	1.5•	1.5•	V
	9	—	10	3	—	3	3	
	13.5	—	15	4•	—	4•	4•	
Input high voltage V_{IH} min. *	0.5, 4.5	—	5	3.5•	3.5•	—	3.5•	V
	1,9	—	10	7	7	—	7	
	1.5, 13.5	—	15	11•	11•	—	11•	
*Measured with external pull-up resistor, R_L = 10k ohm to V_{DD}								
CD40109B								
	V_O	V_{CC}	V_{DD}					
Input low voltage V_{IL} max.	1,9	5	10	1.5•	—	1.5•	1.5•	V
	1.5, 13.5	10	15	3•	—	3•	3•	
Input high voltage V_{IH} max.	1,9	5	10	3.5•	3.5•	—	3.5•	V
	1.5, 13.5	10	15	7•	7•	—	7•	
CD40110B								
	I_{OH}	V_{OH}	V_{IN}	V_{DD}				
Output Voltage Low-Level V_{OL} max.	—	—	0,5	5	0.05	—	0.05	0.05	V
	—	—	0,10	10	0.05	—	0.05	0.05	
	—	—	0,15	15	0.05•	—	0.05•	0.05•	
High-Level V_{OH} min.	—	—	0,5	5	—	—	—	—	V
	—	—	0,10	10	—	—	—	—	
	—	—	0,15	15	—	—	—	—	
7-Segment Outputs Output Drive Voltage, High V_{OH} min.	■	—	—	5	3.9	3.9	—	4	V
	-5	—	—	5	3.65	3.7	—	3.7	
	-10	—	—	5	3.55	3.65	—	3.65	
	-15	—	—	5	3.5	3.6	—	3.5	
	-20	—	—	5	3.45	3.45•	—	3.35	
	-25	—	—	5	3.4	3.4	—	3.3	
	■	—	—	10	8.75	8.75	—	8.85	V
	-5	—	—	10	8.45	8.55	—	8.55	
	-10	—	—	10	8.42	8.5	—	8.5	
	-15	—	—	10	8.4	8.47	—	8.47	
	-20	—	—	10	8.4	8.45•	—	8.40	
	-25	—	—	10	8.3	8.3	—	8.25	

Limits with black dots (•) are tested 100%. ■ 0 (10 μA)

Ratings and Characteristics

Non-Standard DC Electrical Characteristics

Static Electrical Parameters	Conditions				Limits at Indicated Temperatures				Units
					-55° C	+25° C		+125° C	
	I_{OH} (mA)	V_{OH}	V_{IN}	V_{DD}	Min./Max.	Min.	Max.	Min./Max.	
CD40110B (Cont'd.)									
7-Segment Outputs Output Drive Voltage, High V_{OH} min.	■	—	—	15	13.8	13.8	—	13.9	V
	-5	—	—	15	13.65	13.75	—	13.75	
	-10	—	—	15	13.6	13.72	—	13.72	
	-15	—	—	15	13.6	13.7	—	13.7	
	-20	—	—	15	13.6	13.65•	—	13.6	
	-25	—	—	15	13.3	13.3	—	13.25	
7-Segment Outputs Output Low (Sink) Current I_{OL} min.	—	0.4	0,5	5	1.28	1•	—	0.72	mA
	—	0.5	0,10	10	3.2	2.6•	—	1.8	
	—	1.5	0,15	15	8.4	6.8•	—	4.8	
CD40116									
Quiescent current	Enable = 1				6.5•	—	5•	5•	mA
From V_{DD} supply I_{DD} max.	Enable = 0				6.5•	—	5•	5•	
From V_{CC} supply I_{CC} max.					100•	—	100•	200•	μA
Data Flow — CMOS Inputs to TTL Outputs									
Input current (I_{IN})	V_{IN} = 0,12v				± 60•	—	± 60•	± 60•	μA
Output current									
I_{OH} min.	V_{OH} = 3V, V_{IL} = 2V				-7.5•	-6•	—	-4.2•	mA
I_{OL} min.	V_{OL} = 0.4V, V_{IH} = 10V				7.5•	6•	—	4.2•	mA
TTL 3-state leakage current I_{OUT} max.	Enable = 0				± 100•	—	± 100•	± 100•	μA
Data Flow — TTL Inputs to CMOS Outputs									
Input current	Any TTL Input								
I_{IL} max.	V_{IL} = 0 to 0.7V				-600•	—	-500•	-500•	μA
I_{IH} max.	V_{IH} = 2.3V				-450•	—	-350•	-350•	μA
Output current									
I_{OH} min.	V_{OH} = 11.5V, V_{IL} = 0.7V				-4.3•	-3.5•	—	-2.5•	mA
I_{OL} min.	V_{OL} = 0.5V, V_{IH} = 2.3V				4.3•	3.5•	—	2.5•	mA
CMOS 3-state output leakage current*	V_O = 0,12V; V_{IN} = 0,5V				± 60	—	± 60	± 60	μA
Enable and Disable Inputs									
I_{IL}	V_{IL} = 0 to 0.7 V				-600•	—	-500•	-500•	μA
Input current I_{IH}	V_{IH} = 2.3 (TTL)				-450•	—	-350•	-350•	μA
I_{IH}	V_{IH} = 12 V (CMOS)				60	—	60	60	μA

Limits with black dots (•) are tested 100%.

■ 0 (10 μA)

*CMOS 3-state output leakage test is functionally identical to CMOS-to-TTL input current tests.

Ratings and Characteristics

Dynamic Electrical Characteristics

The chart below lists all RCA high-reliability CD4000B-Series devices and shows which dynamic parameters are 100% tested at final electrical and Group A. In general RCA tests propogation delay, transition time, and maximum clock frequency at 5V where applicable. RCA guarantees all other dynamic parameters shown in the appropriate commercial data sheet. RCA High-reliability dynamic tests are performed on a one-input to one-output basis only.

AC Electrical Characteristics at 25° C

Type	Conditions* V_{DD} = 5V C_L = 50pF	Prop. Delay ns	Trans. Time ns	Max. Clock Input Freq. MHz
CD4000B	—	250	200	—
CD4000UB	—	120	200	—
CD4001B	—	250	200	—
CD4001UB	—	120	200	—
CD4002B	—	250	200	—
CD4002UB	—	120	200	—
CD4006B	—	400	200	2.5
CD4007UB	—	110	200	—
CD4008B	Sum In to Sum Out	800	200	—
	Carry In to Sum Out	740	—	—
	Sum In to Carry Out	400	—	—
	Carry In to Carry Out	200	—	—
CD4009UB	—	140*	350*	—
	—	60▲	70▲	—
CD4010B	—	200*	350*	—
	—	130▲	70▲	—
CD4011B	—	250	200	—
CD4011UB	—	120	200	—
CD4012B	—	250	200	—
CD4012UB	—	120	200	—
CD4013B	Clock to Q or $\overline{Q}$	300	200	3.5
	Set to Q or Reset to $\overline{Q}$	300*	—	—
	Set to $\overline{Q}$ or Reset to Q	400▲	—	—
CD4014B	—	320	200	3
CD4015B	Clock to Q	320	200	3
	Reset to Q	400▲	—	—
CD4016B	Sig. Input to Sig. Output	100	—	—
	Turn on	70	—	—
CD4017B	Clock to Out	650	200	2.5
	Clock to Carry Out	600	—	—
	Reset to Out	530	—	—
CD4018B	Clock to Q	400	200	3
	Preset/Reset to Q	550	—	—
CD4019B	—	300	200	—
CD4020B	Ø to Q1	360	200	3.5
	Qn to Qn + 1	200	—	—
	Reset to Q	280▲	—	—
CD4021B	—	320	200	3
CD4022B	Clock to Carry Out	600	200	2.5
	Clock to Decode Out	650	—	—
	Reset to Output	530	—	—
CD4023B	—	250	200	—
CD4023UB	—	120	200	—
CD4024B	Ø to Q1	360	200	3.5
	Qn to Qn + 1	200	—	—
	Reset to Q	280▲	—	—
CD4025B	—	250	200	—
CD4025UB	—	120	200	—

Type	Conditions* V_{DD} - 5V C_L - 50pF	Prop. Delay ns	Trans. Time ns	Max. Clock Input Freq. MHz
CD4026B	Clock to Carry Out	500	200	2.5
	Clock to Decode Out	700	—	—
	Reset to Carry Out	550*	—	—
	Reset to Decode Out	600	—	—
CD4027B	Clock to Q or $\overline{Q}$	300	200	3.5
	Set to Q or Reset to $\overline{Q}$	300*	—	—
	Set to $\overline{Q}$ or Reset to Q	400▲	—	—
	Preset Enable to Q	470	—	—
	Preset Enable to Carry Out	640	—	—
	Carry Input to Carry Out	340	—	—
CD4028B	—	350	200	—
CD4029B	Q Output	500	200	2
	Carry Output	560	—	—
CD4030B	—	280	200	—
CD4031	Clock to $\overline{Q}$	500	200	2
	Clock to Q	500*	—	—
	Clock to Q	380▲	—	—
	Clock to Q'	380	—	—
	$\overline{Clock}$ to CL_D	200	—	—
CD4032B	A, B, or Invert Inputs to Sum Outputs	520	200	2.5
	Clock Input to Sum Outputs	650	—	—
CD4033B	Clock to Carry Out	500	200	2.5
	Clock to Decode Out	700	—	—
	Reset to Carry Out	550*	—	—
	Reset to Decode Out	600	—	—
CD4034B	Parallel In to Parallel Out	700	200	2
	t_{PLZ}, t_{PHZ}	400	—	—
CD4035B	Clock to Q	500	200	2
	Reset to Q	460	—	—
CD4038B	A, B, or Invert Inputs to Sum Outputs	520	200	2.5
	Clock Input to Sum Outputs	650	—	—
CD4040B	Ø to Q1	360	200	3.5
	Qn to Qn + 1	200	—	—
	Reset to Q	280▲	—	—
CD4041UB	—	120	80	—
CD4042B	Data In to $\overline{Q}$	220	200	—
	Data In to Q	300	—	—
	Clock to Q	450	—	—
	Clock to $\overline{Q}$	500	—	—
CD4043B, 44B	Set or Reset to Q	300	200	—
	Enable to Q — t_{PHZ}, t_{PZH}	230	—	—
	Enable to Q — t_{PLZ}, t_{PZL}	180	—	—
CD4045B	Ø to Y Output	5500	50	5
CD4046B	AC Coupled Signal Input Voltage Sensitivity (peak to peak) f_{IN} = 100 KHz Sine Wave	360 mV max.		

*t_{TLH} or t_{PLH}
▲t_{THL} or t_{PHL}

Ratings and Characteristics

AC Electrical Characteristics at 25° C

Type	Conditions* V_{DD} = 5V C_L = 50pF	Prop. Delay ns	Trans. Time ns	Max. Clock Input Freq. MHz
CD4047B	t_R to Q, $\overline{Q}$	1000	200	—
	Astable to Q, $\overline{Q}$	700	—	—
	Retrigger to Q, $\overline{Q}$	600	—	—
	Astable to Oscillator	400	—	—
	Reset to Q, $\overline{Q}$	500	—	—
CD4048B	Ka to Output	600	200	—
CD4049UB	—	120*	160*	—
	—	65▲	60▲	—
CD4050B	—	140*	160*	—
	—	110	60	—
CD4051B, 52B, 53B	Add to Signal Out	720	—	—
	Inhibit to Signal Out — Channel On	720	—	—
	Inhibit to Signal Out — Channel Off	450	—	—
CD4054B	V_{EE} = -5V	800	200	—
CD4055B, 56B	V_{EE} = -5V	1300	200	—
CD4056B	—	1300	200	—
CD4060B	Input Pulse Operation ϕ1 to Q4	740	200	3.5
	Qn to Qn + 1	200	—	—
	Reset Operation	360▲	—	—
CD4063B	Comparator Input to Output	1250	200	—
	Cascade Input to Output	1000	—	—
CD4066B	Signal Input to Signal Output R_L = 200k, V_C = V_{DD}, V_{SS} = GND, V_{IS} = square Wave about 5V & t_r, t_f = 20ns	40	—	—
	t_{pdc} t_{rc}, t_{fc} = 20ns, R_L = 1k & V_{IS} < 5V	70	—	—
CD4067B	Add or Inhib to Signal Out Channel On	650	—	—
	Signal In to Out	60	—	—
CD4068B	—	300	200	—
CD4069UB	—	110	200	—
CD4070B	—	280	200	—
CD4071B, 72B,73B, 75B	—	250	200	—
CD4076B	Clock to Q	600	200	—
CD4077B	—	280	200	—
CD4078B	—	300	200	3
CD4081B, 82B	—	250	200	—
CD4085B, 86B	Data	450▲	200	—
		620*	—	—
	Inhibit	300▲	—	—
		500*	—	—
CD4089B	Clock to Out	300	200	1.2
	Clear to Out	760	—	—
	Cascade to Out	180	—	—
CD4093B	—	380	200	—

*t_{TLH} or t_{PLH}
▲t_{THL} or t_{PHL}

Type	Conditions* V_{DD} = 5V C_L = 50pF	Prop. Delay ns	Trans. Time ns	Max. Clock Input Freq. MHz
CD4094B	Clock to Serial Out Q's	600	200	1.25
	Clock to Serial Out Q's	460	—	—
	Clock to Parallel Out	840	—	—
	Strobe to Parallel Out	580	—	—
	Out Enable to Parallel Out t_{PHZ}, t_{PZH}	280	—	—
	Out Enable to Parallel Out t_{PLZ}, t_{PZL}	200	—	—
CD4095B 96B	Clock to Output	500	200	3.5
	Set or Reset	300	—	—
CD4097B	Addr. or Inhib. to Sig. Out — Chan. On	650	—	—
	Signal In to Out	60	—	—
CD4098B	Trigger to Q, $\overline{Q}$	500	200	—
CD4099B	Data to Output	400	200	—
CD4502B	Data or Inhibit Delay Time	380*	200*	—
		270▲	120▲	—
	Disable Delay Time — t_{PHZ}	120	—	—
	Disable Delay Time — t_{PZH}	220	—	—
	Disable Delay Time — t_{PLZ}, t_{PZL}	250	—	—
CD4503B	—	150*	90*	—
	—	110▲	70▲	—
	t_{PHZ}, t_{PZH}	140	—	—
	t_{PLZ}, t_{PZL}	180	—	—
CD4508B	Strobe In to Data Out	260	200	—
CD4510B	Clock to Q Output	400	200	2
	Preset or Reset to Q	420	—	—
	Clock to Carry Out	480	—	—
	Carry In to Carry Out	250	—	—
	Preset or Reset to Carry Out	640	—	—
CD4511B	Data to Output	1040▲	310▲	—
		1320*	80*	—
CD4512B	Inhibit to Output	280	200	—
	"A" Select to Output	400	—	—
	Data to Output	360	—	—
	t_{PHZ}, t_{PZH}	120	—	—
CD4514B, 15B	Strobe or Data	970	200	—
	Inhibit	500	—	—
CD4516B	Clock to Q Output	400	200	2
	Preset or Reset to Q	420	—	—
	Clock to Carry Out	480	—	—
	Carry In to Carry Out	250	—	—
	Preset or Reset to Carry Out	640	—	—
CD4517B	Clock to Q16	400	200	3
CD4518B, 20B	Clock to Output	560	200	1.5
	Reset to Output	650	—	—
CD4527B	Clock to Out	300	200	1.2
	Clear to Out	760	—	—
	Cascade to Out	180	—	—
CD4532B	E_I to E_O, E_I to Gs	220	200	—
	Dn to Qm	440	—	—
	Dn to Gs, E_1 to Qm	340	—	—

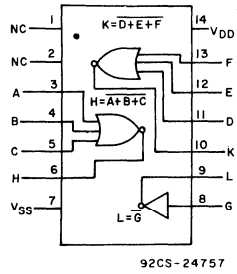
AC Electrical Characteristics at 25° C

Type	Conditions* V_{DD} = 5V C_L = 50pF	Prop. Delay ns	Trans. Time ns	Max. Clock Input Freq. MHz
CD4536B	Clock to Q1 8 Bypass High	2000	200	0.5
	Clock to Q1 8 Bypass Low	5000	—	—
	Clock to Q16	8000	—	—
	Reset to Qn	6000▲	—	—
CD4538B	Trigger to Q, $\overline{Q}$	600	200	—
	Reset to Q or $\overline{Q}$	500	—	—
CD4541B	Clock to Q (2^2)	1050	200▲	1.5
	Clock to Q (2^{16})	1800	360*	—
CD4543B	—	1200▲	360	—
	—	1000*	—	—
CD4555B, 56B	Select to Any Output	440	200	—
	$\overline{\text{Enable}}$ to Any Output	400	—	—
CD4585B	Comparator Inputs to Outputs	600	200	—
	Cascade Inputs to Outputs	400	—	—
CD4724B	Data to Outputs	400	200	—
	Write Disable to Output	400	—	—
	Reset to Output	350▲	—	—
	Address to Output	450	—	—
CD40100B	—	720	200	1
CD40101B	Data-In to Output	700	200	—
	Inhibit-In to Output	280	—	—
CD40102B, 103B	Clock to Output	600	200	0.7
	Carry-in/Counter Enable to Output	400	—	—
	Asynchronous Preset Enable to Output	1300*	—	—
	$\overline{\text{Clear}}$ to Output	750▲	—	—
CD40104B	Clock to Q	440	200	3
	t_{PZH}, t_{PLZ}, t_{PZL}	160	—	—
	t_{PHZ}	90	—	—
CD40105B	Shift Out or Reset to Data Out Ready	370▲	200	1.5
	Shift In to Data in Ready	320▲	—	—
	3-State Control to Data Out t_{PZH}	280	—	—
	Ripple Thru Delay Input to Out t_{PLH}	4000*	—	—
CD40106B	—	280	200	—
CD40107B	R_L = 120 Ω	200	100	—
CD40108B	Clock or Write Enable to Q	720	200	1.5
	Read or Write Address to Q	600	—	—
	Disable Delay Time t_{PZH}, t_{PHZ}	200	—	—
	Disable Delay Time t_{PZL}, t_{PLZ}	260	—	—
CD40109B	Data Input to Output SHIFT MODE V_{CC} V_{DD} L-H 5V 10V	600▲	100	—
	L-H 5V 10V	260*	—	—
	H-L 10V 5V	500▲	200	—
	H-L 10V 5V	460*	—	—
	3-State Disable Delay R_L = 1KΩ SHIFT MODE V_{CC} V_{DD} t_{PHZ} L-H 5V 10V	120	—	—
	t_{PHZ} H-L 10V 5V	400	—	—
	t_{PLZ} L-H 5V 10V	740	—	—

Type	Conditions* V_{DD} = 5V C_L = 50pF	Prop. Delay ns	Trans. Time ns	Max. Clock Input Freq. MHz
CD40109B (cont'd.)	t_{PLZ} H-L 10V 5V	500	—	—
	t_{PZH} L-H 5V 10V	640	—	—
	t_{PZH} H-L 10V 5V	600	—	—
	t_{PZL} L-H 5V 10V	200	—	—
	t_{PZL} H-L 10V 5V	400	—	—
CD40110B	Clock to Carry or Borrow	600	—	1.0
CD40116B	Data In to Data Out — CMOS In, TTL Out	35	40	—
	Data In to Data Out — TTL In, CMOS Out	45	—	—
	Disable to TTL Out — t_{PHZ}, t_{PLZ}	45	—	—
	Disable to TTL Out — t_{PZH}, t_{PZL}	50	—	—
	Enable to CMOS Out — t_{PHZ}, t_{PLZ}	30	—	—
	Enable to CMOS Out — t_{PZH}, t_{PZL}	60	—	—
CD40147B	In-Phase Output	900	200	—
CD40160B, 161B, 162B, 163B	Clock to Q —	400	200	2
	Clock to C_{OUT} —	450	—	—
	T_E to C_{OUT} —	250	—	—
	Clear to Q (CD40160B & CD40161B only)	500	—	—
CD40174B	Clock to Output	300	200	3.5
	Clear to Output	200▲	—	—
CD40175B	Clock to Q Output	400	200	2.0
	Clear to Q Output	500▲	—	—
CD40181B	A or B to F (Logic Mode) A or B to G or P	— 800	— 200	— —
	A or B to F, Cn + 4, or A = B	1000	—	—
	Cn to F	640	—	—
	Cn to Cn + 4	400	—	—
CD40182B	P, G_{IN} to P, G_{OUT} and Carry Outs	400	200	—
	Cn to Carry Outs	480	—	—
CD40192B, 193B	Clock Up or Clock Down to Q, Reset Q	500	200	2
	$\overline{PE}$ to Q	400	—	—
	Clock Up to Carry, Clock Down to $\overline{\text{Borrow}}$	— 320	— —	— —
	Reset or $\overline{PE}$ to $\overline{\text{Borrow}}$ or $\overline{\text{Carry}}$	600	—	—
CD40194B	Clock to Q	440	200	3
	Reset to Q T_{PRHL}	460	—	—
CD40208B	Clock or Write Enable to Q	720	200	1.5
	Read or Write Address to Q	600	—	—
	3-State Disable Delay Time t_{PZH}, t_{PHZ}	200	—	—
	t_{PZL}, t_{PLZ}	260	—	—
CD40257B	Data Input to Output	300	200	—
	Select to Output	380	—	—
	Output Disable to Output	190	—	—

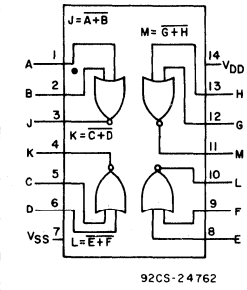
*t_{TLH} or t_{PLH}
▲t_{THL} or t_{PHL}

Functional Diagrams



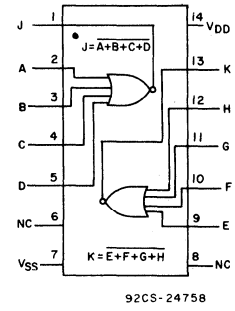
Dual 3-Input NOR Gate Plus Inverter

CD4000B (File No. 985)
CD4000UB (File No. 945)



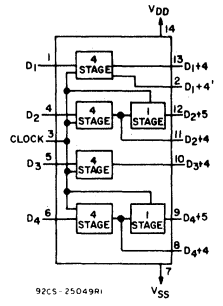
Quad 2-Input NOR Gate

CD4001B (File No. 985)
CD4001UB (File No. 945)



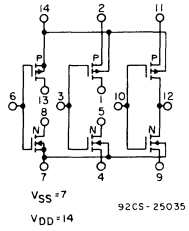
Dual 4-Input NOR Gate

CD4002B (File No. 985)
CD4002UB (File No. 945)



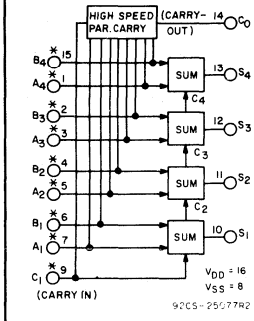
18-Stage Static Shift Register

CD4006B (File No. 1033)



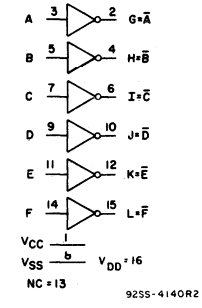
Dual Complementary Pair Plus Inverter

CD4007UB (File No. 977)



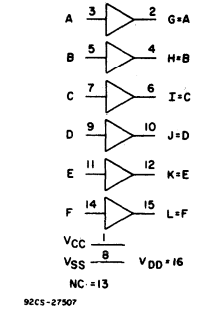
4-Bit Full Adder with Parallel Carry Out

CD4008B (File No. 951)



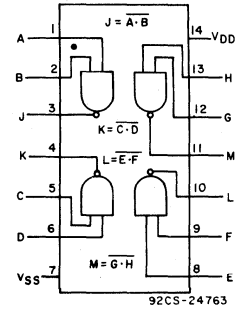
Hex Buffer/Converter Inverting Type

CD4009UB (File No. 940)



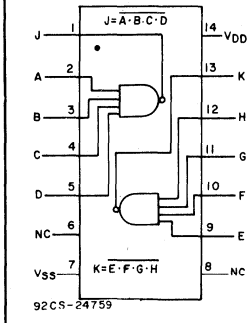
Hex Buffer/Converter Non-Inverting Type

CD4010B (File No. 940)



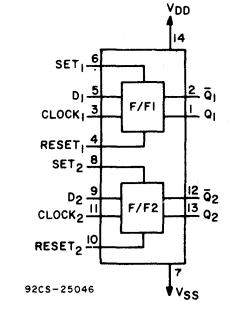
Quad 2-Input NAND Gate

CD4011B (File No. 986)
CD4011UB (File No. 947)



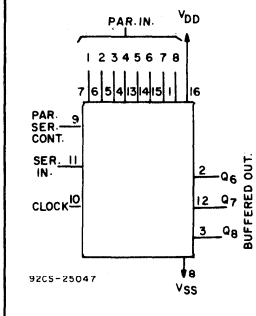
Dual 4-Input NAND Gate

CD4012B (File No. 986)
CD4012UB (File No. 947)



Dual "D" Flip-Flop with Set/Reset Capability

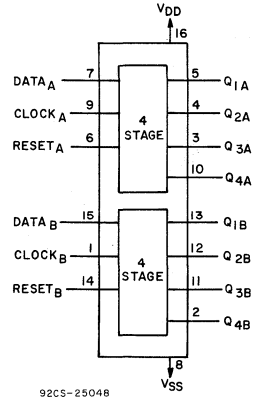
CD4013B (File No. 936)



8-State Synchronous Shift Register with Parallel or Serial Input/Serial Output

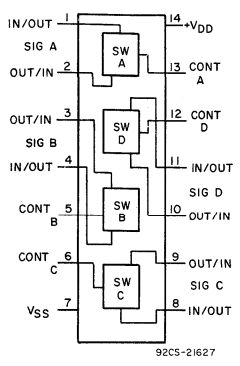
CD4014B (File No. 1043)

Functional Diagrams



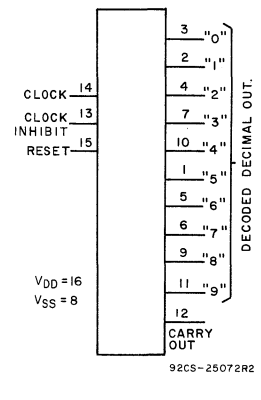
Dual 4-Stage Static Shift Register with Serial Input/Parallel Output

CD4015B (File No. 1024)



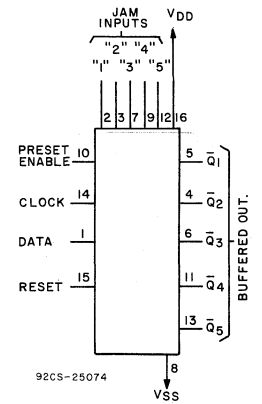
Quad Bilateral Switch

CD4016B (File No. 953)



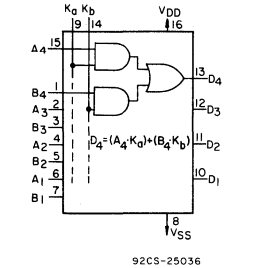
Decade Counter/Divider with 10 Decoded Decimal Outputs

CD4017B (File No. 1113)



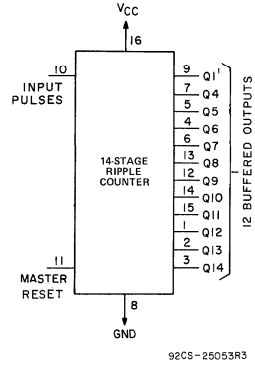
Presettable Divide-by-"N" Counter Fixed or Programmable

CD4018B (File No. 1034)



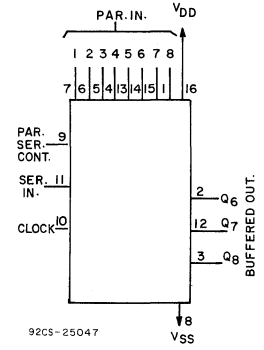
Quad AND/OR Select Gate

CD4019B (File No. 1045)



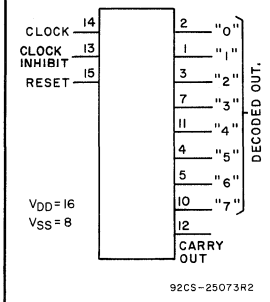
14-Stage Binary Ripple Counter

CD4020B (File No. 1063)



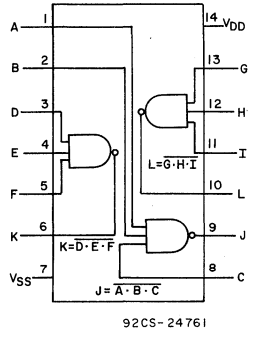
8-Stage Static Shift Register Asynchronous Parallel or Synchronous Serial Input/ Serial Output

CD4021B (File No. 1043)



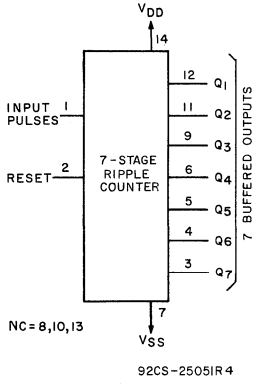
Divide-by-8 Counter/Divider with 8 Decoded Decimal Outputs

CD4022B (File No. 1113)



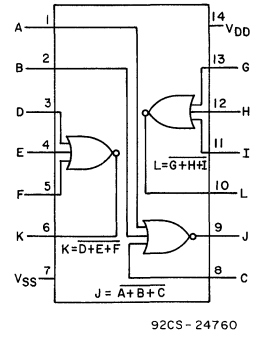
Triple 3-Input NAND Gate

CD4023B (File No. 986)
CD4023UB (File No. 947)



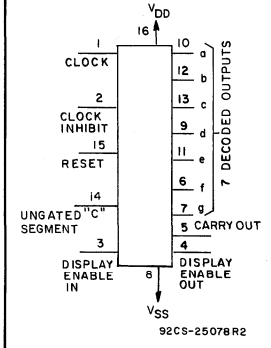
7-Stage Ripple-Carry Binary Counter/Divider

CD4024B (File No. 1063)



Triple 3-Input NOR Gate

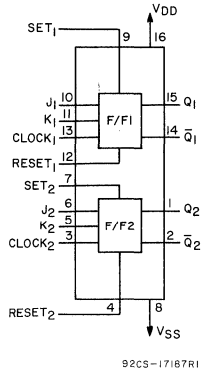
CD4025B (File No. 985)
CD4025UB (File No. 945)



Decade Counter/Divider with 7-Segment Display Output and Display Enable

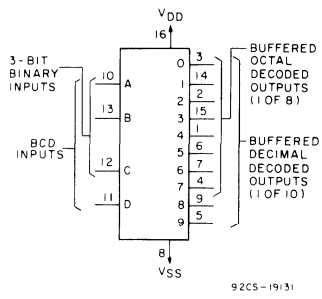
CD4026B (File No. 1118)

Functional Diagrams



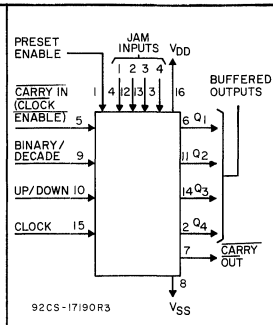
Dual J-K Master-Slave Flip-Flop with Set-Reset Capability

CD4027B (File No. 942)



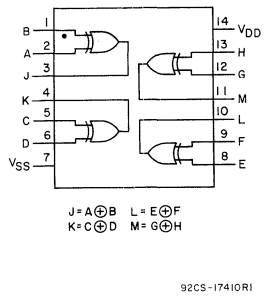
BCD-to-Decimal Decoder

CD4028B (File No. 1016)



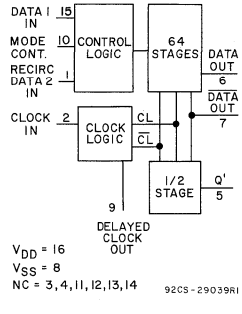
Presettable Up/Down Counter, Binary or BCD-Decade

CD4029B (File No. 1028)



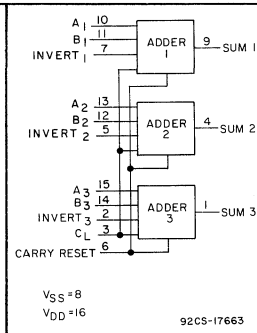
Quad Exclusive-OR Gate

CD4030B (File No. 1055)



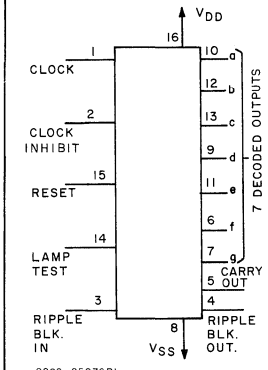
64-Stage Static Shift Register

CD4031B (File No. 1073)



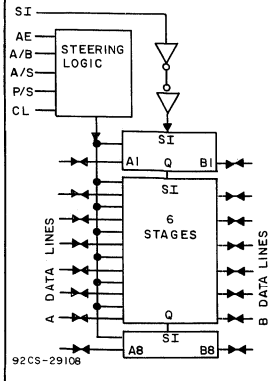
Triple Serial Adders

CD4032B (File No. 1081)
Positive Logic Adder
CD4038B (File No. 1081)
Negative Logic Adder



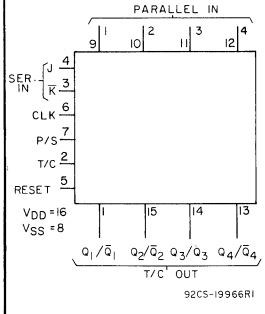
Decade Counter/Divider with 7-Segment Display Outputs and Ripple Blanking

CD4033B (File No. 1118)



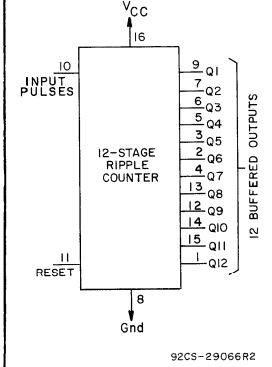
8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

CD4034B (File No. 1062)



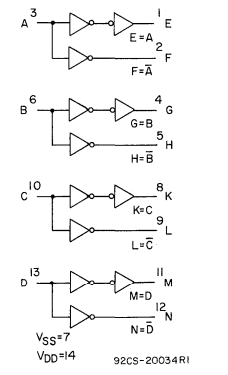
4-Stage Parallel In/Parallel Out Shift Register with J-K Serial Inputs and True/ Complement Outputs

CD4035B (File No. 1101)



12-Stage Ripple-Carry Binary Counter/Divider

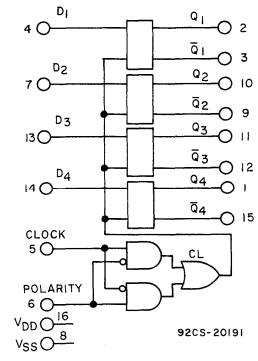
CD4040B (File No. 1063)



Quad True/Complement Buffer

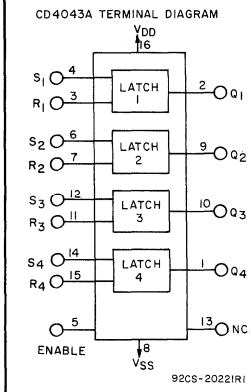
CD4041UB (File No. 934)

Functional Diagrams



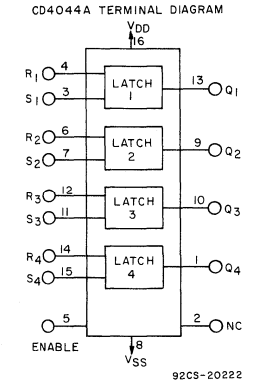
Quad Clocked "D" Latch

CD4042B (File No. 954)



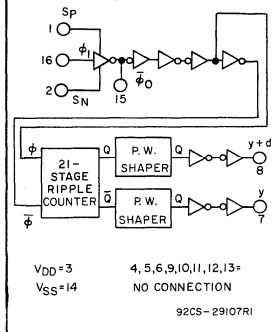
Quad 3-State NOR R/S Latch

CD4043B (File No. 956)



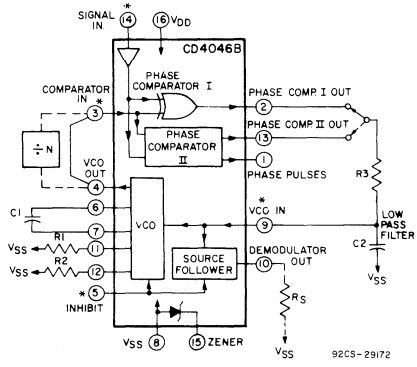
Quad 3-State NAND R/S Latch

CD4044B (File No. 956)



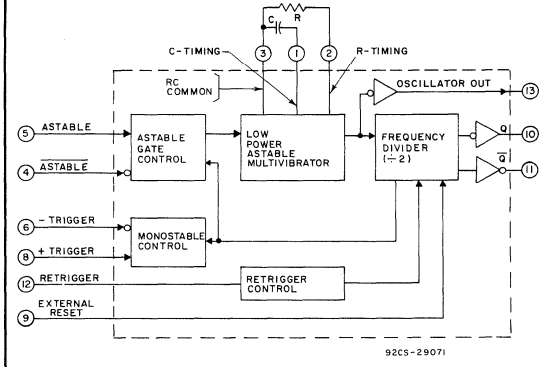
21-Stage Counter

CD4045B (File No. 1119)



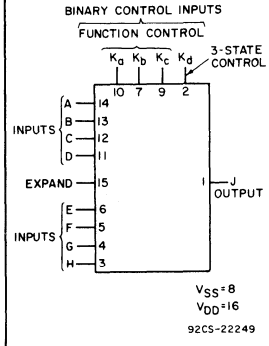
Micropower Phase-Locked Loop

CD4046B (File No. 1099)



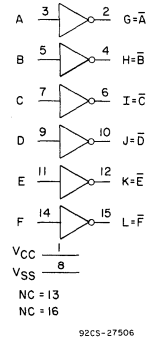
Low-Power Monostable/Astable Multivibrator

CD4047B (File No. 1123)



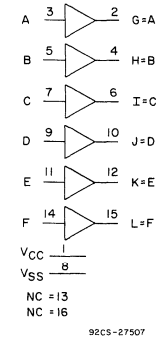
Multi-Function Expandable 8-Input Gate

CD4048B (File No. 1124)



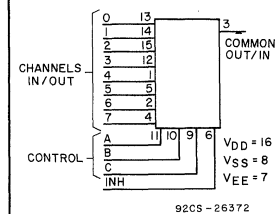
Hex Buffer/Converter Inverting Type

CD4049UB (File No. 926)



Hex Buffer/Converter Non-Inverting Type

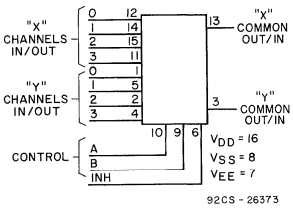
CD4050B (File No. 926)



Single 8-Channel Analog Multiplexer/Demultiplexer

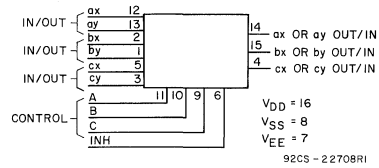
CD4051B (File No. 902)

Functional Diagrams



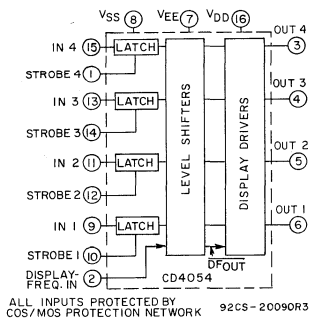
Differential 4-Channel Analog Multiplexer/Demultiplexer

CD4052B (File No. 902)



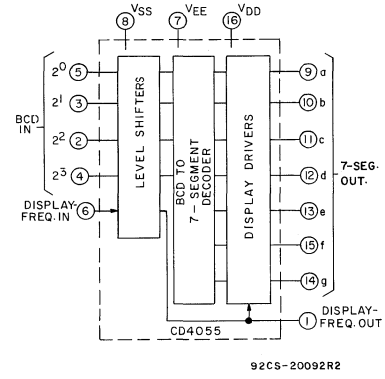
Triple 2-Channel Multiplexer/Demultiplexer

CD4053B (File No. 902)



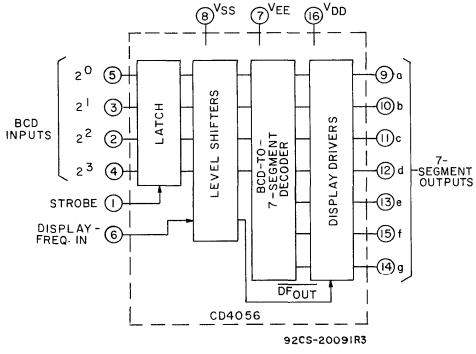
4-Segment Liquid-Crystal Display Driver

CD4054B (File No. 634)



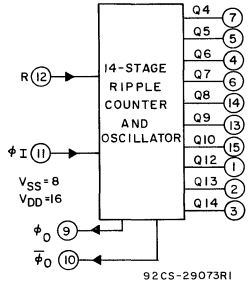
BCD-to-7 Segment Decoder/Driver with Display Frequency Output Liquid-Crystal Display Driver

CD4055B (File No. 634)



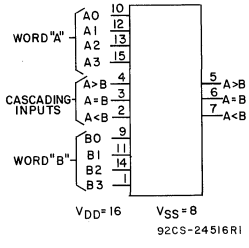
BCD-to-7-Segment Decoder/Driver with Strobed-Latch Function Liquid-Crystal Display Driver

CD4056B (File No. 634)



14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

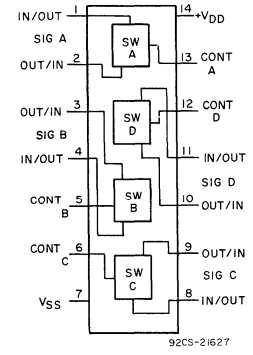
CD4060B (File No. 1120)



4-Bit Magnitude Comparator

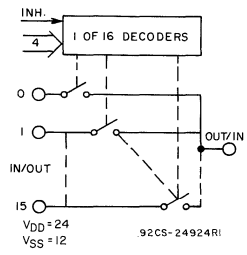
CD4063B (File No. 805)

Functional Diagrams



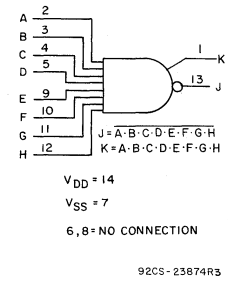
Quad Bilateral Switch

CD4066B (File No. 1114)



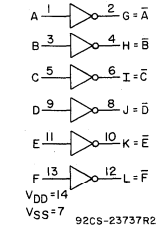
16-Channel Multiplexer/Demultiplexer

CD4067B (File No. 909)



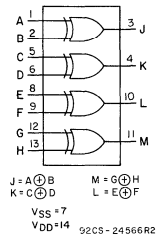
8-Input NAND/AND Gate

CD4068B (File No. 809)



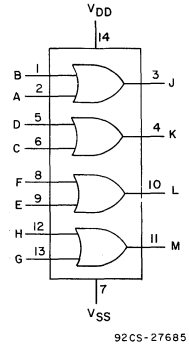
Hex Inverter

CD4069UB (File No. 804)



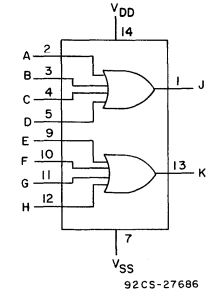
Quad Exclusive-OR Gate

CD4070B (File No. 910)



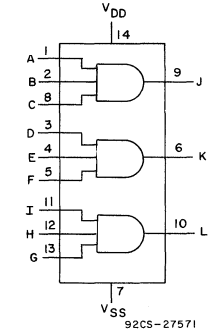
Quad 2-Input OR Gate

CD4071B (File No. 807)



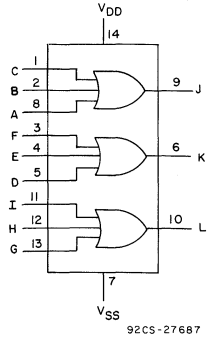
Dual 4-Input OR Gate

CD4072B (File No. 807)



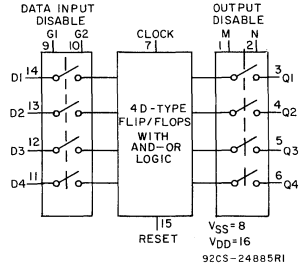
Triple 3-Input AND Gate

CD4073B (File No. 806)



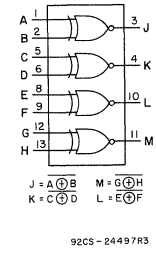
Triple 3-Input OR Gate

CD4075B (File No. 807)



4-Bit D-Type Register

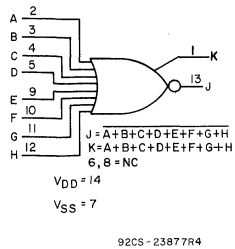
CD4076B (File No. 903)



Quad Exclusive-NOR Gate

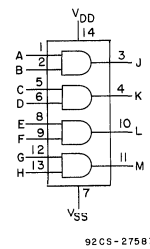
CD4077B (File No. 910)

Functional Diagrams



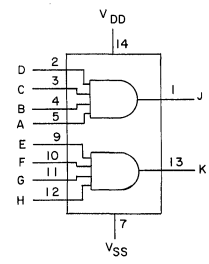
8-Input NOR/OR Gate

CD4078B (File No. 810)



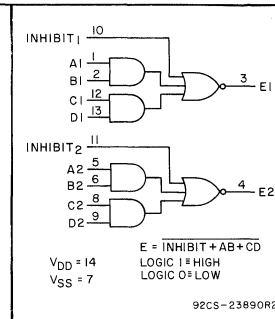
Quad 2-Input AND Gate

CD4081B (File No. 806)



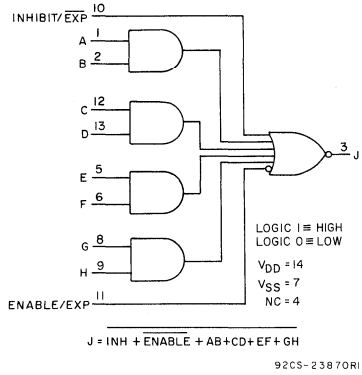
Dual 4-Input AND Gate

CD4082B (File No. 806)



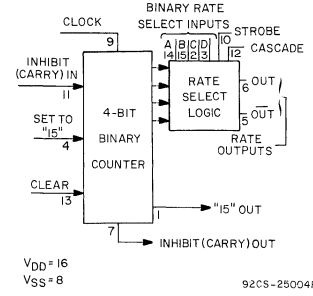
Dual 2-Wide, 2-Input AND-OR-INVERT (AOI) Gate

CD4085B (File No. 811)



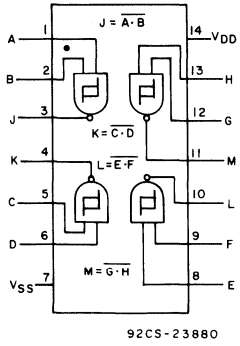
Expandable 4-Wide, 2-Input AND-OR-INVERT (AOI) Gate

CD4086B (File No. 812)



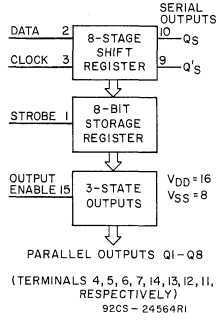
Binary Rate Multiplier

CD4089B (File No. 1003)



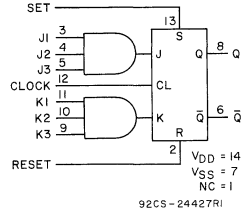
Quad 2-Input NAND Schmitt Trigger

CD4093B (File No. 836)



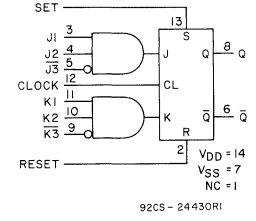
8-Stage Shift-and-Store Bus Register

CD4094B (File No. 869)



Gated J-K Master-Slave Flip-Flop, Non-Inverting Inputs

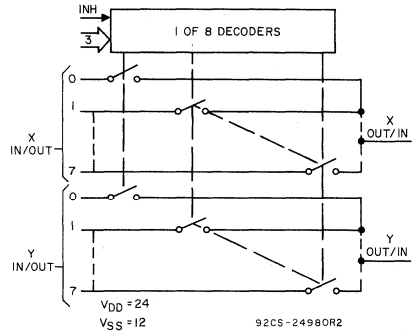
CD4095B (File No. 879)



Gated J-K Master-Slave Flip-Flop, Inverting and Non-Inverting Inputs

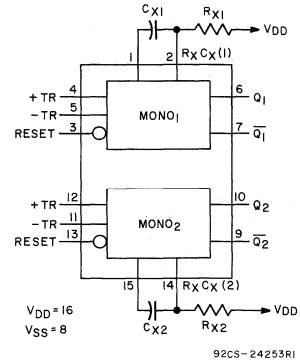
CD4096B (File No. 879)

Functional Diagrams



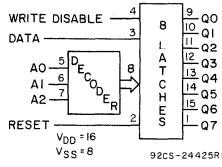
Differential 8-Channel Multiplexer/Demultiplexer

CD4097B (File No. 909)



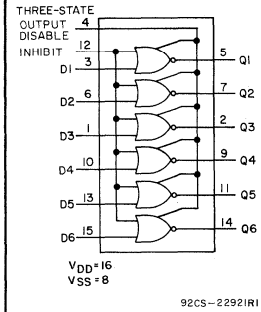
Dual Monostable Multivibrator

CD4098B (File No. 979)



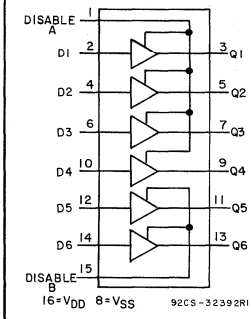
8-Bit Addressable Latch

CD4099B (File No. 948)



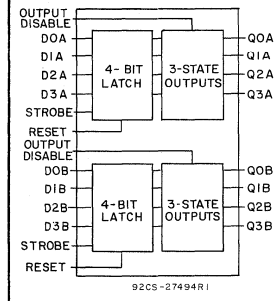
Strobed Hex Inverter/Buffer

CD4502B (File No. 1002)



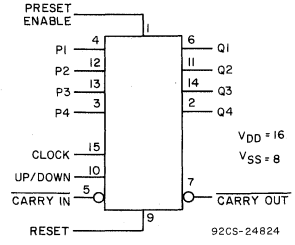
Hex Buffer Non-Inverting Type

CD4503B (File No. 1224)



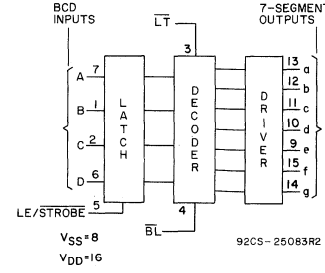
Dual 4-Bit Latch

CD4508B (File No. 1009)



BCD Presettable Up/Down Counter

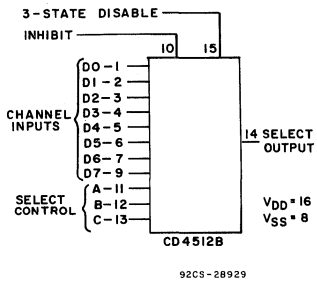
CD4510B (File No. 899)



BCD-to-7-Segment Latch Decoder Driver

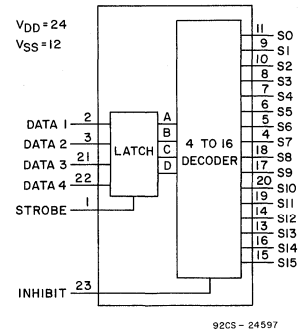
CD4511B (File No. 901)

Functional Diagrams



8-Channel Data Selector

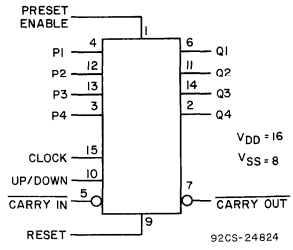
CD4512B (File No. 1032)



4-Bit Latch/4-to-16 Line Decoder

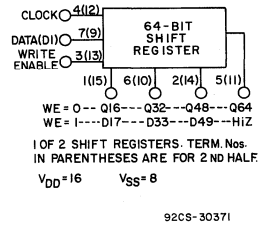
CD4514B (File No. 814) Output "High" on Select

CD4515B (File No. 814) Output "Low" on Select



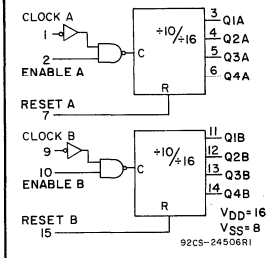
Binary Presettable Up/Down Counter

CD4516B (File No. 899)



Dual 64-Bit Shift Register

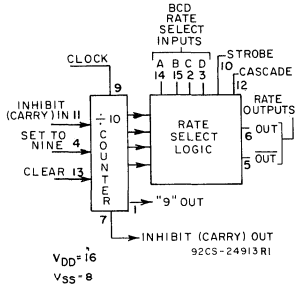
CD4517B (File No. 1148)



Dual Up Counter

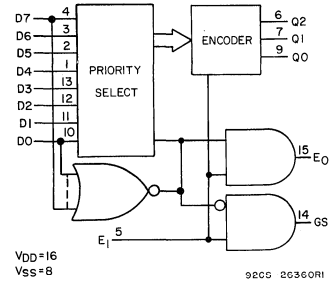
CD4518B (File No. 808) BCD

CD4520B (File No. 808) Binary



BCD Rate Multiplier

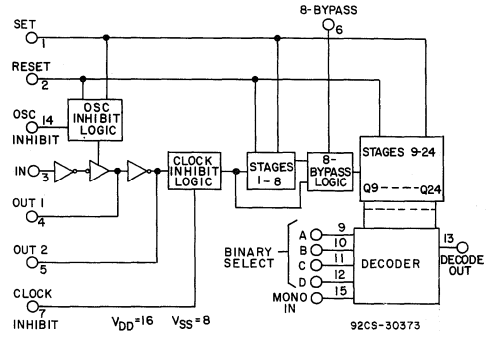
CD4527B (File No. 1006)



8-Bit Priority Encoder

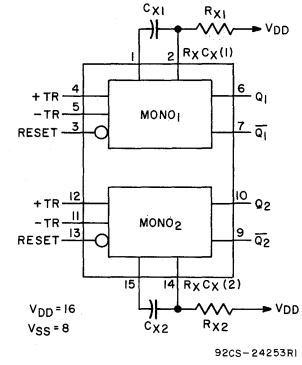
CD4532B (File No. 876)

Functional Diagrams



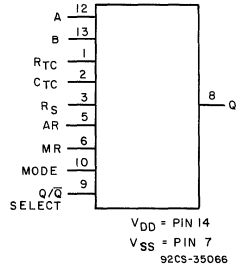
Programmable Timer

CD4536B (File No. 1186)



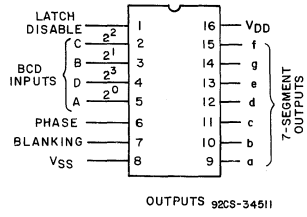
Dual Precision Monostable Multivibrator

CD4538B (File No. 1245)



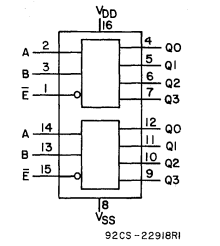
Programmable Timer

CD4541B (File No. 1378)



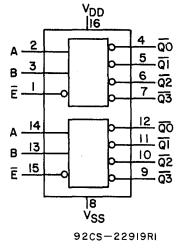
BCD-to-7-Segment Latch/Decoder/Driver

CD4543B (File No. 1327)



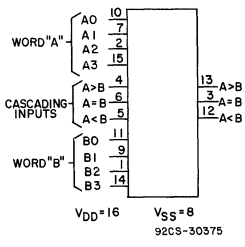
Dual Binary-to-1-of-4 Decoder/Demultiplexer Output "High" on Select

CD4555B (File No. 858)



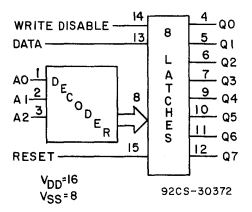
Dual Binary-to-1-of-4 Decoder/Demultiplexer Output "Low" on Select

CD4556B (File No. 858)



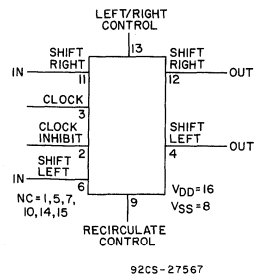
4-Bit Magnitude Comparator

CD4585B (File No. 1146)



8-Bit Addressable Latch

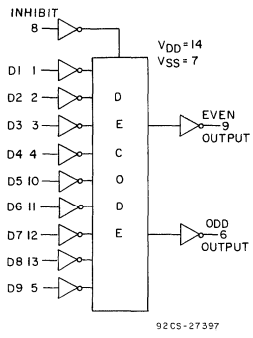
CD4724B (File No. 1111)



32-Stage Static Left/Right Shift Register

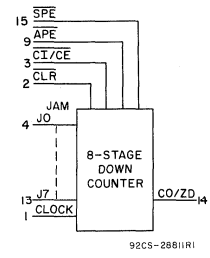
CD40100B (File No. 980)

Functional Diagrams



9-Bit Parity Generator/Checker

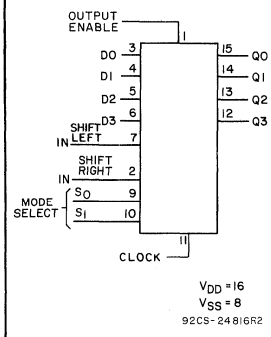
CD40101B (File No. 1000)



8-Stage Presettable Synchronous Down Counter

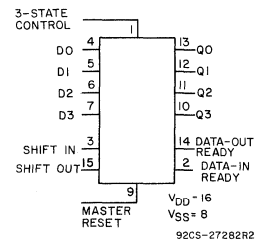
CD40102B (File No. 984)
2-Decade BCD

CD40103B (File No. 984)
8-Bit Binary



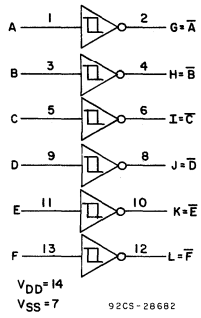
4-Bit Bidirectional Universal Shift Register

CD40104B, CD40194B
(File No. 1220)



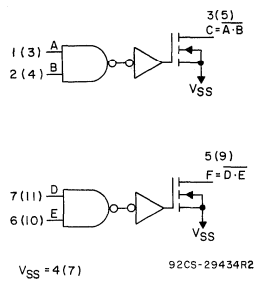
FIFO Register 4-Bits Wide by 16-Bits Long

CD40105B (File No. 1044)



Hex Schmitt Trigger

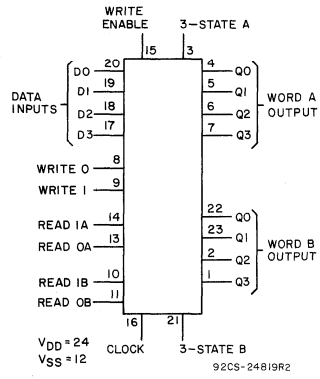
CD40106B (File No. 1017)



NOTE:
NUMBERS IN PARENTHESES FOR CD40107BF, OTHERS FOR CD40107BE.

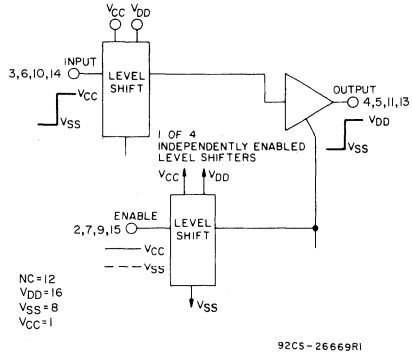
Dual 2-Input NAND Buffer/Driver

CD40107B (File No. 1015)



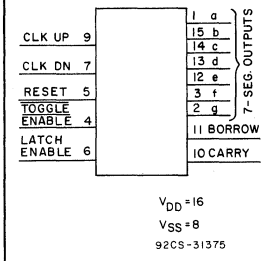
4-by-4 Multiport Register

CD40108B (File No. 1011)



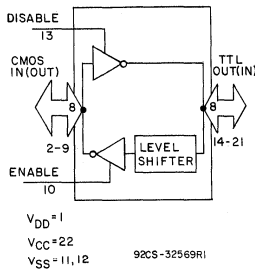
Quad Low-to-High Voltage Level Shifter

CD40109B (File No. 1018)



Decade Up-Down Counter/ Decoder/Latch/Driver

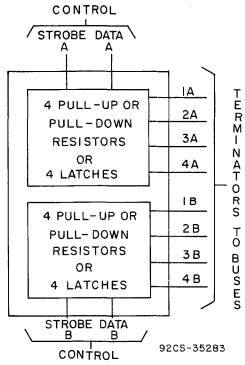
CD40110B (File No. 1125)



8-Bit Universal Bidirectional CMOS/TTL Level Converter

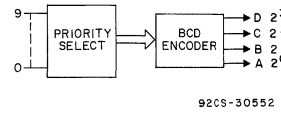
CD40116B (File No. 689)

Functional Diagrams



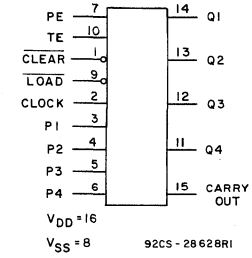
Programmable Dual 4-Bit Terminator

CD40117B (File No. 1333)



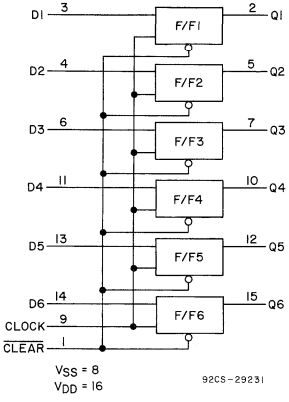
10-Line-to-4-Line BCD Priority Encoder

CD40147B (File No. 1117)



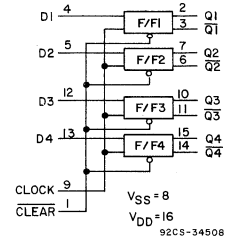
Synchronous 4-Bit Counter

CD40160B (File No. 1047)
Decade with Asynchronous Clear
CD40161B (File No. 1047)
Binary with Asynchronous Clear
CD40162B (File No. 1047)
Decade with Synchronous Clear
CD40163B (File No. 1047)
Binary with Synchronous Clear



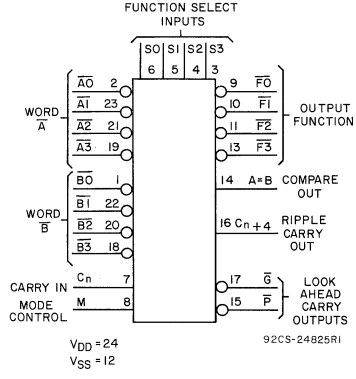
Hex "D" Type Flip-Flop

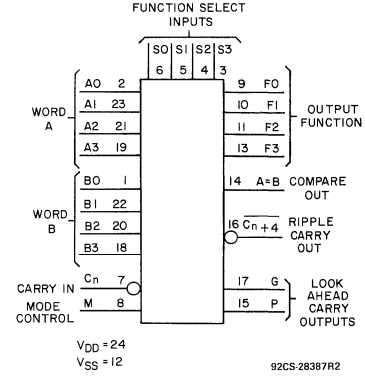
CD40174B (File No. 1031)



Quad 'D'-Type Flip-Flop

CD40175B (File No. 1326)



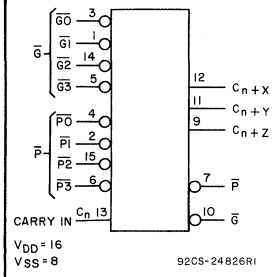


4-Bit Arithmetic Logic Unit

Active-Low Data **Active-High Data**

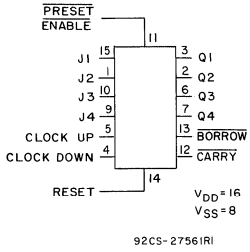
CD40181B (File No. 989)

Functional Diagrams



Look-Ahead Carry Generator

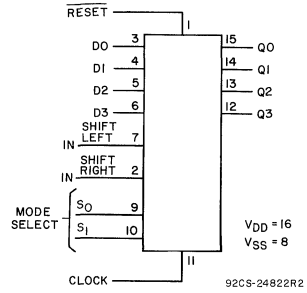
CD40182B (File No. 1008)



Presettable Up/Down Counter (Dual Clock with Reset)

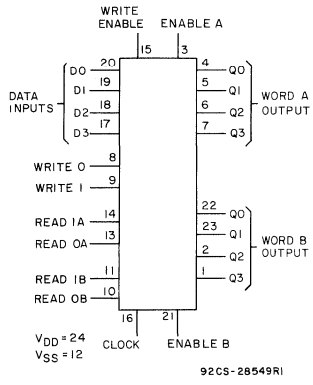
CD40192B (File No. 993)
BCD

CD40193B (File No. 993)
Binary



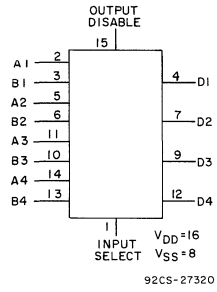
4-Bit Universal Bidirectional Shift Register with Asynchronous Master Reset

CD40194B (File No. 1220)



4-by-4 Multiport Register

CD40208B (File No. 1007)



Quad 2-Line-to-1-Line Data Selector/Multiplexer

CD40257B (File No. 982)

Static Burn-In Test-Circuit Connections

For Type A devices, use V_{DD} = 12.5V. For Type B and UB devices, use V_{DD} = 18V.

NOTE: Each pin except V_{DD} and V_{SS} must have resistors of 2-47 kilohms. In most cases, V_{SS} is at pin 7 (of 14-pin IC), pin 8 (of 16-pin) or pin 12 (of 24-pin), while V_{DD} is at the highest-numbered pin; exceptions are noted by an asterisk (*).

	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{DD}	OPEN	GROUND	V_{DD}
CD4000	1,2,6,9,10	3-5,7,8,11-13	14	1,2,6,9,10	7	3-5,8,11-14
CD4001	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9, 12-14
CD4002	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD4006	2,8-13	1,3-7	14	2,8-13	7	1,3-6,14
CD4007	1,5,8,12,13	3,4,6,7,9,10	2,11,14	1,5,8,12,13	4,7,9	2,3,6,10,11,14
CD4008	10-14	1-9,15	16	10-14	8	1-7,9,15,16
CD4009*	2,4,6,10,12, 13,15	3,5,7-9,11,14	1•,16•	2,4,6,10,12,13,15	8	1•,3,5,7,9,11, 14,16•
CD4010*	2,4,6,10,12, 13,15	3,5,7-9,11,14	1•,16•	2,4,6,10,12,13,15	8	1•,3,5,7,9,11, 14,16•
CD4011	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4012	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD4013	1,2,12,13	3-11	14	1,2,12,13	7	3-6,8-11,14
CD4014	2,3,12	1,4-11,13-15	16	2,3,12	8	1,4-7,9-11,13-16
CD4015	2-5,10-13	1,6-9,14,15	16	2-5,10-13	8	1,6,7,9,14-16
CD4016	2,3,9,10	1,4-8,11-13	14	2,3,9,10	7	1,4-6,8,11-14
CD4017	1-7,9-12	8,13-15	16	1-7,9-12	8	13-16
CD4018	4-6,11,13	1-3,7-9,10,12, 14,15	16	4-6,11,13	8	1-3,7,9,10,12 14-16
CD4019	10-13	1-9,14,15	16	10-13	8	1-7,9,14-16
CD4020	1-7,9,12-15	8,10,11	16	1-7,9,12-15	8	10,11,16
CD4021	2,3,12	1,4-11,13-15	16	2,3,12	8	1,4-7,9-11,13-16
CD4022	1-7,9-12	8,13-15	16	1-7,9-12	8	13-16
CD4023	6,9,10	1-5,7,8,11-13	14	6,9,10	7	1-5,8,11-14
CD4024	3-6,8-13	1,2,7	14	3-6,8-13	7	1,2,14
CD4025	6,9,10	1-5,7,8,11-13	14	6,9,10	7	1-5,8,11-14
CD4026	4-7,9-14	1-3,8,15	16	4-7,9-14	8	1-3,15,16
CD4027	1,2,14,15	3-13	16	1,2,14,15	8	3-7,9-13,16
CD4028	1-7,9,14,15	8,10-13	16	1-7,9,14,15	8	10-13,16
CD4029	2,6,7,11,14	1,3-5,8-10,12, 13,15	16	2,6,7,11,14	8	1,3-5,9,10,12,13 15,16
CD4030	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4031	3-7,9,11-14	1,2,8,10,15	16	3-7,9,11-14	8	1,2,10,15,16
CD4032	1,4,9	2,3,5-8,10-15	16	1,4,9	8	2,3,5-7,10-16
CD4033	4-7,9-13	1-3,8,14,15	16	4-7,9-13	8	1-3,14-16
CD4034	1-8	12,15-23	9-11,13,14,24	1-8	12	9-11,13-24
CD4035	1,13-15	2-12	16	1,13-15	8	2-7,9-12,16
CD4038	1,4,9	2,3,5-8,10-15	16	1,4,9	8	2,3,5-7,10-16
CD4040	1-7,9,12-15	8,10,11	16	1-7,9,12-15	8	10,11,16
CD4041	1,2,4,5,8,9,11,12	3,6,7,10,13	14	1,2,4,5,8,9,11,12	7	3,6,10,13,14
CD4042	1-3,9-12,15	4-8,13,14	16	1-3,9-12,15	8	4-7,13,14,16
CD4043	1,2,9,10,13	3-8,11,12,14,15	16	1,2,9,10,13	8	3-7,11,12,14-16
CD4044	1,2,9,10,13	3-8,11,12,14,15	16	1,2,9,10,13	8	3-7,11,12,14-16
CD4045*	4-13,15	2,14•,16	1,3•	4-13,15	2,14•	1,3•,16
CD4046	1,2,4,6,7,10,11, 13,15	3,5,8,9,14	12,16	1,2,4,6,7,10,11, 13,15	8	3,5,9,12,14,16
CD4047	1,2,10,11,13	3-9,12	14	1,2,10,11,13	7	3-6,8,9,12,14

*Non-standard pin arrangement, or multiple supply pins; connect pins marked (•) without using resistor.

Static Burn-In Test-Circuit Connections

TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{DD}	OPEN	GROUND	V_{DD}
CD4048	1	2-15	16	1	8	2-7,9-16
CD4049*	2,4,6,10,12, 13,15	3,5,7-9,11,14	1•,16•	2,4,6,10,12, 13,15	8	1•,3,5,7,9,11, 14.16•
CD4050*	2,4,6,10,12, 13,15	3,5,7-9,11,14	1•,16•	2,4,6,10,12, 13,15	8	1•,3,5,7,9,11, 14,16•
CD4051*	3	1,2,4-6,7•,8•, 9-15	16	3	7•,8•	1,2,4-6,9-16
CD4052*	3,13	1,2,4-6,7•,8•, 9-12,14,15	16	3,13	7•,8•	1,2,4-6,9-12, 14-16
CD4053*	4,14,15	1-3,5,6,7•,8•, 9-13	16	4,14,15	7•,8•	1-3,5,6,9-13,16
CD4054*	3-6	1,2,7•,8-15	16	3-6	7•,8	1,2,9-16
CD4055*	1,9-15	2-6,7•,8	16	1,9-15	7•,8	2-6,,16
CD4056*	9-15	1-6,7•,8	16	9-15	7•,8	1-6, 16
CD4060	1-7,9,10,13-15	8,11,12	16	1-7,9,10,13-15	8	11,12,16
CD4063	5-7	1,2,4,8-15	3,16	5-7	3,8	1,2,4,9-16
CD4066	2,3,9,10	1,4-8,11-13	14	2,3,9,10	7	1,4-6,8,11-14
CD4067	1	2-23	24	1	12	2-11,13-23
CD4068	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD4069	2,4,6,8,10,12	1,3,5,7,9,11,13	14	2,4,6,8,10,12	7	1,3,5,9,11,13,14
CD4070	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4071	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4072	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD4073	6,9,10	1-5,7,8,11-13	14	6,9,10	7	1-5,8,11-14
CD4075	6,9,10	1-5,7,8,11-13	14	6,9,10	7	1-5,8,11-14
CD4076	3-6	1,2,7-15	16	3-6	8	1,2,7,9-16
CD4077	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4078	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD4081	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4082	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD4085	3,4	1,2,5-13	14	3,4	7	1,2,5,6,8-14
CD4086	3,4	1,2,5-13	14	3,4	7	1,2,5,6,8-14
CD4089	1,5-7	2-4,8-15	16	1,5-7	8	2-4,9-16
CD4093	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4094	4-7,9-14	1-3,8,15	16	4-7,9-14	8	1-3,15,16
CD4095	1,6,8	2-5,7,9-13	14	1,6,8	7	2-5,9-14
CD4096	1,6,8	2-5,7,9-13	14	1,6,8	7	2-5,9-14
CD4097	1,17	2-16,18-23	24	1,17	12	2-11,13-24
CD4098	2,6,7,9,10,14	1,3-5,8,11-13,15	16	2,6,7,9,10,14	1,8,15	3-5,11-13,16
CD4099	1,9-15	2-8	16	1,9-15	8	2-7,16
CD4502	2,5,7,9,11,14	1,3,4,6,8,10,12, 13,15	16	2,5,7,9,11,14	8	1,3,4,6,10,12,13 15,16
CD4503	3,5,7,9,11,13	1,2,4,6,8,10,12, 14,15	16	3,5,7,9,11,13	8	1,2,4,6,10,12, 14-16
CD4508	5,7,9,11,17,19, 21,23	1-4,6,8,10, 12-16,18,20,22	24	5,7,9,11,17,19, 21,23	12	1-4,6,8,10,13-16, 18,20,22,24
CD4510	2,6,7,11,14	1,3-5,8-10,12, 13,15	16	2,6,7,11,14	8	1,3-5,9,10,12, 13,15,16
CD4511	9-15	1-8	16	9-15	8	1-7,16
CD4512	14	1-13,15	16	14	8	1-7,9-13,15,16
CD4514	4-11,13-20	1-3,12,21-23	24	4-11,13-20	12	1-3,21-24

*Non-standard pin arrangement, or multiple supply pins; connect pins marked (•) without using resistor.

Static Burn-In Test-Circuit Connections

TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{DD}	OPEN	GROUND	V_{DD}
CD4515	4-11,13-20	1-3,12,21-23	24	4-11,13-20	12	1-3,21-24
CD4516	2,6,7,11,14	1,3-5,8-10,12, 13,15	16	2,6,7,11,14	8	1,3-5,9,10,12, 13,15,16
CD4517	1,2,5,6,10,11, 14,15	3,4,7-9,12,13	16	1,2,5,6,10,11, 14,15	8	3,4,7,9,12, 13,16
CD4518	3-6,11-14	1,2,7-10,15	16	3-6,11-14	8	1,2,7,9,10, 15,16
CD4520	3-6,11-14	1,2,7-10,15	16	3-6,11-14	8	1,2,7,9,10, 15,16
CD4527	1,5-7	2-4,8-15	16	1,5-7	8	2-4,9-16
CD4532	6,7,9,14,15	1-5,8,10-13	16	6,7,9,14,15	8	1-5,10-13,16
CD4536	4,5,13	1-3,6-12,14,15	16	4,5,13	8	1-3,6,7,9-12, 14-16
CD4538	2,6,7,9,10,14	1,3-5,8,11-13,15	16	2,6,7,9,10,14	1,8,15	3-5,11-13,16
CD4541	1,2,4,8,11	3,5-7,9,10,12,13	14	1,2,4,8,11	7	3,5,6,9,10, 12-14
CD4543	9-15	1-8	16	9-15	8	1-7
CD4555	4-7,9-12	1-3,8,13-15	16	4-7,9-12	8	1-3,13-16
CD4556	4-7,9-12	1-3,8,13-15	16	4-7,9-12	8	1-3,13-16
CD4585	3,12,13	1,2,4-11,14,15	16	3,12,13	8	1,2,4-7,9-11, 14-16
CD4724	4-7,9-12	1-3,8,13-15	16	4-7,9-12	8	1,3,13-16
CD40100	1,4,5,7,10,12,14 15	2,3,6,8,9,11,13	16	1,4,5,7,10,12, 14,15	8	2,3,6,9,11, 13,16
CD40101	6,9	1-5,7,8,10-13	14	6,9	7	1-5,8,10-14
CD40102	14	1-13,15	16	14	8	1-7,9-13,15,16
CD40103	14	1-13,15	16	14	8	1-7,9-13,15,16
CD40104	12-15	1-11	16	12-15	8	1-7,9-11,16
CD40105	2,10-14	1,3-9,15	16	2,10-14	8	1,3-7,9,16
CD40106	2,4,6,8,10,12	1,3,5,7,9,11,13	14	2,4,6,8,10,12	7	1,3,5,9,11, 13,14
CD40107	1,2,5,6,8,9, 12,13	3,4,7,10,11	14	1,2,5,6,8,9,12,13	7	3,4,10,11,14
CD40108	1,2,4-7,22,23	3,8-21	24	1,2,4-7,22,23	12	3,8-11,13-21, 24
CD40109*	4,5,11-13	2,3,6-10,14,15	1•,16	4,5,11-13	8	(1•,2,3,6,7,9,10, 14,15)[1]16
CD40110	1-3,10-15	4-9	16	1-3,10-15	8	4-7,9,16
CD40116*	—	—	—	2-9	11,12	(1•,10=V_{DD})[2] (13-22•=V_{CC})
CD40117	3-6,8-11	1,2,7,12,13	14	3-6,8-11	7	1,2,12-14
CD40147	6,7,9,14	1-5,8,10-13	16	6,7,9,14	8	1-5,10-13,16
CD40160	11-15	1-10	16	11-15	8	1-7,9,10,16
CD40161	11-15	1-10	16	11-15	8	1-7,9,10,16
CD40162	11-15	1-10	16	11-15	8	1-7,9,10,16
CD40163	11-15	1-10	16	11-15	8	1-7,9,10,16
CD40174	2,5,7,10,12,15	1,3,4,6,8,9,11, 13,14	16	2,5,7,10,12,15	8	1,3,4,6,9,11,13, 14,16
CD40175	2,3,6,7,10,11, 14,15	1,4,5,8,9,12,13	16	2,3,6,7,10,11, 14,15	8	1,4,5,9,12,13,16
CD40181	9-11,13-17	1-8,12,18-23	24	9-11,13-17	12	1-8,18-24
CD40182	7,9-12	1-6,8,13-15	16	7,9-12	8	1-6,13-16

*Non-standard pin arrangement, or multiple supply pins; connect pins marked (•) without using resistor.
[1]Pin voltage is $V_{DD}/2$ for pins inside parentheses.
[2]V_{DD} = 11.5 volts; V_{CC} = 6.5 volts; use 300 Ω resistors at pins 10,13-21.

Static Burn-In Test-Circuit Connections

TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{DD}	OPEN	GROUND	V_{DD}
CD40192	2,3,6,7,12,13	1,4,5,8-11,14,15	16	2,3,6,7,12,13	8	1,4,5,9-11, 14-16
CD40193	2,3,6,7,12,13	1,4,5,8-11,14,15	16	2,3,6,7,12,13	8	1,4,5,9-11, 14-16
CD40194	12-15	1-11	16	12-15	8	1-7,9-11,16
CD40208	1,2,4-7,22,23	3,8-21	24	1,2,4-7,22,23	12	3,8-11,13-21, 24
CD40257	4,7,9,12	1-3,5,6,8,10,11, 13-15	16	4,7,9,12	8,15	1-3,5,6,10,11, 13,14,16

Dynamic Burn-In Test-Circuit Connections

For Type A devices, use V_{DD} = 12.5V and 1/2 V_{DD} = 6.25V.
For Type B and UB devices, use V_{DD} = 18V and 1/2 V_{DD} = 9V.
NOTE: Each pin except V_{DD} and V_{SS} may have resistors of 2-47 kilohms. In most cases, V_{SS} is at pin 7 (of 14-pin IC), pin 8 (of 16-pin IC), or pin 12 (of 24-pin IC) while V_{DD} is at the highest-numbered pin. Exceptions are marked by an asterisk (*).

TYPE	OPEN	GROUND	1/2 V_{DD}	V_{DD}	OSCILLATOR	
					50 kHz	25 kHz
CD4000	1,2	7	6,9,10	14	3-5,8,11-13	—
CD4001	—	7	3,4,10,11	14	1,2,5,6,8,9,12,13	—
CD4002	6,8	7	1,13	14	2-5,9-12	—
CD4006	2	7	8-13	14	3	1,4-6
CD4007	—	4,7,9	1,5,8,12,13	2,11,14	3,6,10	—
CD4008	—	8	10-14	16	2,4,6,15	1,3,5,7,9
CD4009*	13	8	2,4,6,10,12,15	1•,16•	3,5,7,9,11,14	—
CD4010*	13	8	2,4,6,10,12,15	1•,16•	3,5,7,9,11,14	—
CD4011	—	7	3,4,10,11	14	1,2,5,6,8,9,12,13	—
CD4012	6,8	7	1,13	14	2-5,9-12	—
CD4013	—	4,6-8,10	1,2,12,13	14	3,11	5,9
CD4014	—	1,4-9,13-15	2,3,12	16	10	11
CD4015	—	6,8,14	2-5,10-13	16	1,9	7,15
CD4016	—	7	2,3,9,10	14	5,6,12,13	1,4,8,11
CD4017	—	8,13,15	1-7,9-12	16	14	—
CD4018	—	2,8,9,15	4-6,11,13	1,3,12,16	7,14	10
CD4019	—	8	10-13	16	—	1-7,9,14,15
CD4020	—	8,11	1-7,9,12-15	16	10	—
CD4021	—	1,4-9,13-15	2,3,12	16	10	11
CD4022	—	8,13,15	1-7,9-12	16	14	—
CD4023	—	7	6,9,10	14	1-5,8, 11-13	—
CD4024	8,10,13	2,7	3-6,9,11,12	14	1	—
CD4025	—	7	6,9,10	14	1-5,8,11-13	—
CD4026	—	2,8,15	4-7,9-14	3,16	1	—
CD4027	—	4,7-9,12	1,2,14,15	5,6,10,11,16	3,13	—
CD4028	—	8	1-7,9,14,15	16	10,12,13	11
CD4029	—	1,3-5,8,12,13	2,6,7,11,14	9,10,16	15	—
CD4030	—	7	3,4,10,11	14	2,6,9,13	1,5,8,12
CD4031	3-5,11-14	8,15	6,7,9	1,16	2	10
CD4032	—	2,5-8	1,4,9	10,13,15,16	3	11,12,14
CD4033	—	2,3,8,14,15	4-7,9-13	16	1	—
CD4034	—	1-8,11-14	16-23	9,24	15	10
CD4035	1,3,4	2,5,7-12	13-15	16	6	—
CD4038	—	2,5-8	1,4,9	10,13,15,16	3	11,12,14

*Non-standard pin arrangement, or multiple supply pins; connect pins marked (•) without using a resistor.

Dynamic Burn-In Test-Circuit Connections

TYPE	OPEN	GROUND	1/2 V_{DD}	V_{DD}	OSCILLATOR	
					50 kHz	25 kHz
CD4040	—	8,11	1-7,9,12-15	16	10	—
CD4041	—	7	1,2,4,5,8,9,11,12	14	3,6,10,13	—
CD4042	—	8	1-3,9-12,15	6,16	5	4,7,13,14
CD4043	13	8	1,2,9,10	5,16	4,6,12,14	3,7,11,15
CD4044	2	8	1,9,10,13	5,16	4,6,12,14	3,7,11,15
CD4045*	4-6,9-13,15	2,14•	7,8	1,3•	16	—
CD4046	1,4,6,7,10,11, 13,15	8,9	2	3,5,12,16	14	—
CD4047	—	7,9,12	1,2,10,11,13	4,5,14	6,8	3
CD4048	—	8,15	1	2,16	9-14	3-7
CD4049*	13	8	2,4,6,10,12,15	1•,16	3,5,7,9,11,14	—
CD4050*	13	8	2,4,6,10,12,15	1•,16	3,5,7,9,11,14	—
CD4051*	—	4-6,7•,8•,9, 12,14	3	1,2,13,15,16	11	10
CD4052*	—	4-6,7•,8•,12,15	3,13	1,2,11,14,16	10	9
CD4053*	—	1,5,6,7•,8•,12	4,14,15	2,3,13,16	9-11	—
CD4054	—	7•,8	3-6	1,10,12,14	2	9,11,13,15
CD4055	—	7•,8	1,9-15	16	6	2-5
CD4056	—	7•,8	9-15	1,16	6	2-5
CD4060	—	8,12	1-7,9,10,13-15	16	11	—
CD4063	—	1,2,4,8,10,11,13	5-7	3,16	12,15	9,14
CD4066	—	7	2,3,9,10	14	5,6,12,13	1,4,8,11
CD4067	—	12,15	1	24	2-9,16-23	(10,11,13,14)[1]
CD4068	6,8	7	1,13	14	2-5,9-12	—
CD4069	—	7	2,4,6,8,10,12	14	1,3,5,9,11,13	—
CD4070	—	7	3,4,10,11	14	1,5,8,12	2,6,9,13
CD4071	—	7	3,4,10,11	14	1,2,5,6,8,9,12,13	—
CD4072	6,8	7	1,13	14	2-5,9-12	—
CD4073	—	7	6,9,10	14	—	1-5,8,11-13
CD4075	—	7	6,9,10	14	—	1-5,8,11-13
CD4076	—	1,2,8-10,15	3-6	16	7	11-14
CD4077	—	7	3,4,10,11	14	1,5,8,12	2,6,9,13
CD4078	6,8	7	1,13	14	2-5,9-12	—
CD4081	—	7	3,4,10,11	14	1,2,5,6,8,9,12,13	—
CD4082	6,8	7	1,13	14	2-5,9-12	—
CD4085	—	7	3,4	14	1,2,5,6,8,9,12,13	10,11
CD4086	4	7	3	14	1,2,5,6,8,9,11-13	10
CD4089	—	2,4,8,10,12-15	1,5-7	3,16	9	11
CD4093	—	7	3,4,10,11	14	1,2,5,6,8,9,12,13	—
CD4094	—	8	4-7,9-14	1,15,16	3	2
CD4095	1	2,7,13	6,8	3-5,9-11,14	—	12
CD4096	1	2,5,7,9,13	6,8	3,4,10,11,14	12	—
CD4097	—	12,13	1,17	24	2-9,15,16,18-23	(10,11,14)[2]
CD4098	—	1,4,8,12,15	6,7,9,10	2,14,16	5,11	3,13
CD4099	—	5-8	1,9-15	16	2,4	3
CD4502	—	8	2,5,7,9,11,14	16	4	1,3,6,10,12,13,15
CD4503	—	1,8,15	3,5,7,9,11,13	16	2,4,6,10,12,14	—
CD4508	—	1,3,12,13,15	5,7,9,11,17,19, 21,23	2,14,24	4,6,8,10,16,18, 20,22	—
CD4510	—	1,3,4,8,9,12,13	2,6,7,11,14	10,16	15	5
CD4511	9-15	5,8	—	3,4,16	1,2,7	6

[1]Pin 10 is @ 14 kHz; pin 11 is @ 7 kHz; pin 13 is @ 1.7 kHz; pin 14 is @ 3.5 kHz.
[2]Pin 10 is 14 kHz; pin 11 is @ 7 kHz; pin 14 is @ 3.5 kHz.
*Non-standard pin arrangement or multiple supply pinS; connect pinS marked (•) without using a resistor.

Dynamic Burn-In Test-Circuit Connections

TYPE	OPEN	GROUND	1/2 V_{DD}	V_{DD}	OSCILLATOR	
					50 kHz	25 kHz
CD4512	—	8,10,15	14	16	1-7,9,11,12	13
CD4514	—	2,3,12	4-11,13-20	21,22,24	1	23
CD4515	—	2,3,12	4-11,13-20	21,22,24	1	23
CD4516	—	1,3,4,8,9,12,13	2,6,7,11,14	10,16	15	5
CD4517	—	3,8,13	1,2,5,6,10,11, 14,15	16	4,12	7,9
CD4518	—	7,8,15	3-6,11-14	2,10,16	1,9	—
CD4520	—	7,8,15	3-6,11-14	2,10,16	1,9	—
CD4527	—	2,4,8,10,12-15	1,5-7	3,16	9	11
CD4532	—	8	6,7,9,14,15	5,16	1-4,10-13	—
CD4536	—	1,2,6-8,14,15	4,5,13	9-12,16	3	—
CD4538	—	1,4,8,12,15	6,7,9,10	2,14,16	5,11	3,13
CD4541	4,11	5-7	1,2,8	9,10,12-14	3	—
CD4543	—	6-8	9-15	1,4,16	2,3,5	—
CD4555	—	1,8,15	4-7,9-12	16	2,14	3,13
CD4556	—	1,8,15	4-7,9-12	16	2,14	3,13
CD4585	—	5-9,11,14,15	3,12,13	1,4,16	2	10
CD4724	—	1-3,8	4-7,9-12	16	14,15	13
CD40100	1,5,7,10,14,15	2,8,13	4,12	9,16	3	6,11
CD40101	—	4,7	6,9	12,14	2,3,5,8,10	1,11,13
CD40102	—	3,8,15	14	2,16	1,4,6,11,13	5,7,9,10,12
CD40103	—	3,8,15	14	2,16	1,4,6,11,13	5,7,9,10,12
CD40104	—	7,8,10	12-15	1,3-6,9,16	11	2
CD40105	—	1,8,9	2,10-14	16	3,15	4-7
CD40106	—	7	2,4,6,8,10,12	14	1,3,5,9,11,13	—
CD40107	1,2,6,8,12,13	7	5,9	14	—	3,4,10,11
CD40108	—	12	1,2,4-7,22,23	3,15,16,21,24	8,11,14,19,20	9,10,13,17,18
CD40109*	12	8	1•,4,5,11,13	16	(3,6,10,14)[3]	(2,7,9,15)[3]
CD40110	—	4-8	1-3,10-15	16	9	—
CD40116*	—	—	—	—	—	—
CD40117	—	7	3-6,8-11	14	12,13	1,2
CD40147	—	8	6,7,9,14	16	1,3,11,13	2,4,5,10,12,15
CD40160	—	8	11-15	1,7,9,10,16	2-6	—
CD40161	—	8	11-15	1,7,9,10,16	2-6	—
CD40162	—	8	11-15	1,7,9,10,16	2-6	—
CD40163	—	8	11-15	1,7,9,10,16	2-6	—
CD40174	—	8	2,5,7,10,12,15	1,16	9	3,4,6,11,13,14
CD40175	—	8	2,3,6,7,10,11, 14,15	1,16	9	4,5,12,13
CD40181	—	4-6,8,12	9-11,13-17	3,24	1,2,18-23	7
CD40182	—	8	7,9-12	16	1-6,14,15	13
CD40192	—	8,14	2,3,6,7,12,13	1,5,9-11,15,16	4	—
CD40193	—	8,14	2,3,6,7,12,13	1,5,9-11,15,16	4	—
CD40194	—	7,8,10	12-15	1,3-6,9,16	11	2
CD40208	—	12	1,2,4-7,22,23	3,15,16,21,24	8,10,14,19,20	9,11,13,17,18
CD40257	—	8,15	4,7,9,12	16	2,3,5,6,10,11, 13,14	1

[3]Pin Voltage is $V_{DD}/2$.
*Non-standard pin arrangement, or multiple supply pins; connect pins marked (•) without using a resistor.

Leadless-Chip-Carrier Pinout

The following table and diagrams show JEDEC standard pinout conversions from 14-, 16-, 22-, and 24-pin leaded FP/DIL packages to 20- and 28-terminal leadless-chip carriers. RCA CD4000B-series products offered in leadless-chip carriers are shown below.

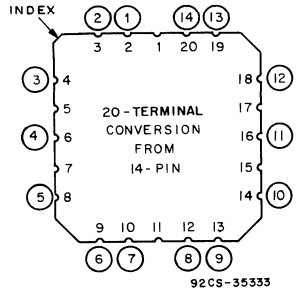
Pinout Conversion From Leaded Package to Leadless-Chip Carrier

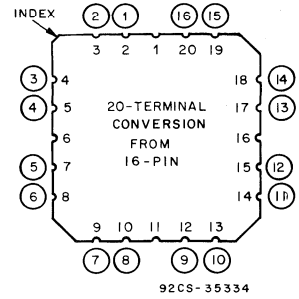
FP/DIL Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Leadless	2	3	4	6	8	9	10	12	13	14	16	18	19	20										
Chip	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20								
Carrier	2	3	4	5	6	8	10	11	12	13	14	16	17	18	19	20	22	24	25	26	27	28		
Terminal	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28

CD4000B-Series Conversion Diagrams

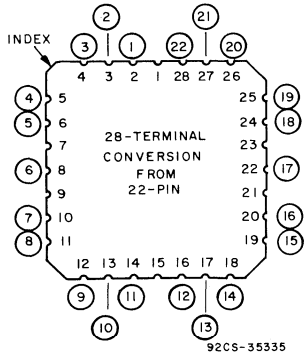
Top Views Shown

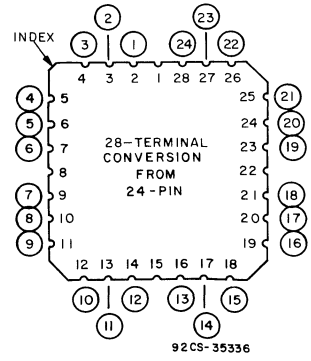
20-Terminal Leadless-Chip Carriers





28-Terminal Leadless-Chip Carriers





Reliability Data

Reliability Data for High-Reliability CD4000-Series CMOS IC's

The following pages provide reliability data of Failure Rates and MTTF covering primarily devices manufactured in the 1982 and 1983 time period. Emphasis has been placed on the CD4000B-series product processed to a radiation level of 10^5 rads (Si). Data is also provided on CD4000A-series devices made in 1982 and 1983. Also included is a table of the latest satellite and military applications for CMOS and BiPolar Devices. The data presented indicates excellent package integrity for device types evaluated and stability for devices subjected to life testing at 135°C and 125°C.

Satellite and Military Applications For RCA High-Reliability Devices

SATELLITES, AEROSPACE	MILITARY	
ATMOSPHERIC EXPLORER	TOW COBRA	PARKHILL
70P	TENLEY	MULTI ROLE COMBAT AIRCRAFT
HEAO	S-3A AIRCRAFT	AN-TPN-19
SPACE SHUTTLE	LANS PROGRAM	AN-ASQ-119
ITOS	D-1065 COMMUNICATIONS	ARCTIC BEACON
B-SAT	VINSON	AWACS
SAT COM	AIRS	MK46
NIMBUS	ARC-150	NYVO
HELIOS	ARC-154	B155
OSCAR-6	PRC-85	M-56
PIONEER F	STINGER	XM-70
ATS	CAPTOR	ADAM
IMP SATELLITES	MANPACK	FMU 112B
MJS-77 (MARINER-JUPITER-SATURN)	SKIRU	FMU 117B
CTS	AN/ALE 139	ROLAND MISSILE
IUS	DMD/PLARS	BISS
VELA	AFSCS	PAY PENNY
DMSP	COPPER HEAD	GEMSS
IUS	PTARMIGAN	SEELEY
ISPM	LOW CALS-HELLFIRES	REMBASS
GALILEO	CLC	GPS
MAGSAT	CUTTYSARK	NAVY 5" GP
ISEES	F-15	AEGIS
DYNAMIC EXPLORER	G-16	PRC 77
ASTRO C	DMD	PRC 25
MILSTAR	MSC64	SAM-D
GPS	XM-12	BULL-DOG
FLEET SATCOM	TRIDENT	CONDOR
PIONEER/VENUS	MAYBERRY	NIKE X
AIRS	SINCGARS	PEWS
TIROS	MILES	FALCON
ISSP	VALLOR	KG 84
HEART PACERS	SPARROW	B1 BOMBER
CUSTOM DEVICES	MOPMS	
HS250	BCS	
	SCATTERABLE MINE	

Reliability Data

JAN Qualification Test Data

The table below contains recent qualification test data for JAN product radiation resistance to 1 x 10^5 rads (Si). Data is presented for the cerdip package and specific types on the QPL list for Class B product. The table shows reliability figures generated for life tests performed at 135°C for 500 hours versus 125°C for 1000 hours using the new regression table of Method 1005 of MIL-STD-883C. The figures show that approximately the same reliability is experienced at 135°C when acceleration factors are used to arrive at a 55°C operating temperature, a failure rate of 0.0012 to 0.0014%/1000 hours. All rejects experienced were degradation, not functional, showing excellent reliability for JAN product.

JAN Class B Qualification Test Data for CD4000B-Series Rad-Hard to 10^5 Rads (Si)

38510/	Type	Temp °C	Hrs.	Tested	Rejects	Device Hrs.
5255	CD4001BF	135	528.8	82	1	43,033
5052	CD4012BF	135	582.5	82	1	47,765
5651	CD4017BF	135	553.8	82	0	45,411
5653	CD4020BF	135	544.8	82	0	44,673
17002	CD4082BF	135	672	81	0	54,432
17504	CD4098BF	135	672	82	0	55,104
17403	CD4502BF	135	672	82	1	55,104
Total Number of Hours 345,522 Total Number of Rejects 3 MTTF at 135°C 83 x 10^3 Hrs. Failure Rate at 135°C 1.2%/1000 Hrs. MTTF at 55°C 85 x 10^6 Hrs. Failure Rate at 55°C 0.0012%/1000 Hrs.						
38510/	**Type**	**Temp °C**	**Hrs.**	**Tested**	**Rejects**	**Device Hours**
17001	CD4081BF	125	1000	82	1	82,000
17003	CD4073BF	125	1000	81	0	81,000
17101	CD4071BF	125	1000	82	1	82,000
17102	CD4072BF	125	1000	77	0	77,000
17103	CD4075BF	125	1000	80	0	80,000
17201	CD4085BF	125	1000	78	1	78,000
17202	CD4086BF	125	1000	79	0	79,000
17203	CD4070BF	125	1000	82	1	82,000
17204	CD4077BF	125	1000	82	0	82,000
Total Number of Hours 723,000 Total Number of Rejects 4 MTTF at 125°C 138,000 Hrs. Failure Rate at 125°C 0.72%/1000 Hrs. MTTF at 55°C 68.8 x 10^6 Hrs. Failure Rate at 55°C 0.0014%/1000 Hrs.						

Non-JAN Reliability Data

The next table presents reliability data for Non-JAN CD4000-series A and B product for 1983 at a life-test temperature of 135°C. Three package configurations were evaluated involving numerous CMOS die types. These packages are identified by the last letter in the part description.

K — White Ceramic Flat Pack, Welded Seal
D — White Ceramic Dual-in-Line, Welded Seal
F — Black Ceramic Cerdip, Glass Seal

As noted in the reliability data presented, a failure rate of 0.8%/1000 hours at 135°C was measured for both the CD4000A-series and CD4000B-series devices in any package configuration. Again rejects were degradation only. There were no functional rejects in any of the devices. Failure rates determined at a temperature of 55°C using an activation energy of 1 eV show an excellent reliability rate of 0.00079%/1000 hours.

Reliability Data

Reliability Data for Non-JAN Class S and B CD4000-Series CMOS ICs Rad-Hard to 10^5 Rads (Si) (Life-Test Hours and Failure Rates at 135°C)

CD4000A Series				CD4000B Series			
Type	Sample Size	Rej.	Device Hrs.	Type	Sample Size	Rej.	Device Hrs.
CD4013AK	77	1	38,808	CD4075BK	77	0	38,808
CD4027AK	77	1	38,808	CD4071BK	77	1	38,808
CD4001AK	77	0	38,808	CD4085BK	77	0	38,808
CD4049AK	154	1	77,616	CD4099BK	77	0	38,808
CD4050AK	77	0	38,808	CD4069UBK	77	0	38,808
CD4021AK	77	0	38,808	CD4072BF	77	0	38,808
CD4022AK	77	1	38,808	CD4075BF	77	0	38,808
CD4031AK	77	0	38,808	CD4098BF	77	1	38,808
CD4020AK	77	0	38,808	CD4069UBF	154	1	77,616
CD4019AF	77	0	38,808	CD4052BD	77	0	38,808
CD4050AF	77	0	38,808	CD40174BD	77	0	38,808
CD4013AF	154	0	77,616	CD4518BD	77	0	38,808
CD4021AF	77	0	38,808				
CD4024AF	77	0	38,808				
CD4049AD	77	0	38,808				
Total Number of Hours			659,736	504,504			
Total Number of Rejects			4	3			
Failure Rate at 135°C			0.8	0.82	%/1000 Hrs.		
Failure Rate at 55°C			0.00078	0.00079	%/1000 Hrs.		
MTTF at 135°C			124,000	122,000	Hrs.		
MTTF at 55°C			127,340,000	125,290,00	Hrs.		

Notes:

1. Each device was tested at 504 hours.
2. All rejects were degradation either delta or maximum limit I_{SS}.
3. Failure rates are at a confidence level of 60% at 125°C.
4. Failure rates determined at 55°C are based on an activation energy of 1.0 eV.

The following table shows reliability data for Non-JAN CD4000-series A and B product for 1983 at a life-test temperature of 125°C. The package configuration used here was the white ceramic dual-in-line welded-seal assembly. Again there is no difference in the reliability of the CD4000-series A and B product. Reliability figures are good at 125°C and are excellent when extrapolated down to 55°C using an acceleration factor based on an active energy of 1 eV. Failure rates in the area of 0.0004%/1000 hours were determined which proved MTTF figures shown in the table below.

Reliability Data for Non-JAN Class S CD4000-Series CMOS ICs Rad-Hard to 10^5 Rads (Si) (Life-Test Hours and Failure Rates at 125°C)

CD4000A Series				CD4000B Series			
Type	Sample Size	Rej.	Device Hrs.	Type	Sample Size	Rej.	Device Hrs.
CD4006AD	77	0	77,000	CD4008BD	77	0	77,000
CD4013AD	154	0	154,000	CD4017BD	77	0	77,000
CD4017AD	77	0	77,000	CD4043BD	77	0	77,000
CC4028AD	154	0	154,000	CD4081BD	77	0	77,000
CD4050AD	77	0	77,000	CD40116BD	77	0	77,000
				CD40174BD	77	0	77,000
Total Number of Hours			539,000	462,000			
Total Number of Rejects			0	0			
Failure Rate at 125°C			0.17	0.2	%/1000 Hrs.		
Failure Rate at 55°C			.00034	0.0004	%/1000 Hrs.		
MTTF at 125°C			582,000	500,000	Hrs.		
MTTF at 55°C			290 x 10^6	249 x 10^6	Hrs.		

Notes:

1. Each device was tested for 1000 hours.
2. Failure rates and MTTF were generated at a confidence level of 60%.
3. Failure rates determined at 55°C are based on an activation energy of 1.0 eV.

Reliability Data

In addition, no significant difference is noted in the performance after life testing at 135° C or 125° C. A higher degradation failure rate does occur at 135° C as noted in the table showing life test hours and failure rates at 135° C. However, when acceleration factors are applied, reliability figures of failure rate at 55° C are excellent for both life-test temperatures. Thereafter, the trend in burn-in and life testing is to standardize on the higher 135° C temperature thereby reducing the number of test hours and providing a more effective burn-in and life test, as shown below.

MIL-STD-883C
Regression Burn-in and Life-Test Conditions

	Burn-In Method 1015		Life-Test Method 1005	
	Class S	Class B	Class S	Class B
135°C*	180	120	800	504
125°C	240	160	1000	1000

*RCA standardized method of temperature and time for burn-in and life testing

Field Reliability Data Update

The table below presents an update of field reliability data in which no acceleration factor was used. The most significant updated data is from the Voyager program in which two additional years of operating time from 1980 to 1982 has been accumulated with no more rejects. Also AE/C and D satellites have accumulated two more years of operational data. The resultant reliability failure rate is based on a total of 596,801,000 device hours with only 2 degradation rejects reported.

Field-usage operating-life data on CD4000A family of high-reliability integrated circuits (MIL-STD-883 slash-series types)

Satellite	Oscar-6	ITOS D/F/G/H[1]	Atmosphere Explorer C/D/E[2]	Satcom F1/F2[5]	Voyager 1/2[6]
Time in orbit (months)	32	85.5	121	16.5	52
Number of units	90	168	7200	1652	10346
Device hours	2,073,600	2,585,520	209,880,000	9,812,880	372,450,000
Number of rejects	0	0	0	0	2
Failure rate (%/1000 hrs)[3,4]	0.045	0.035	0.00044	0.0092	0.00042
MTTF (hrs)[3]	2,360,000	2,900,000	225,000,000	10,750,000	122,000,000
Total device hours	596,801,000				
Total failure rate [3,4]	0.00056 %/1000 Hrs.				
Total MTTF hrs[3]	188,000,000				

1. Satellite D orbit time 23 months, F 36 months, G 24 months, H 2.5 months.
2. AE/C orbit time 70 months, AE/D 40 months, AE/E 11 months.
3. Failure rates and MTTF presented at 60 percent one-sided s-confidence level.
4. Operating temperature range 25°C to 125°C; no acceleration factor used.
5. Satcom orbit time: F1, 10 months; F2, 6.5 months.
6. Voyager 1 orbit time is 51 months, Voyager 2 orbit time is 49 months as of Oct. 1982. Program is considered complete as of Oct. 1982.

Radiation Data

RCA Radiation-Hardened Integrated Circuits

Solid-state devices intended for use in applications such as space satellites or military-weapons systems must be able to survive various types of radiation without significant changes in performance characteristics. The damaging types of radiation most likely to be encountered include neutron bombardment, gamma rays, flash x-rays, and electromagnetic pulses (EMP). The following is a discussion of these types of radiation exposure and their effect on integrated circuits.

Neutron radiation can be particularly harmful to discrete or monolithic bipolar transistors. Fast-neutron bombardment can cause displacement of atoms from the silicon crystal lattice; these atoms trap charge carriers and increase the recombination rate of charge-carrier pairs. As a result, the lifetime of minority carriers in bipolar transistor base regions is shortened (causing a decrease in current gain), the collector series resistance rises (causing higher collector saturation voltage), and transistor leakage currents increase. Current gain is affected most rapidly and most critically, and is the chief cause of failure in devices exposed to neutron radiation.

Neutron-displacement damage results primarily in a shortening of minority-carrier lifetime; therefore adverse effects are minimal on MOS transistors (both discrete and monolithic) since they are majority-carrier devices. In fact, CD4000-series CMOS ICs can benefit from the effects of neutron irradiation. RCA offers a special neutron-irradiation option to prevent latch-up. See the Latch-up Protection section.

Gamma Rays are considered ionizing radiation because they normally cause ejection of bound electrons from atoms, freeing them with enough energy to place them into the conduction band. This effect creates what are commonly called "photocurrents." Photocurrents are particularly undesirable in integrated circuits because they form coupling and shorting paths throughout the chip. At large gamma dose rates, the photocurrents can be sufficient to upset logic states and cause latch-up.

Gamma radiation also induces unwanted positive charge in the gate oxide. This occurs when electrons are freed from their bound state, leaving holes that become trapped in the gate oxide. The positive charge accumulates and changes the threshold voltage of the device. The stability of the device threshold voltage is an important factor in determining its total-dose radiation resistance.

RCA uses advanced design, technology and processing techniques to reduce the effects of gamma radiation on its radiation-resistant solid-state devices.

Flash x-rays and electromagnetic pulses produced by a nuclear explosion can cause permanent physical damage to any type of solid-state device. Flash x-rays generate a thermo-mechanical shock that propagates through the dense material (molybdenum, gold, or copper) used for lead connections and for bonding the pellet to the header. At high energy levels (above 10 keV), the shock wave can be strong enough to fracture the pellet. In integrated circuits, the heat generated by absorption of even soft x-rays (with energies of 1 to 10 keV) can melt the gold metallization or the gold eutectic bond used to attach the chip to the header.

Electromagnetic-pulse (EMP) radiation can induce extremely high voltage pulses in the cables used to interconnect electrical equipment. If these voltage pulses exceed the junction-breakdown capability of a solid-state device, they can cause junction avalanching and result in device destruction.

The effects of flash x-rays and EMP radiation cannot be overcome by any changes in device design and processing, but must be treated as system-design problems. The chief weapons used to prevent x-ray or EMP damage are the traditional methods used to combat any RFI: shielding and line-filtering.

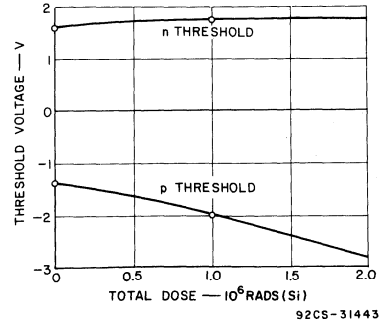
Radiation-Resistant CD4000-Series CMOS ICs

RCA supplies CD4000-series CMOS integrated circuits that are specially processed to be radiation resistant. The following discussion explains how RCA radiation-hardened CD4000-series devices are tested and describes their expected radiation resistance.

Total-Dose Radiation Resistance

Ionizing radiation effects appear at the silicon dioxide-silicon interface. The effects are cumulative and therefore radiation tolerance is characterized in terms of total dose.

Customers most commonly require radiation-hardened devices for space system applications as well as systems intended to survive a nuclear blast. These two environments impose widely different demands on radiation-hardened integrated circuits. A typical dose rate emitted from a Cobalt 60 test chamber is approximately 1 x 10^6 rads (Si) per hour. This high dose rate along with the requirement for rapid electrical parameter evaluation leads to results which are more representative of a nuclear burst rather than that of space environment. Systems in space experience dose rates of about one rad (Si) per hour over a period of perhaps ten years. Because of the low dose rate in space and the simultaneous annealing of the device over a long period of time, radiation-hardened devices in space systems do not experience the parameter shifts measured after Cobalt 60 exposure for radiation verification testing. Therefore, the customary total-dose ratings based on Cobalt 60 testing are considered very conservative for space flight hardware.



Typical threshold-voltage variations of RCA MEGARAD CD4000-series CMOS integrated circuits as a function of total-dose gamma radiation.

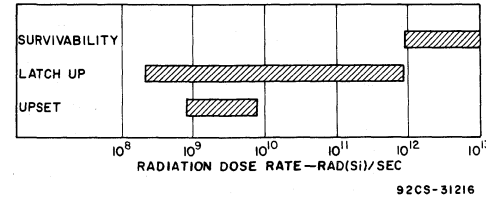
Radiation Data

RCA offers radiation-hardened CD4000-series CMOS integrated circuits tested to withstand total ionizing radiation dosages of 1 x 10^5 rads (Si) — R-suffix types, and 1 x 10^6 rads (Si) — H-suffix types. These radiation tolerances are achieved by special process controls imposed during wafer fabrication.

RCA radiation-hardened R-suffix types may be screened to MIL-M-38510 Class S, and both R-suffix and H-suffix types may be screened to RCA level /MS. The specified levels of radiation resistance are verified per Table V Group E Subgroup 2 of Method 5005 and Method 1019 of MIL-STD-883. Four electrically good packaged samples from each wafer, one from each quadrant, are exposed in a Cobalt 60 source for a time period corresponding to the specified total dose. The samples are then electrically tested within two hours after exposure for threshold voltage, threshold voltage delta, I_{DD} leakage current, and functionality. Propogation delay is also measured for 38510 tested product and may also be measured for DATABOOK tested product if required.

Transient-Radiation Resistance

Samples of CD4000-series devices representing all levels of circuit complexity have been characterized for transient-radiation effects. The data indicates the ranges of occurence of upset, latch-up, and survivability as a function of radiation dose rate.



Effects of transient radiation (10^6 rads (Si) on CD4000-series integrated circuits (aluminum-gate CMOS on bulk silicon).

Radiation-Resistant CD4000-Series CMOS Integrated Circuits

Post-Radiation Test Criteria — Maximum Limits for I_{DD}
(V_{DD} = 18 V for B-Series Types or 15 V for A-Series Types)

Type	I_{DD} (max) μA	Type	I_{DD} (max) μA	Type	I_{DD} (max) μA	Type	I_{DD} (max) μA
CD4000	2.5	CD4035	25	CD4076	25	CD4538	25
CD4001	2.5	CD4040	25	CD4077	2.5	CD4541	25
CD4002	2.5	CD4041	7.5	CD4078	2.5	CD4543	25
CD4006	25	CD4042	7.5	CD4081	2.5	CD4555	25
CD4007	2.5	CD4043	7.5	CD4082	2.5	CD4556	25
CD4008	25	CD4044	7.5	CD4085	2.5	CD4585	25
CD4009	7.5	CD4045	25	CD4086	2.5	CD4724	25
CD4010	7.5	CD4046	25	CD4089	25	CD40100	25
CD4011	2.5	CD4047	25	CD4093	7.5	CD40101	25
CD4012	2.5	CD4048	7.5	CD4094	25	CD40102	25
CD4013	7.5	CD4049	7.5	CD4095	7.5	CD40103	25
CD4014	25	CD4050	7.5	CD4096	7.5	CD40104	25
CD4015	25	CD4051	25	CD4097	25	CD40105	25
CD4016	2.5	CD4052	25	CD4098	7.5	CD40106	7.5
CD4017	25	CD4053	25	CD4099	25	CD40107	7.5
CD4018	25	CD4057	25	CD4502	7.5	CD40108	25
CD4019	7.5	CD4059	25	CD4503	7.5	CD40109*	7.5
CD4020	25	CD4060	25	CD4508	25	CD40147	25
CD4021	25	CD4061	25	CD4510	25	CD40160	25
CD4022	25	CD4062	25	CD4511	25	CD40161	25
CD4023	2.5	CD4063	25	CD4512	25	CD40162	25
CD4024	25	CD4066	2.5	CD4514	25	CD40163	25
CD4025	2.5	CD4067	25	CD4515	25	CD40174	7.5
CD4026	25	CD4068	7.5	CD4516	25	CD40175	7.5
CD4027	7.5	CD4069	2.5	CD4517	25	CD40181	25
CD4028	25	CD4070	2.5	CD4518	25	CD40182	25
CD4029	25	CD4071	2.5	CD4520	25	CD40192	25
CD4030	7.5	CD4072	2.5	CD4527	25	CD40193	25
CD4031	25	CD4073	2.5	CD4532	25	CD40194	25
CD4032	25	CD4075	2.5	CD4536	25	CD40208	25
CD4033	25					CD40257	7.5
CD4034	25						

Post-Radiation Threshold-Voltage Test Criteria
(V_{DD} = 10 V; I = constant 10 μA)

N Threshold = 0.2 V min. P Threshold = 2.8 V max. ΔN Threshold = 1.0 V max. ΔP Threshold = 1.0 V max.
*P Threshold = 3.5 V max. CD40109 only.

Radiation Data

Transient upset is a change in the logic state of a device due to radiation exposure. Transient ionizing radiation causes photocurrents which tend to charge and discharge nodes of the integrated circuit and may cause logic upset. If the incorrect output state of a device only lasts for the duration of the radiation pusle, the momentary disturbance is called temporary upset.

Latch-up occurs because of the presence of inherent bipolar SCR structures in bulk CMOS devices. In normal operation, the parasitic bipolar SCR remains inactive. The device is said to be in the latch-up state when the parasitic SCR structures become activated, thereby creating a low-impedance path from V_{DD} to V_{SS}. In the "ON" condition, the SCR can conduct heavily at low voltages. Latch-up may be induced by the resulting photocurrents of high-intensity transient ionizing radiation or by applying excessive voltage. Once turned on, the SCR can be rendered dormant again only by removing the power supply. Burn-out of the device may result if the current is not limited in some way.

The region of occurrence of the latch condition in CMOS ICs under high-intensity transient radiation is quite wide. Only two known device types latch below the 1×10^9-rad (Si)/sec level. A significant number of device types do not latch above dose rates of 1×10^{11} rads (Si)/sec.

The occurrence of latch-up can be prevented by means of neutron irradiation. See the Latch-up Protection section.

Survivability level is the maximum transient-radiation level at which damage does not occur. Above this level photocurrents are created to the extent that excessive dissipation is caused, resulting in permanent damage to the device.

Latch-Up Protection

Latch-up protection in CMOS devices can be achieved by taking advantage of the effects of neutron irradiation. Neutron irradiation will reduce minority-carrier lifetime which, in turn, attenuates the current gains, or betas, of bipolar transistors. To turn on the SCR structure of CMOS devices, it is necessary for the beta product of its bipolar transistors to be greater than unity. Neutron irradiation can reduce the beta product to less than unity. Since CMOS transistors are majority-carrier devices, normal CMOS performance is generally unaffected by neutron irradiation. Therefore, neutron irradiation is a suitable method for precluding latch-up in CMOS devices. In addition, neutron-irradiated CMOS devices are less susceptible to logic upset due to transient radiation.

RCA offers custom CD4000-series devices which are made from wafers that are exposed to a neutron fluence of approximately 1×10^{14} n/cm^2. After neutron irradiation, wafers can be assembled and screened to all requirements of the RCA /MS level product. Product yields remain high and all of RCA's DATABOOK electrical parameters are well within specification.

Radiation-Resistant CD4000B-Series Types for Project GALILEO.

RCA supplied fifty types of radiation-resistant CD4000B-Series CMOS ICs for the Project GALILEO Spacecraft program. This program was carried out for JPL and NASA during 1979 through 1981. A total of 33,000 parts, covering the fifty CD4000B-series types, were provided. These parts were screened to criteria that exceeded Class S requirements. Mounted devices from each wafer were tested for a total radiation resistance of 1,000,000 rads (Si). Sample quantities of each of the 50 types were subjected to a 2000-hour life test with excellent results.

RCA has provided several hundred thousand CD4000A- and B-series device types to 100,000 and 1,000,000 rads (Si) on a number of programs. Voyager 1 and 2 satellites, DMSP, TRIOS, Block 5, and VJ930 programs used these devices. RCA is providing neutron-irradiated devices on a number of military programs during 1985 and 1986 that have the 1,000,000-rads (Si) requirement.

High-Reliability QMOS 54HC/HCT Slash-Series CMOS ICs

The 54/HC/HCT High-Reliability Product Line

The RCA QMOS 54HC/HCT series of high-speed CMOS logical integrated circuits include an extensive line of products that are pin compatible with many existing bipolar 54LSTTL and CMOS 4000 series of digital logic types. The new 54HC/HCT IC's provide high-speed CMOS replacements for the most popular LSTTL devices in existing designs and also offer low-power all-CMOS designs for new digital systems. Key family features of the RCA 54HC/HCT types include:

- Speeds equivalent to LSTTL types with typical gate delays of 10 ns.
- Fanout to 10 54-LSTTL loads; 15 loads using Bus Driver 54 types.
- Operating frequencies equivalent to LSTTL types, typically 30 MHz.
- The high-voltage noise-immunity characteristic of CMOS, typically 45 percent of V_{CC}, a two to three times improvement over LSTTL.
- Wide range of power supply operating voltages, 2 to 6 volts.
- CMOS low static power consumption, typically less than 1 microwatt.

With the broad line of CMOS MSI-function types currently available, together with performance offered by the RCA 54HC/HCT series of high-speed CMOS integrated circuits, the designer need not sacrifice speed for power consumption. Add the other classical advantages of CMOS, including high noise immunity and wide power-supply and temperature ranges, and the decision to use high-speed CMOS logic is the choice for the 80's. This new family provides for the design of more cost-effective systems to serve high-speed market applications.

The RCA 54HC/HCT high-reliability product line consists primarily of CD54HC-series types, which feature CMOS input-voltage-level compatibility, and CD54HCT-series types, which are input-voltage-level compatible with LSTTL devices. The 54HC/HCT high-reliability line also includes a limited number of single-stage, unbuffered inverter types (CD54HCU-series) for added versatility in oscillator and amplifier applications. The following paragraphs outline some key advantages that 54HC/HCT high-reliability IC's offer over standard CMOS and LSTTL types.

Power Consumption

CMOS is well established in the marketplace as the leading technology for applications in which low power consumption is a prime requisite. Relative to LSTTL, CMOS IC's feature low static power dissipation or heat generation. In comparison to 54 series LSTTL types, RCA 54HC/HCT devices enhance system reliability and reduce costs by reducing, or eliminating, the number and size of parts such as heat sinks, fans, tightly regulated high-current power supplies, and copper busses. A typical system in which LSTTL types have been replaced by equivalent 54HC/HCT types can be expected to operate with only 1% of the power, assuming that all logic nodes are switched at an average rate of 10 KHz. Although some 54HC/HCT logic nodes may switch at speeds greater than 10 MHz, it's the over-all duty cycle and average switching rate that counts. This average switching is the key to the advantage of CMOS low power. For LSTTL, the high dc current dominates.

Noise Immunity Considerations

The noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation, and layout rules for PC boards and signal cables. A true system assessment of noise immunity is the noise margin provided by a logic family. The table shown below illustrates the superior (2:1) system noise margin of the CD54HC series over the 54LSTTL series. The system noise margin of CD54HCT series is similar to that of the 54LSTTL series.

Table III — 54LSTTL and CD54HC Family Input, Output, And Noise Margin Voltage (V_{CC} = 5V)

Parameter	54LSTTL Series	CD54HC Series
V_{IL}	0.8 V	1 V
V_{IH}	2 V	3.5 V
V_{OH}	2.7 V	4.9 V
V_{OL}	0.4 V	0.1 V
$V_{NML} = V_{IL} - V_{OL}$ (Noise Margin LOW)	0.4 V	0.9 V
$V_{NMH} = V_{OH} - V_{IH}$ (Noise Margin High)	0.7 V	1.4 V

AC Performance

In comparison to standard CD4000-Series CMOS, LSTTL types provide higher operating frequencies as well as considerably shorter propagation delays. The RCA 54HC/HCT high-speed logic series is designed to meet the dynamic switching speeds and operating frequency of LSTTL. This new series, therefore, offers a higher-performance family of low-power logic products that should be widely accepted in computer and communication applications and for other uses that require fast switching speed.

Output Drives

A prominent characteristic of LSTTL is its restrictive output drive capacity, or fanout rules. Each basic logic type in the RCA 54HC/HCT High-Speed CMOS series is capable of driving a full complement of 10 LSTTL loads (4mA at 0.4 V). An additional factor of 50% was applied to parts in the octal grouping for a total bus driving capability of 6 mA or a fanout of 15 LSTTL loads. These improved drive capabilities are achieved without sacrifice of the power, speed, and noise-immunity benefits of the CMOS family. For driving 54HC/HCT loads, a fanout of 20 at high noise margin is specified. This fanout capability is twice that of standard 74LSTTL. Much higher fanout capability exists for 54HC/HCT types, but speed and noise margin are reduced.

The 54/HC/HCT High-Reliability Product Line

High-Speed CMOS Generic Type, DESC and JAN Device Cross Reference

Generic Number 54HC-	DESC-Dwg. Number	Military Specification MIL-M-38510/	Generic Number 54HC-	DESC-Dwg. Number	Military Specification MIL-M-38510/
00	84037	65001	243	84090	65502
02	84041	65101	244	84096	65705
04	84098	65701	245	84085	65503
08	84047	65203	251	—	66205
10	84038	65002	253	—	66206
11	84048	65204	257	—	66207
14	84091	65702	259	—	65402
20	84039	65003	273	84099	65601
27	84042	65102	280	—	66801
30	84040	65004	283	—	66701
32	84045	65201	299	—	66506
42	—	65801	354	—	66208
73	—	65301	356	—	66209
74	84056	65302	365	85001	65706
75	84070	65401	366	—	65707
85	—	66101	367	85002	65708
86	84046	65202	368	—	65709
107	—	65303	373	84072	65403
109	84150	65304	374	84071	65602
112	84088	65305	377	—	65603
123	—	65901	390	—	66308
132	—	65005	393	84100	66309
138	84062	65802	533	—	65404
139	84092	65803	534	—	65605
147	84064	66001	540	—	65710
151	—	66201	541	—	65711
153	84093	66202	563	—	65405
154	—	65804	564	—	65606
157	—	66203	573	—	65406
158	—	66204	574	—	65604
160	—	66301	597	—	66508
161	84075	66302	640	—	65506
162	84094	66303	643	—	65507
163	—	66304	646	—	65508
164	84162	66501	648	—	65509
165	84095	66502	670	—	66601
166	—	66503	688	—	66105
173	—	65306	4002	84044	65104
174	84073	65307	4017	—	66310
175	84089	65308	4020	85003	66311
191	—	66305	4024	—	66312
192	—	66306	4040	85004	66313
193	—	66307	4049	—	65712
194	—	66504	4050	—	65713
195	—	66505	4520	—	66314
221	—	65902			
238	—	65805			
240	84074	65703			
241	—	65704			
242	—	65501			

Function Selection Guide

Type	Function/Description	No. of Pins
	NAND/NOR Gates	
CD54HC/HCT00	Quad 2-Input NAND Gate	14
CD54HC/HCT02	Quad 2-Input NOR Gate	14
CD54HC/HCT03	Quad 2-Input NAND Gate with Open Collector	14
CD54HC/HCT10	Triple 3-Input NAND Gate	14
CD54HC/HCT20	Dual 4-Input NAND Gate	14
CD54HC/HCT27	Triple 3-Input NOR Gate	14
CD54HC/HCT30	8-Input NAND Gate	14
CD54HC/HCT4002	Dual 4-Input NOR Gate	14
	AND/OR/EXCLUSIVE-OR Gates	
CD54HC/HCT08	Quad 2-Input AND Gate	14
CD54HC/HCT11	Triple 3-Input AND Gate	14
CD54HC/HCT21	Dual 4-Input AND Gate	14
CD54HC/HCT32	Quad 2-Input OR Gate	14
CD54HC/HCT86	Quad 2-Input EXCLUSIVE-OR Gate	14
CD54HC/HCT4075	Triple 3-Input OR Gate	14
CD54HC7266	Quad Exclusive NOR Gate	16
	Inverters/Buffers/Bus Drivers	
CD54HC/HCT04	Hex Inverter	14
CD54HCU04	Hex Inverter (Unbuffered)	14
CD54HC/HCT125	Quad 3-State Buffer	14
CD54HC/HCT126	Quad 3-State Buffer	14
CD54HC/HCT240*	Octal Buffer/Line Driver; 3-State; Inverting	20
CD54HC/HCT241*	Octal Buffer/Line Driver; 3-State	20
CD54HC/HCT244*	Octal Buffer/Line Driver; 3-State	20
CD54HC/HCT365*	Hex Buffer/Line Driver; 3-State	16
CD54HC/HCT366*	Hex Buffer/Line Driver; 3-State Inverting	16
CD54HC/HCT367*	Hex Buffer/Line Driver; 3-State	16
CD54HC/HCT368*	Hex Buffer/Line Driver; 3-State; Inverting	16
CD54HC/HCT540*	Octal Buffer/Line Driver; 3-State; Inverting	20
CD54HC/HCT541*	Octal Buffer/Line Driver; 3-State	20
CD54HC4049	Hex Inverting High-to-Low-Level Shifter	16
CD54HC4050	Hex High-to-Low-Level Shifter	16
	Flip-Flops/Latches/Registers	
CD54HC/HCT73	Dual JK Flip-Flop with Reset; Negative-Edge Trigger	14
CD54HC/HCT74	Dual D-Type Flip-Flop with Set and Reset; Positive-Edge Trigger	14
CD54HC/HCT107	Dual JK Flip-Flop with Reset; Negative-Edge Trigger	14
CD54HC/HCT109	Dual JK Flip-Flop with Set and Reset; Positive-Edge Trigger	16
CD54HC/HCT112	Dual JK Flip-Flop with Set and Reset; Positive-Edge Trigger; 3-State	16
CD54HC/HCT173*	Quad D-Type Flip-Flop with Set and Reset; Positive-Edge Trigger; 3-State	16
CD54HC/HCT174	Hex D-Type Flip-Flop with Reset; Positive-Edge Trigger	16
CD54HC/HCT175	Quad D-Type Flip-Flop with Reset; Positive-Edge Trigger	16
CD54HC/HCT273	Octal D-Type Flip-Flop with Set and Reset; Positive-Edge Trigger	20
CD54HC/HCT374*	Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State	20
CD54HC/HCT377	Octal D-Type Flip-Flop with Data Enable; Positive-Edge Trigger	20
CD54HC/HCT534*	Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State; Inverting	20
CD54HC/HCT564*	Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State; Inverting	20
CD54HC/HCT574*	Octal D-Type Flip-Flop; Positive-Edge; 3-State	20
	Shift/FIFO Buffer/Multiport Registers	
CD54HC/HCT164	8-Bit Serial-In/Parallel-Out Shift Register	14
CD54HC/HCT165	8-Bit Parallel-In/Serial-Out Shift Register	16
CD54HC/HCT166	8-Bit Parallel/Serial-In Serial-Out Shift Register	16
CD54HC/HCT194	4-Bit Bidirectional Universal Shift Register	16
CD54HC/HCT195	4-Bit Parallel Access Shift Register	16
CD54HC/HCT299*	8-Bit Universal Shift Register; 3-State	20
CD54HC/HCT597	8-Bit Shift Register with Input Latch	16
CD54HC/HCT670	4 x 4 Register File; 3-State	16
CD54HC/HCT4015	Dual 4-Bit Serial-In/Parallel-Out Shift Register	16
CD54HC/HCT4094	8-State Shift-and-Store Bus Register	16

*Types with bus driver output stage

Function Selection Guide

Type	Function/Description	No. of Pins
	Shift/FIFO Buffer/Multiport Registers (Cont'd)	
CD54HC/HCT40104*	4-Bit Bidirectional Universal Shift Register; 3-State	16
CD54HC/HCT40105	4 Bit x 16 Word FIFO Register	16
	Phase-Locked Loop	
CD54HC/HCT7046	Phase Locked Loop with In-Lock Detection	16
	Arithmetic Circuits	
CD54HC/HCT85	4-Bit Magnitude Comparator	16
CD54HC/HCT181	ALU	24
CD54HC/HCT182	Carry Generator	16
CD54HC/HCT280	9-Bit Odd/Even Parity Generator/Checker	14
CD54HC/HCT283	4-Bit Full Adder With Fast Carry	16
CD54HC/HCT583	4-Bit Full-Adder With Fast Carry	16
CD54HC/HCT688	8-Bit Magnitude Comparator	20
	Counters	
CD54HC/HCT93	4-Bit Binary Ripple Counter	14
CD54HC/HCT160	Presettable Synchronous BCD Decade Counter; Asynchronous Reset	16
CD54HC/HCT161	Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset	16
CD54HC/HCT162	Presettable Synchronous BCD Decade Counter; Synchronous Reset	16
CD54HC/HCT163	Presettable Synchronous 4-Bit Binary Counter; Synchronous Reset	16
CD54HC/HCT190	Presettable Synchronous BCD Decade Up/Down Counter	16
CD54HC/HCT191	Presettable Synchronous 4-Bit Binary Up/Down Counter	16
CD54HC/HCT192	Presettable Synchronous BCD Decade Up/Down Counter	16
CD54HC/HCT193	Presettable Synchronous 4-Bit Binary Up/Down Counter	16
CD54HC/HCT390	Dual Decade Ripple Counter	16
CD54HC/HCT393	Dual 4-Bit Binary Ripple Counter	14
CD54HC/HCT4017	Johnson Decade Counter with 10 Decoded Outputs	16
CD54HC/HCT4020	14-Stage Binary Ripple Counter	16
CD54HC/HCT4024	7-Stage Binary Ripple Counter	14
CD54HC/HCT4040	12-Stage Binary Ripple Counter	16
CD54HC/HCT4059	Programmable Divide-by-"N" Counter	24
CD54HC/HCT4060	14-Stage Binary Ripple Counter with Oscillator	16
CD54HC/HCT4510	Presettable Synchronous 4-Bit BCD Up/Down Counter	16
CD54HC/HCT4516	Presettable Synchronous 4-Bit Binary Up/Down Counter	16
CD54HC/HCT4518	Dual Synchronous BCD Counter	16
CD54HC/HCT4520	Dual 4-Bit Synchronous Binary Counter	16
CD54HC/HCT40102	8-Bit Synchronous BCD Down Counter	16
CD54HC/HCT40103	8-Bit Binary Down Counter	16
	Analog and Digital Multiplexers/Demultiplexers	
CD54HC/HCT151	8-Input Multiplexer	16
CD54HC/HCT153	Dual 4-Input Multiplexer	16
CD54HC/HCT157	Quad 2-Input Multiplexer	16
CD54HC/HCT158	Quad 2-Input Multiplexer; Inverting	16
CD54HC/HCT251	8-Input Multiplexer; 3-State	16
CD54HC/HCT253	Dual 4-Input Multiplexer; 3-State	16
CD54HC/HCT257*	Quad 2-Input Multiplexer; 3-State	16
CD54HC/HCT258	Quad 2-Line to 4-Line Data Selector	16
CD54HC/HCT354*	8-Input Multiplexer/Register; 3-State	20
CD54HC/HCT356	8-Input Multiplexer/Register; 3-State	20
CD54HC/HCT4051	8-Channel Analog Multiplexer/Demultiplexer	16
CD54HC/HCT4052	Dual 4-Channel Analog Multiplexer/Demultiplexer	16
CD54HC/HCT4053	Triple 2-Channel Analog Multiplexer/Demultiplexer	16
CD54HC/HCT4067	16-Channel Analog Multiplexer/Demultiplexer	24
CD54HC/HCT4316	Quad Analog Switch	16
CD54HC/HCT4351	Analog Multiplexer with Latch	20
CD54HC/HCT4352	Analog Multiplexer with Latch	20
CD54HC/HCT4353	Analog Multiplexer with Latch	20

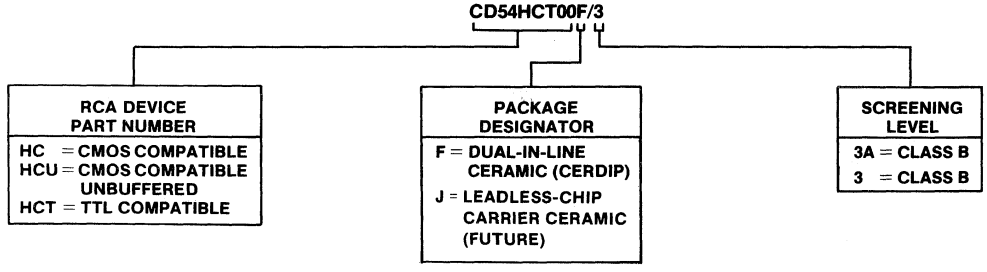
*Types with a bus driver output stage.

Function Selection Guide

Type	Function/Description	No. of Pins
	Decoders/Encoders	
CD54HC/HCT42	BCD-to-Decimal Decoder (1-to-10)	16
CD54HC/HCT137	3-to-8-Line Decoder with Latch, Inverting	16
CD54HC/HCT138	3-to-8-Line Decoder/Demultiplexer; Inverting	16
CD54HC/HCT139	Dual 2-to-4-Line Decoder/Demultiplexer	16
CD54HC/HCT147	10-to-4-Line Priority Encoder	16
CD54HC/HCT154	4-to-16-Line Decoder/Demultiplexer	24
CD54HC/HCT237	3-to-8-Line Decoder	16
CD54HC/HCT238	3-to-8-Line Decoder/Demultiplexer	16
CD54HC/HCT4511	BCD-to-7-Segment Latch/Decoder/Driver	16
CD54HC/HCT4514	4-to-16-Line Decoder/Demultiplexer with Input Latches	24
CD54HC/HCT4515	4-to-16-Line Decoder/Demultiplexer with Input Latches	24
CD54HC/HCT4543	BCD-to-7-Segment Latch/Decoder/Driver for LCDs	16

*Types with bus driver output stage.

Guide to the Reliability Class and Package of RCA High Reliability 54HC/HCT Integrated Circuits



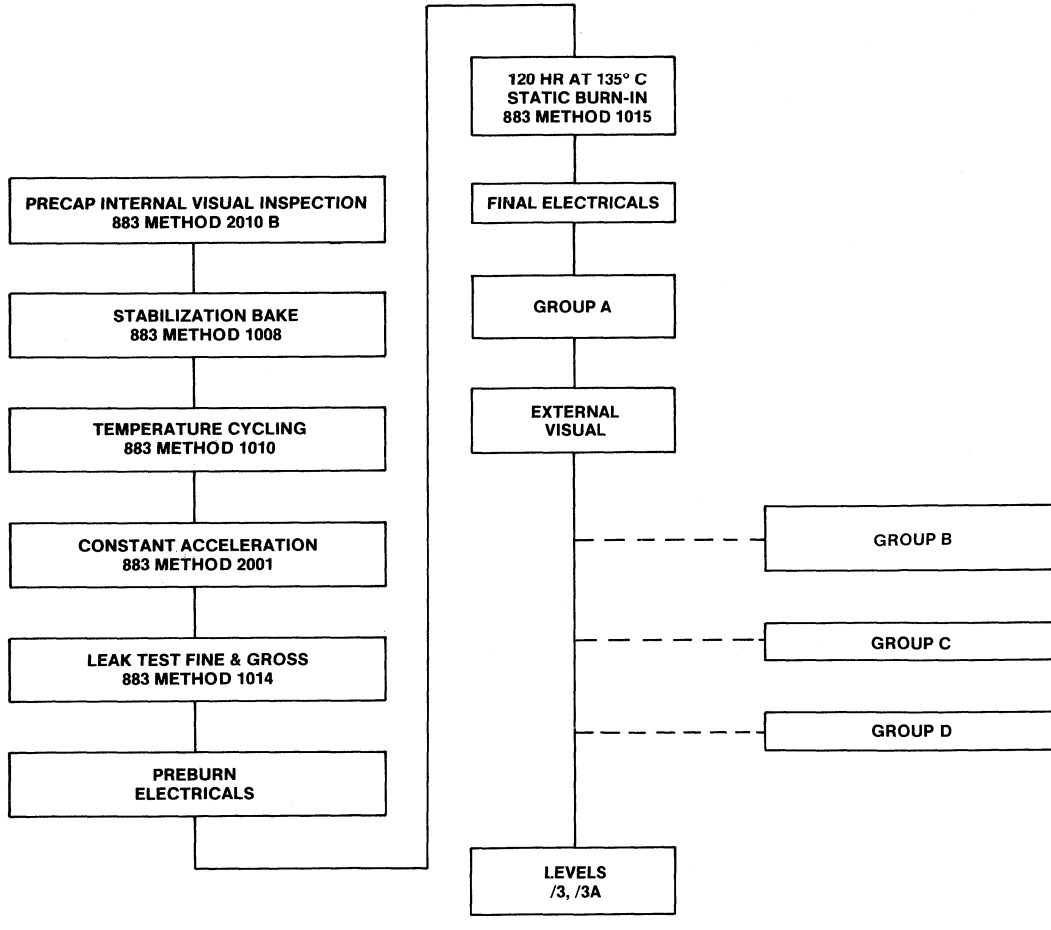
Screening and Conformance Testing

Screening Levels

Screening Levels†		Application	Description
For Packaged Devices (F Suffix)			
/3A	Class B	Military and Industrial For example, in Airborne Electronics	For devices intended for use where maintenance and replacement can be performed but are difficult and expensive.
/3	Class B, Modified		
For Chips (H Suffix)			
/M	Condition B Precap Visual inspection	Military and Industrial	For general applications

†For screening details, refer to Total Lot Screening Chart. Refer to 54HC/HCT-Series manufacturing and conformance testing table for descriptions of levels /3A and /3.

Product Flow Diagram



RCA HIGH-RELIABILITY LEVEL /3 AND /3A 54HC/HCT IC'S

Screening and Conformance Testing

Total Lot Screening (X = 100% Testing)

Screening Tests	Conditions	MIL-STD-883 Method	MIL-STD-883 Conditions	Screening Levels /3, /3A	Notes
Assembly					
Precap Visual		2010	B	X	
Preconditioning					
Stabilization Bake	24 hrs. min. at 150°C	1008	C	X	
Temperature Cycling	10 Cycles	1010	C	X	
Centrifuge	Y_1 direction only	2001	E	X	
Fine Leak	—	1014	A or B	X	
Gross Leak	—	1014	C	X	
Test and Burn-in					
Initial Test	—	—	—	X	
Static Burn-in	120 hrs. @ 135°C	1015	B	X	1
Final Electrical					
Static Electrical (DC)	25°C	—	—	X	2, 3
	-55°C	—	—	X	
	125°C	—	—	X	
Dynamic Electrical (AC)	25°C	—	—	X	
Group A	—	—	X	X	4

Notes:

1. Alternate time/temperature regression used per Method 1015.
2. All electrical testing per parameters shown in individual device data sheets.
3. PDA = 5%, one reburn allowed at 3%.
4. Sample test performed per Method 5005 of MIL-STD-883.

Manufacturing and Conformance Testing

Characteristic	/3A[1]	/3[2]
SERIES	HC, HCT, HCU	HC, HCT, HCU
PACKAGE	F	F
DIE ATTACH	EUTECTIC	GLASS
LEAD FINISH	MATTE TIN REFLOWED	MATTE TIN
MANUFACTURING LOCATION	OFF-SHORE	OFF-SHORE
SCREENING	METHOD 5004	METHOD 5004
CONFORMANCE TESTS		
GROUP A	METHOD 5005	YES
CLASS B, GROUP B	METHOD 5005	GENERIC[3]
CLASS B, GROUP C	METHOD 5005	GENERIC[3]
GROUP D	METHOD 5005	GENERIC[3]
DATA SUPPLIED		
C OF C[5]	YES	YES

NOTES:

1. Slash 3A meets MIL-STD-883 Class B.
2. Slash 3 meets MIL-STD-883 Class B less tin reflow.
3. Conformance tests are not run on a continuous basis, but available generic data can be provided upon request.
4. For Slash 3A Series, Group B will be run on each inspection lot representing 6 weeks of product.
5. Certificate of compliance (C of C) signed by RCA representative provides identity and customer order number, and lists and certifies tests, methods and conditions per MIL-STD-883. No variables or attributes data supplied.

Ratings and Characteristics

RCA Standardized Maximum Ratings and Recommended Operating Conditions

MAXIMUM RATINGS, *Absolute Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7V
DC INPUT VOLTAGE RANGE, ALL INPUTS (V_{IN}) ..... -0.5 to V_{CC} + 0.5V
DC OUTPUT VOLTAGE RANGE, ALL OUTPUTS (V_{OUT}) ..... -0.5 to V_{CC} + 0.5V
CLAMP DIODE CURRENT, PER PIN (I_K) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_{OUT}):
STANDARD OUTPUT ..... ±25 mA
BUS DRIVER OUTPUT ..... ±35 mA
DC V_{CC} or GROUND CURRENT, PER PIN (I_{CC}):
STANDARD OUTPUT ..... ±50 mA
BUS DRIVER OUTPUT ..... ±70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to + 100°C (PACKAGE TYPE F) ..... 500 mW
For T_A = + 100 to + 125°C (PACKAGE TYPE F) ..... Derate Linearly at 12 mW/°C to 200 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F ..... -55 to + 125°C
STORAGE TEMPERATURE (T_{stg}) ..... -66 to + 150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max. ..... + 300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}*			
CD54HC Types	2	6	V
CD54HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A	-55	+125	° C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

Ratings and Characteristics

Classification According to Circuit Complexity

CMOS LOGIC	TTL LOGIC
SSI	
CD54HC00	CD54HCT00
CD54HC02	CD54HCT02
CD54HC03	CD54HCT03
CD54HC04	CD54HCT04
CD54HCU04	—
CD54HC08	CD54HCT08
CD54HC10	CD54HCT10
CD54HC11	CD54HCT11
CD54HC14	CD54HCT14
CD54HC20	CD54HCT20
CD54HC21	CD54HCT21
CD54HC27	CD54HCT27
CD54HC30	CD54HCT30
CD54HC32	CD54HCT32
CD54HC86	CD54HCT86
CD54HC132	CD54HCT132
CD54HC4002	CD54HCT4002
CD54HC4016	CD54HCT4016
CD54HC4049	—
CD54HC4050	—
CD54HC4066	CD54HCT4066
CD54HC4075	CD54HCT4075
CD54HC7266	—
FF	
CD54HC73	CD54HCT73
CD54HC74	CD54HCT74
CD54HC75	CD54HCT75
CD54HC107	CD54HCT107
CD54HC109	CD54HCT109
CD54HC112	CD54HCT112
MSI	
CD54HC42	CD54HCT42
CD54HC85	CD54HCT85
CD54HC93	CD54HCT93
CD54HC123	CD54HCT123
CD54HC125	CD54HCT125
CD54HC126	CD54HCT126
CD54HC137	CD54HCT137
CD54HC138	CD54HCT138
CD54HC139	CD54HCT139
CD54HC147	CD54HCT147
CD54HC151	CD54HCT151
CD54HC153	CD54HCT153
CD54HC154	CD54HCT154
CD54HC157	CD54HCT157
CD54HC158	CD54HCT158

CMOS LOGIC	TTL LOGIC
MSI	
CD54HC160	CD54HCT160
CD54HC161	CD54HCT161
CD54HC162	CD54HCT162
CD54HC163	CD54HCT163
CD54HC164	CD54HCT164
CD54HC165	CD54HCT165
CD54HC166	CD54HCT166
CD54HC173*	CD54HCT173*
CD54HC174	CD54HCT174
CD54HC175	CD54HCT175
CD54HC181	CD54HCT181
CD54HC182	CD54HCT182
CD54HC190	CD54HCT190
CD54HC191	CD54HCT191
CD54HC192	CD54HCT192
CD54HC193	CD54HCT193
CD54HC194	CD54HCT194
CD54HC195	CD54HCT195
CD54HC221	CD54HCT221
CD54HC237	CD54HCT237
CD54HC238	CD54HCT238
CD54HC240*	CD54HCT240*
CD54HC241*	CD54HCT241*
CD54HC242*	CD54HCT242*
CD54HC243*	CD54HCT243*
CD54HC244*	CD54HCT244*
CD54HC245*	CD54HCT245*
CD54HC251	CD54HCT251
CD54HC253	CD54HCT253
CD54HC257*	CD54HCT257*
CD54HC258	CD54HCT258
CD54HC259	CD54HCT259
CD54HC273	CD54HCT273
CD54HC280	CD54HCT280
CD54HC283	CD54HCT283
CD54HC297	CD54HCT297
CD54HC299*	CD54HCT299*
CD54HC354*	CD54HCT354*
CD54HC356*	CD54HCT356*
CD54HC365*	CD54HCT365*
CD54HC366*	CD54HCT366*
CD54HC367*	CD54HCT367*
CD54HC368*	CD54HCT368*
CD54HC373*	CD54HCT373*
CD54HC374*	CD54HCT374*
CD54HC377	CD54HCT377
CD54HC390	CD54HCT390

CMOS LOGIC	TTL LOGIC
MSI	
CD54HC393	CD54HCT393
CD54HC423	CD54HCT423
CD54HC533*	CD54HCT533*
CD54HC534*	CD54HCT534*
CD54HC540*	CD54HCT540*
CD54HC541*	CD54HCT541*
CD54HC563*	CD54HCT563*
CD54HC564*	CD54HCT564*
CD54HC573*	CD54HCT573*
CD54HC574*	CD54HCT574*
CD54HC583	CD54HCT583
CD54HC597	CD54HCT597
CD54HC640*	CD54HCT640*
CD54HC643*	CD54HCT643*
CD54HC646*	CD54HCT646*
CD54HC648*	CD54HCT648*
CD54HC670	CD54HCT670
CD54HC688	CD54HCT688
CD54HC4015	CD54HCT4015
CD54HC4017	CD54HCT4017
CD54HC4020	CD54HCT4020
CD54HC4024	CD54HCT4024
CD54HC4040	CD54HCT4040
CD54HC4046	CD54HCT4046
CD54HC4051	CD54HCT4051
CD54HC4052	CD54HCT4052
CD54HC4053	CD54HCT4053
CD54HC4059	CD54HCT4059
CD54HC4060	CD54HCT4060
CD54HC4067	CD54HCT4067
CD54HC4094	CD54HCT4094
CD54HC4316	CD54HCT4316
CD54HC4351	CD54HCT4351
CD54HC4352	CD54HCT4352
CD54HC4353	CD54HCT4353
CD54HC4510	CD54HCT4510
CD54HC4511	CD54HCT4511
CD54HC4514	CD54HCT4514
CD54HC4515	CD54HCT4515
CD54HC4516	CD54HCT4516
CD54HC4518	CD54HCT4518
CD54HC4520	CD54HCT4520
CD54HC4538	CD54HCT4538
CD54HC4543	CD54HCT4543
CD54HC7046	CD54HCT7046
CD54HC40102	CD54HCT40102
CD54HC40103	CD54HCT40103
CD54HC40104*	CD54HCT40104*
CD54HC40105	CD54HCT40105

*Types with a bus driver output stage.

Ratings and Characteristics

Static Electrical Characteristics for CD54HC Types

Characteristics	Test Conditions				CD54HC Series				Units
	V_{IN} V			V_{CC} V	+25°C		-55/+125°C		
					Min.	Max.	Min.	Max.	
High-Level Input Voltage V_{IH}				2	1.5	—	1.5	—	V
				4.5	3.15•	—	3.15•	—	
				6	4.2	—	4.2	—	
Low-Level Input Voltage V_{IL}				2	—	0.5	—	0.5	V
				4.5	—	1.35•	—	1.35•	
				6	—	1.8	—	1.8	
High-Level Output Voltage CMOS Loads V_{OH}	V_{IL} or V_{IH}	I_O = -20 μA		2	1.9	—	1.9	—	V
				4.5	4.4•	—	4.4•	—	
				6	5.9	—	5.9	—	
	V_{IL} or V_{IH}	I_O (mA)	STD. BUS						V
			-4 -6	4.5	3.98•	—	3.7•	—	
TTL Loads			-5.2 -7.8	6	5.48	—	5.2	—	
Low-Level Output Voltage CMOS Loads V_{OL}	V_{IL} or V_{IH}	I_O = 20 μA		2	—	0.1	—	0.1	V
				4.5	—	0.1•	—	0.1•	
				6	—	0.1	—	0.1	
TTL Loads	V_{IL} or V_{IH}	I_O (mA)	STD. BUS						V
			4 6	4.5	—	0.26•	—	0.4•	
			5.2 7.8	6	—	0.26	—	0.4	
Input Leakage Current I_{IN}	V_{CC} or G_{ND}			6	—	±0.1•	—	±1•	μA
*Quiescent Device Current (I_{CC}) SSI	V_{CC}	I_{OUT} = 0		6	—	2•	—	40•	μA
FF	or			6	—	4•	—	80•	
MSI	GND			6	—	8•	—	160•	
*3-State Leakage Current† I_{OZ}	V_{IL} or V_{IH}	V_O = V_{CC} or GND		6	—	±0.5•	—	±10•	μA

*Refer to "Classification of RCA High-Rel QMOS Integrated Circuits According to Circuit Complexity" table.
†For applicable devices only. • Black dot limits are 100% tested.

Ratings and Characteristics

Static Electrical Characteristics for CD54HCT Types

Characteristics	Test Conditions				CD54HC Series				Units
	V_{IN} V			V_{CC} V	+25°C		-55/+125°C		
					Min.	Max.	Min.	Max.	
High-Level Input Voltage V_{IH}				4.5	2•	—	2•	—	V
				5.5	2	—	2	—	
Low-Level Input Voltage V_{IL}				4.5	—	0.8•	—	0.8•	V
				5.5	—	0.8	—	0.8	
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	I_O = -20 μA		4.5	4.4•	—	4.4•	—	V
TTL Loads	V_{IL} or V_{IH}	I_O =	STD. -4mA	BUS -6mA	4.5	3.98•	—	3.7•	—	V
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	I_O = 20 μA			4.5	—	0.1•	—	0.1•	V
TTL Loads	V_{IL} or V_{IH}	I_O =	STD. 4mA	BUS 6mA	4.5	—	0.26•	—	0.4•	V
Input Leakage Current I_{IN}	V_{CC} or GND				6	—	±0.1•	—	±1•	μA
*Quiescent Device Current I_{CC} SSI	V_{CC} or GND	I_{OUT} = 0			6	—	2•	—	40•	μA
MSI					6	—	4•	—	80•	
					6	—	8•	—	160•	
*3-State Leakage Current†	V_{IL} or V_{IH}	V_O = V_{CC} or GND			6	—	±0.5•	—	±10•	μA

*Refer to "Classification of RCA High-Rel QMOS Integrated Circuits According to Circuit Complexity" table.
†For applicable devices only. • Black dot limits are 100% tested.

100% Tested AC Electrical Characteristics at +25°C

Type		Conditions V_{CC} = 4.5V, C_L = 50 pF INPUT T_r = T_f = 6ns	Prop. Delay (Max. Limits) T_{PHL}, T_{PLH}	
HC	HCT		HC	HCT
CD54HC00	CD54HCT00	Input To Output	18ns	20ns
CD54HC02	CD54HCT02	Input To Output	18ns	22ns
CD54HC03	CD54HCT03	Input To Output	18ns	20ns
CD54HC04	CD54HCT04	Input To Output	18ns	20ns
CD54HCU04	—	Input To Output	16ns	—
CD54HC08	CD54HCT08	Input To Output	18ns	27ns
CD54HC10	CD54HCT10	Input To Output	20ns	24ns
CD54HC11	CD54HCT11	Input To Output	22ns	28ns
CD54HC14	CD54HCT14	Input To Output	25ns	38ns
CD54HC20	CD54HCT20	Input To Output	20ns	28ns
CD54HC27	CD54HCT27	Input To Output	20ns	24ns
CD54HC30	CD54HCT30	Input To Output	26ns	30ns
CD54HC32	CD54HCT32	Input To Output	18ns	24ns
CD54HC42	CD54HCT42	Input To $\overline{Y}$	30ns	37ns
CD54HC73	CD54HCT73	$\overline{CP}$ To Q $\overline{R}$ To Q	33ns 28ns	43ns 34ns

Ratings and Characteristics

100% Tested AC Electrical Characteristics at +25° C

Type		Conditions V_{CC} = 4.5V, C_L = 50 pF INPUT $T_r = T_f$ = 6ns	Prop. Delay (Max. Limits) T_{PHL}, T_{PLH}	
HC	HCT		HC	HCT
CD54HC74	CD54HCT74	CP To Q	35ns	35ns
CD54HC75	CD54HCT75	Data to Q $\overline{\text{Enable}}$ To Q	22ns 26ns	30ns 30ns
CD54HC85	CD54HCT85	A_3 To A < B (T_{PHL}) A_1 To A > B (T_{PLH}) A = B To A = B (T_{PLH})	33ns 33ns 24ns	36ns 36ns 31ns
CD54HC86	CD54HCT86	Input To Output	24ns	32ns
CD54HC107	CD54HCT107	CP TO Q R To Q	34ns 31ns	43ns 38ns
CD54HC109	CD54HCT109	CP To Q $\overline{\text{Reset}}$ To $\overline{\text{Q}}$ $\overline{\text{Set}}$ To Q	35ns 37ns 24ns	40ns 37ns 30ns
CD54HC132	CD54HCT132	A, B To Y	25ns	33ns
CD54HC138	CD54HCT138	Address To Output $\overline{\text{Enable}}$ To Output	30ns 35ns	35ns 40ns
CD54HC139	CD54HCT139	Select To Output $\overline{\text{Enable}}$ To Output	32ns 30ns	35ns 35ns
CD54HC147	CD54HCT147	Input To Output	32ns	35ns
CD54HC151	CD54HCT151	Data Input To Y Select To $\overline{\text{Y}}$	34ns 41ns	40ns 46ns
CD54HC153	CD54HCT153	Select To Y Data To Y	32ns 29ns	34ns 24ns
CD54HC154	CD54HCT154	Address To Output $\overline{\text{Enable}}$ To Output	35ns 35ns	35ns 35ns
CD54HC157	CD54HCT157	Select To Output $\overline{\text{Enable}}$ To Output Data To Output	29ns 27ns 25ns	40ns 30ns 30ns
CD54HC158	CD54HCT158	Data To Output $\overline{\text{Enable}}$ To Output Select To Output	28ns 32ns 30ns	32ns 37ns 35ns
CD54HC160	CD54HCT160	CP To Qn TE To TC	41ns 30ns	43ns 35ns
CD54HC161	CD54HCT161	CP To Qn TE To TC	41ns 30ns	43ns 35ns
CD54HC162	CD54HCT162	CP To Qn TE To TC	41ns 30ns	43ns 35ns
CD54HC163	CD54HCT163	CP To Qn TE To TC	41ns 30ns	43ns 35ns
CD54HC164	CD54HCT164	CP To Q	34ns	36ns
CD54HC165	CD54HCT165	CP To Q $\overline{\text{PL}}$ To Q	40ns 35ns	40ns 40ns
CD54HC166	CD54HCT166	CP To Output	35ns	40ns
CD54HC173	CD54HCT173	CP To Output MR To Output $\overline{\text{Output Enable}}$ To Output T_{PHZ}, T_{PLZ} T_{PZL}, T_{PZH}	40ns 40ns 30ns 30ns	43ns 40ns 30ns 35ns
CD54HC174	CD54HCT174	Clock To Q $\overline{\text{MR}}$ To Q	33ns 30ns	40ns 44ns
CD54HC175	CD54HCT175	CP To Q	35ns	35ns
CD54HC181	CD54HCT181	B To $\overline{\text{Cn}}$ + 4 B To G B To A = B	56ns 48ns 56ns	56ns 58ns 56ns

Ratings and Characteristics

100% Tested AC Electrical Characteristics at +25° C

Type		Conditions V_{CC} = 4.5V, C_L = 50 pF INPUT T_r = T_f = 6ns	Prop. Delay (Max. Limits) T_{PHL}, T_{PLH}	
HC	HCT		HC	HCT
CD54HC182	CD54HCT182	$\overline{G_0}$ To Cn + X Cn To Cn + X $\overline{Pn}$ To P	31ns 34ns 26ns	38ns 45ns 31ns
CD54HC190	CD54HCT190	CP To $\overline{RC}$	30ns	35ns
CD54HC194	CD54HCT194	Clock To Output $\overline{MR}$ To Output	35ns 30ns	40ns 40ns
CD54HC195	CD54HCT195	CP To Output $\overline{MR}$ To Output	35ns 30ns	35ns 35ns
CD54HC238	CD54HCT238	Address To Output $\overline{Enable}$ To Output	30ns 35ns	35ns 40ns
CD54HC240	CD54HCT240	Data To Output $\overline{Output\ Enable}$ and $\overline{Disable}$ T_{PZH}, T_{PZL} T_{PHZ}, T_{PLZ}	20ns 30ns	22ns 30ns
CD54HC241	CD54HCT241	Data To Output $\overline{Output\ Enable}$ and $\overline{Disable}$ T_{PZH}, T_{PZL}, T_{PHZ}, T_{PLZ}	22ns 30ns	26ns 30ns
CD54HC242	CD54HCT242	Data To Output $\overline{OEB}$ To B1 T_{PZH}, T_{PZL} $\overline{OEB}$ To B1 T_{PHZ}, T_{PLZ}	25ns 35ns 40ns	30ns 45ns 45ns
CD54HC243	CD54HCT243	Data To Output $\overline{OEB}$ To B1 T_{PZH}, T_{PZL} $\overline{OEB}$ To B1 T_{PHZ}, T_{PLZ}	22ns 35ns 40ns	27ns 45ns 45ns
CD54HC244	CD54HCT244	Data To Output $\overline{Output\ Enable}$ and $\overline{Disable}$ T_{PZH}, T_{PZL}, T_{PHZ}, T_{PLZ}	22ns 30ns	26ns 30ns
CD54HC245	CD54HCT245	Data To Output $\overline{Output\ Disable}$ T_{PLZ}, T_{PHZ} $\overline{Output\ Enable}$ T_{PZL}, T_{PZH}	22ns 30ns 30ns	26ns 30ns 35ns
CD54HC251	CD54HCT251	Select To Output $\overline{OE}$ To Y T_{PZH}, T_{PZL}, T_{PHZ}, T_{PLZ}	40ns 35ns	40ns 35ns
CD54HC253	CD54HCT253	Select To Output $\overline{Output\ Enable}$ and $\overline{Disable}$ T_{PZH}, T_{PZL}, T_{PHZ}, T_{PLZ}	35ns 30ns	40ns 30ns
CD54HC257	CD54HCT257	I_n To Y S To Y $\overline{OE}$ To Y	32ns 35ns 30ns	35ns 40ns 30ns
CD54HC258	CD54HCT258	Select To Output Output Enable and Disable To Output T_{PZH}, T_{PZL}, T_{PHZ}, T_{PLZ}	30ns 30ns	35ns 30ns
CD54HC273	CD54HCT273	CP To Output $\overline{MR}$ To Output	32ns 35ns	37ns 43ns
CD54HC280	CD54HCT280	Input To Odd Input To Even	40ns 40ns	45ns 42ns
CD54HC299	CD54HCT299	Clock To Q $\overline{MR}$ To Output $\overline{OE2}$ To Output T_{PZH}, T_{PHZ}, T_{PLH}, T_{PLZ}	40ns 42ns 37ns	45ns 46ns 40ns
CD54HC354	CD54HCT354	D_n To Y Output Disable To Y T_{PLZ}, T_{PHZ} Output Enable To Y T_{PZL}, T_{PZH}	42ns 33ns 30ns	49ns 33ns 34ns

Ratings and Characteristics

100% Tested AC Electrical Characteristics at +25° C

Type		Conditions V_{CC} = 4.5V, C_L = 50 pF INPUT T_r = T_f = 6ns	Prop. Delay (Max. Limits) T_{PHL}, T_{PLH}	
HC	HCT		HC	HCT
CD54HC356	CD54HCT356	CP To Y, $\overline{Y}$ Output Disable To Y T_{PLZ} T_{PHZ} Output Enable To Y T_{PZL} T_{PZH}	51ns 33ns 35ns 30ns 32ns	51ns 33ns 39ns 34ns 34ns
CD54HC365	CD54HCT365	Data To Output Output Enable and Disable T_{PZH}, T_{PZL}, T_{PHZ}, T_{PLZ}	22ns 30ns	25ns 35ns
CD54HC366	CD54HCT366	Data To Output $\overline{OE}$ To Output T_{PZH}, T_{PZL}, T_{PHZ}, T_{PLZ}	25ns 30ns	30ns 35ns
CD54HC367	CD54HCT367	Data To Output $\overline{OE}$ To Output T_{PZH}, T_{PZL}, T_{PHZ}, T_{PLZ}	22ns 30ns	25ns 35ns
CD54HC368	CD54HCT368	Data To Output $\overline{OE}$ To Output T_{PZH}, T_{PZL}, T_{PHZ}, T_{PLZ}	25ns 30ns	30ns 35ns
CD54HC373	CD54HCT373	Data To Q Output Enable and Disable T_{PZH}, T_{PZL}, T_{PHZ}, T_{PLZ}	35ns 30ns	35ns 35ns
CD54HC374	CD54HCT374	CP To Output Output Disable To Q T_{PLZ}, T_{PHZ} Output Enable To Q T_{PZL}, T_{PZH}	36ns 30ns 35ns	35ns 28ns 33ns
CD54HC377	CD54HCT377	CP To Q	41ns	41ns
CD54HC390	CD54HCT390	Clock To Q_0 Clock To Q_3 MR To Q	29ns 31ns 33ns	34ns 38ns 36ns
CD54HC393	CD54HCT393	CP To Q_O MR To Q	30ns 28ns	32ns 32ns
CD54HC533	CD54HCT533	DATA To Qn $\overline{LE}$ To Qn Output Disable To Q T_{PLZ}, T_{PHZ} Output Enable To Q T_{PZL}, T_{PZH}	33ns 35ns 30ns 35ns	35ns 40ns 30ns 35ns
CD54HC534	CD54HCT534	Clock To Output Output Disable To Q T_{PLZ}, T_{PHZ} Output Enable To Q T_{PZL}, T_{PZH}	33ns 30ns 35ns	35ns 30ns 35ns
CD54HC540	CD54HCT540	Data To Output Output Enable and Disable To Y T_{PHZ}, T_{PLZ}, T_{PZH}, T_{PZL}	23ns 35ns	28ns 35ns
CD54HC541	CD54HCT541	Data To Output Output Enable and Disable To Y T_{PHZ}, T_{PLZ}, T_{PZH}, T_{PZL}	23ns 35ns	28ns 35ns
CD54HC564	CD54HCT564	Clock To Output Output Disable To Q T_{PLZ}, T_{PHZ} Output Enable To Q T_{PZL}, T_{PZH}	33ns 30ns 35ns	35ns 30ns 35ns
CD54HC573	CD54HCT573	Data To Q $\overline{LE}$ To Q Output Enable To Q T_{PZL}, T_{PZH} Output Disable To Q T_{PLZ}, T_{PHZ}	35ns 35ns 30ns 30ns	40ns 35ns 35ns 35ns

Ratings and Characteristics

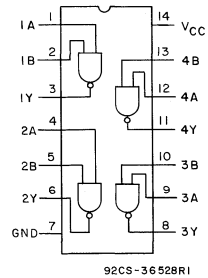
100% Tested AC Electrical Characteristics at +25° C

Type		Conditions V_{CC} = 4.5V, C_L = 50 pF INPUT $T_r = T_f$ = 6ns	Prop. Delay (Max. Limits) T_{PHL}, T_{PLH}	
HC	HCT		HC	HCT
CD54HC574	CD54HCT574	Clock To Output Output Disable To Q Output Enable To Q	36ns 30ns 35ns	35ns 28ns 33ns
CD54HC583	CD54HCT583	B_0 To S_3 B_1 To S_1 Cn To Cn + 4	40ns 40ns 25ns	50ns 50ns 35ns
CD54HC640	CD54HCT640	A To $\overline{B}$ B To $\overline{A}$ Output Enable and Disable To A T_{PZH}, T_{PZL}, T_{PHZ}, T_{PLZ}	20ns 20ns 34ns	22ns 22ns 34ns
CD54HC643	CD54HCT643	B_O To A_O $\overline{OE}$ To A_1 T_{PZH}, T_{PZL} $\overline{OE}$ To A_1 T_{PHZ}, T_{PLZ}	22ns 30ns 34ns	26ns 36ns 36ns
CD54HC688	CD54HCT688	B_N To Output	34ns	34ns
CD54HC4020	CD54HCT4020	$\overline{CP}$ To Q_1	35ns	40ns
CD54HC4024	CD54HCT4024	Clock To Q_1 MR To Q_1	35ns 40ns	40ns 45ns
CD54HC4040	CD54HCT4040	$\overline{CP}$ To Q_1	35ns	40ns
CD54HC4049	—	Input To Output	17ns	—
CD54HC4050	—	Input To Output	17ns	—
CD54HC4510	CD54HCT4510	Clock To Q MR, PE To Q Carry In To Carry Out	40ns 45ns 25ns	40ns 45ns 25ns
CD54HC4518	CD54HCT4518	CP To Q MR To Q	55ns 40ns	60ns 40ns
CD54HC4520	CD54HCT4520	CP To Q MR To Q	55ns 40ns	60ns 40ns
CD54HC4543	CD54HCT4543	A To C Blanking To a $\overline{LD}$ To b	70ns 50ns 70ns	70ns 50ns 70ns
CD54HC7266		Input To Output	24ns	—

NOTES:

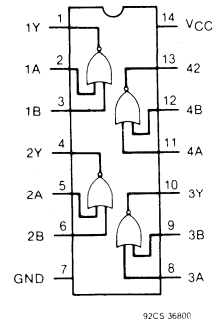
1. This is a table of the parameters which will be 100% tested.
2. AC tests are one input/one output unless otherwise specified.
3. For T_{PHZ} and T_{PZH}, a 1k Ω resistor is connected between the output and V_{SS} terminal. For T_{PZL} and T_{PZL}, a 1k Ω resistor is connected between the output and V_{CC} terminal.

Functional Diagrams



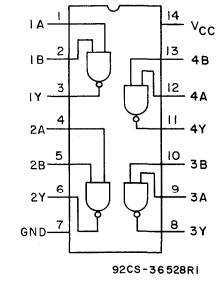
Quad 2-Input NAND Gate

CD54HC00
CD54HCT00 (File No. 1464)



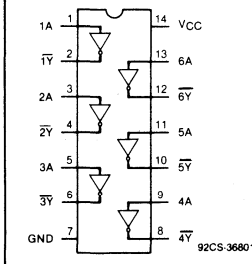
Quad 2-Input NOR Gate

CD54HC02
CD54HCT02 (File No. 1647)



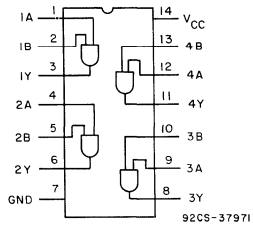
Quad 2-Input NAND Gate

CD54HC03
CD54HCT03



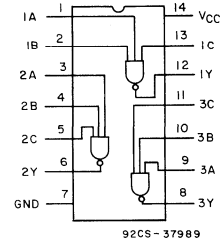
Hex Inverter

CD54HC04
CD54HCT04 (File No. 1471)
CD54HCU04 (File No. 1655)



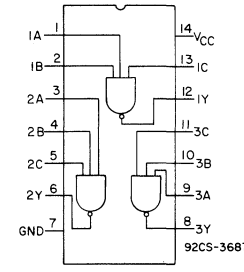
Quad 2-Input AND Gate

CD54HC08
CD54HCT08 (File No. 1549)



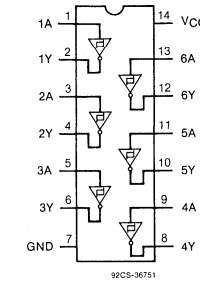
Triple 3-Input NAND Gate

CD54HC10
CD54HCT10 (File No. 1551)



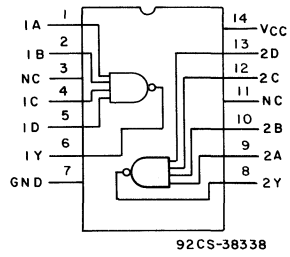
Triple 3-Input AND Gate

CD54HC11
CD54HCT11 (File No. 1475)



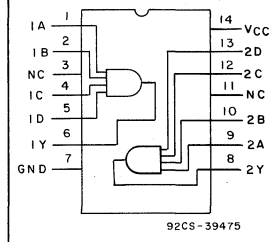
Hex Inverting Schmitt Trigger

CD54HC14
CD54HCT14



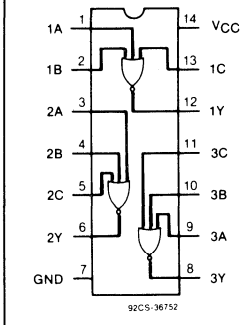
Dual 4-Input NAND Gate

CD54HC20
CD54HCT20 (File No. 1601)



Dual 4-Input AND Gate

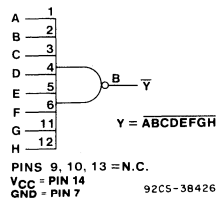
CD54HC21
CD54HCT21



Triple 3-Input NOR Gate

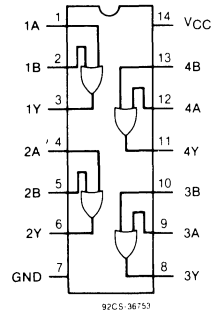
CD54HC27
CD54HCT27 (File No. 1648)

Functional Diagrams



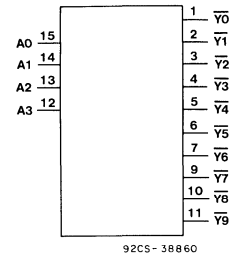
8-Input NAND Gate

CD54HC30
CD54HCT30 (File No. 1652)



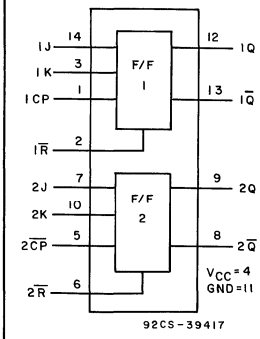
Quad 2-Input OR Gate

CD54HC32
CD54HCT32 (File No. 1643)



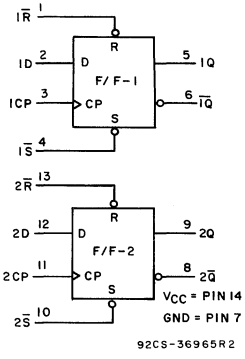
BCD-to-Decimal Decoder (1-to-10)

CD54HC42
CD54HCT42 (File No. 1689)



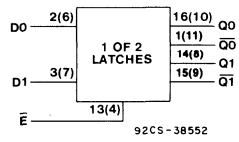
Dual J-K Flip-Flop w/RESET

CD54HC73
CD54HCT73 (File No. 1721)



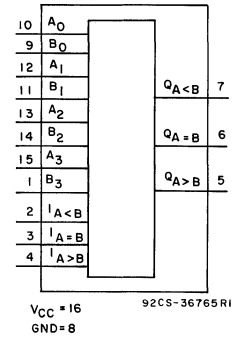
Dual D Flip-Flop w/SET and RESET

CD54HC74
CD54HCT74 (File No. 1476)



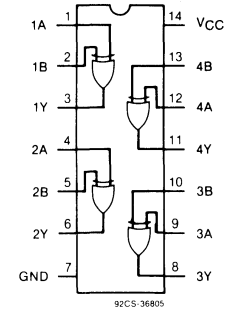
Quad Bistable Transparent Latch

CD54HC75
CD54HCT75 (File No. 1666)



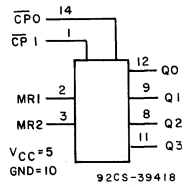
4-Bit Magnitude Comparator

CD54HC85
CD54HCT85



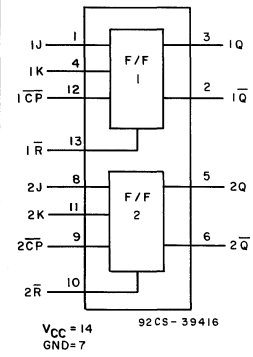
Quad 2-Input EXCLUSIVE-OR Gate

CD54HC86
CD54HCT86 (File No. 1644)



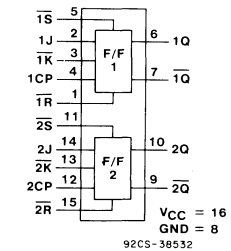
4-Bit Binary Ripple Counter

CD54HC93
CD54HCT93



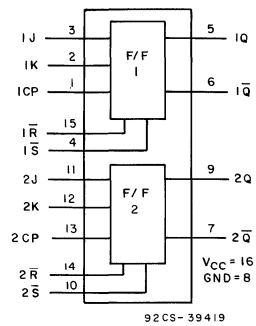
Dual J-K Flip-Flop w/RESET

CD54HC107
CD54HCT107 (File No. 1722)



Dual J-K Flip-Flop w/SET and RESET

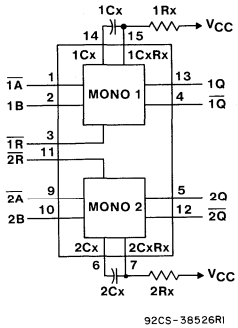
CD54HC109
CD54HCT109 (File No. 1667)



Dual J-K Flip-Flop w/SET and RESET

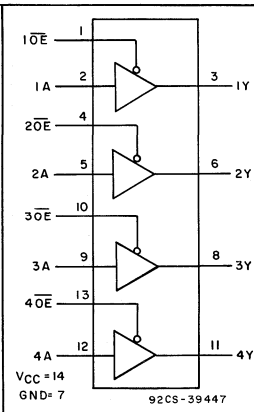
CD54HC112
CD54HCT112

Functional Diagrams



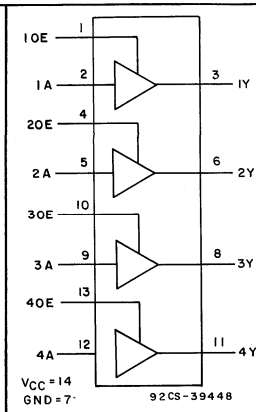
Dual Retriggerable Monostable Multivibrator w/RESET

CD54HC123
CD54HCT123 (File No. 1708)



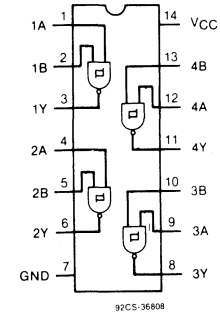
Quad 3-State Buffer

CD54HC125
CD54HCT125



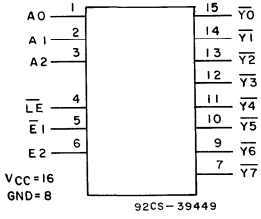
Quad 3-State Buffer

CD54HC126
CD54HCT126



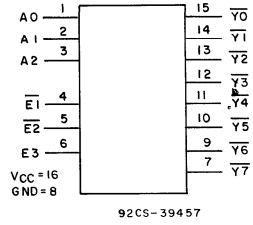
Quad 2-Input NAND Schmitt Trigger

CD54HC132
CD54HCT132 (File No. 1649)



3-to-8-Line Decoder with Latch, Inverting

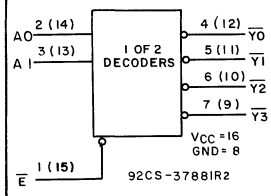
CD54HC137
CD54HCT137



3-to-8-Line Decoder/ Demultiplexer

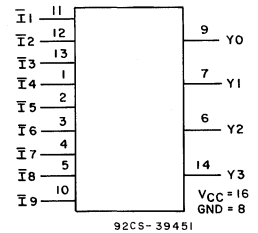
CD54HC138
CD54HCT138
Inverting

(File No. 1477)



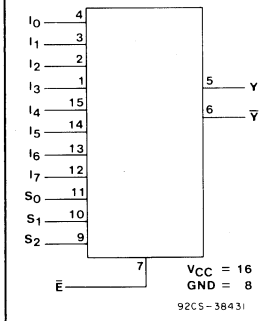
Dual 2-of-4-Line Decoder/ Demultiplexer

CD54HC139
CD54HCT139 (File No. 1545)



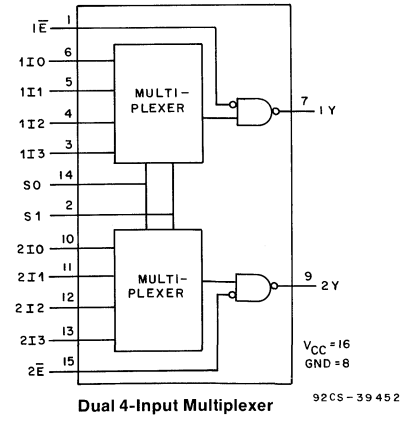
10-to-4-Line Priority Encoder

CD54HC147
CD54HCT147



8-Input Multiplexer

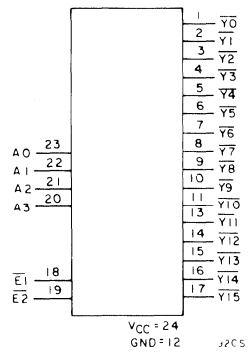
CD54HC151
CD54HCT151 (File No. 1645)



Dual 4-Input Multiplexer

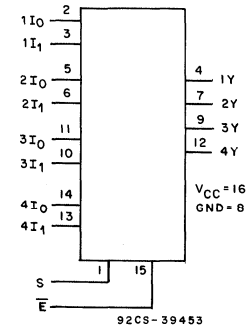
CD54HC153
CD54HCT153

Functional Diagrams



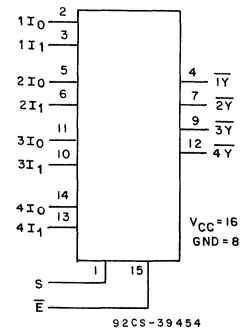
4-to-16-Line Decoder/ Demultiplexer

CD54HC154
CD54HCT154 (File No. 1657)



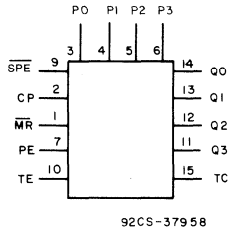
Quad 2-Input Multiplexer

CD54HC157
CD54HCT157 (File No. 1642)



Quad 2-Input Multiplexer

CD54HC158
CD54HCT158 (File No. 1642)
Inverting



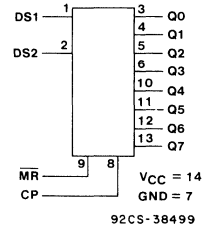
Synchronous Presettable Counters

CD54HC160
CD54HCT160 (File No. 1550)
BCD Decade, Asynchronous Reset

CD54HC162
CD54HCT162 (File No. 1550)
BCD Decade, Synchronous Reset

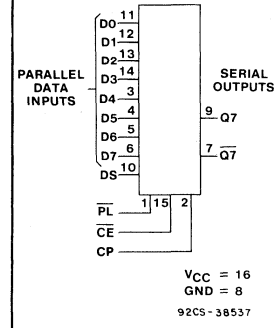
CD54HC161
CD54HCT161 (File No. 1550)
4-Bit Binary Asynchronous Reset

CD54HC163
CD54HCT163 (File No. 1550)
4-Bit Binary, Synchronous Reset



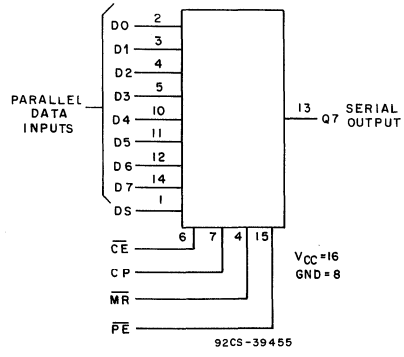
8-Bit Serial-In Parallel-Out Shift Register

CD54HC164
CD54HCT164 (File No. 1658)



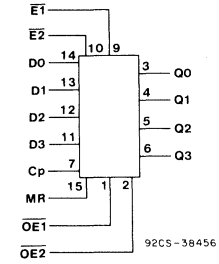
8-Bit Parallel-In Serial-Out Shift Register

CD54HC165
CD54HCT165 (File No. 1672)



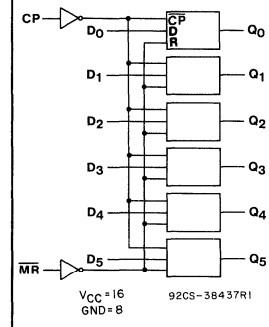
8-Bit Parallel-In Serial-Out Shift Register

CD54HC166
CD54HCT166 (File No. 1501)



Quad D-Type Flip-Flop, 3-State

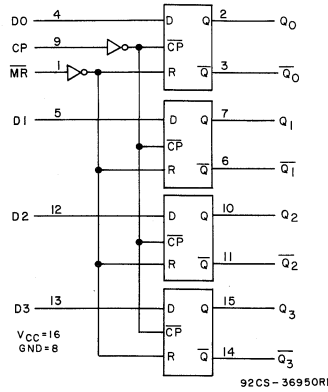
CD54HC173
CD54HCT173 (File No. 1641)



Hex D-Type Flip-Flop w/RESET

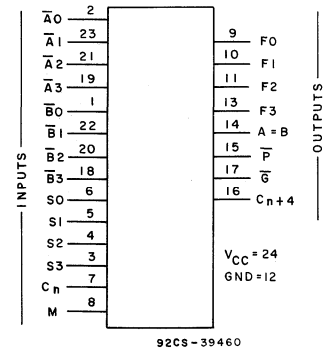
CD54HC174
CD54HCT174 (File No. 1608)

Functional Diagrams



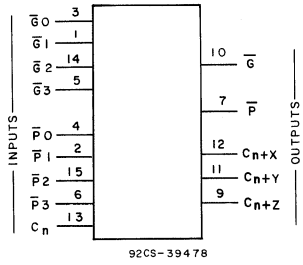
Quad D-Type Flip-Flop w/RESET

CD54HC175
CD54HCT175 (File No. 1474)



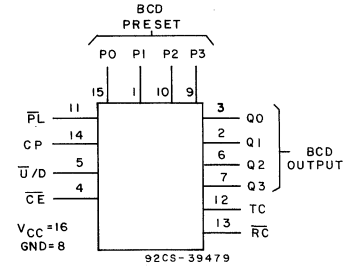
4-Bit Arithmetic Logic Unit (ALU)

CD54HC181
CD54HCT181



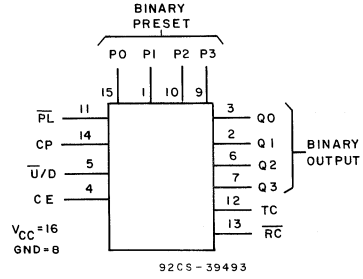
Carry Generator

CD54HC182
CD54HCT182



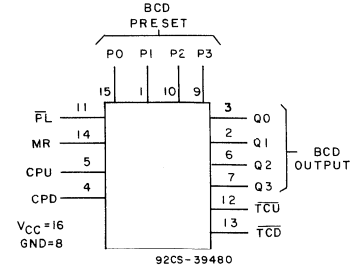
Presettable Synchronous Up/Down Counters

CD54HC190
CD54HCT190 (File No. 1662)
BCD Decade



Presettable Synchronous Up/Down Counters

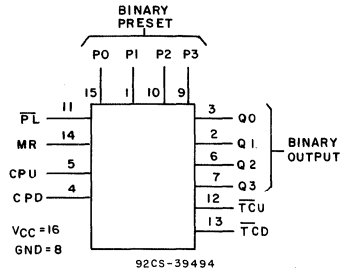
CD54HC191
CD54HCT191 (File No. 1662)
4-Bit Binary



Presettable Synchronous Up/Down Counters

CD54HC192
CD54HCT192 (File No. 1674)
BCD Decade

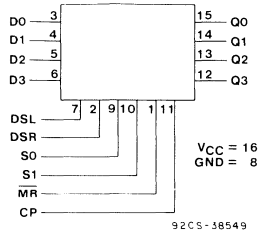
Functional Diagrams



Presettable Synchronous Up/Down Counters

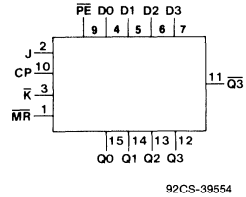
CD54HC193
CD54HCT193
4-Bit Binary

(File No. 1674)



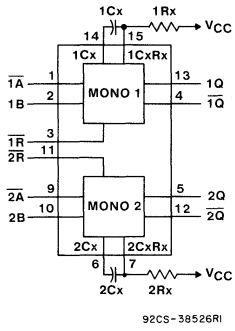
4-Bit Bidirectional Universal Shift Register

CD54HC194
CD54HCT194 (File No. 1668)



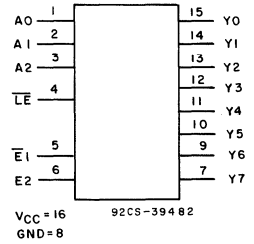
4-Bit Parallel Access Shift Register

CD54HC195
CD54HCT195 (File No. 1482)



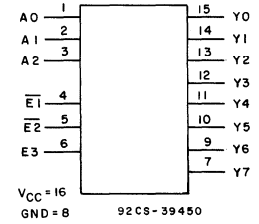
Dual Monostable Multivibrator w/RESET

CD54HC221
CD54HCT221 (File No. 1670)



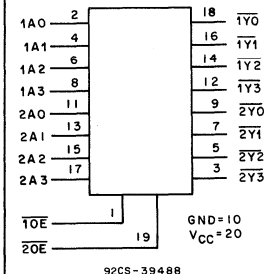
3-to-8-Line Decoder/Demultiplexer

CD54HC237
CD54HCT237



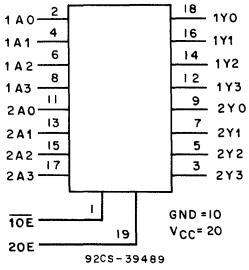
3-to-8-Line Decoder/Demultiplexer

CD54HC238
CD54HCT238 (File No. 1477)



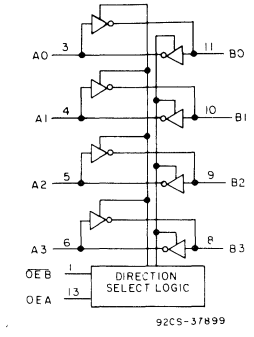
Octal Buffer/Line Driver, 3-State, Inverting

CD54HC240
CD54HCT240 (File No. 1656)



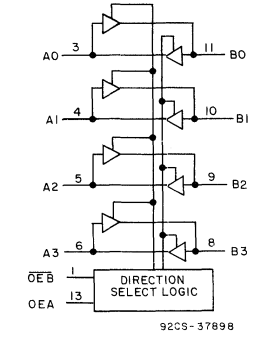
Octal Buffer/Line Driver, 3-State

CD54HC241
CD54HCT241 (File No. 1656)



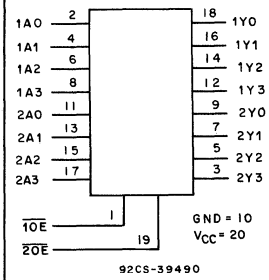
Quad Bus Transceiver, 3-State, Inverting

CD54HC242
CD54HCT242 (File No. 1488)



Quad Bus Transceiver, 3-State

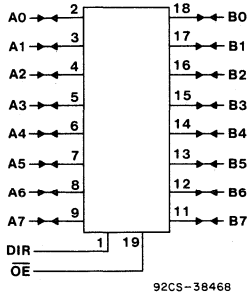
CD54HC243
CD54HCT243 (File No. 1488)



Octal Buffer/Line Driver, 3-State

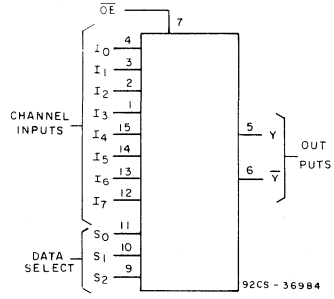
CD54HC244
CD54HCT244 (File No. 1656)

Functional Diagrams



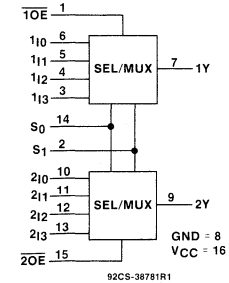
Octal Bus Transceiver, 3-State

CD54HC245
CD54HCT245 (File No. 1651)



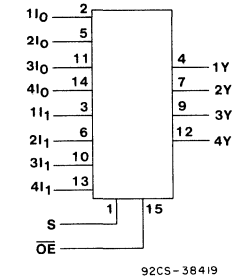
8-Input Multiplexer, 3-State

CD54HC251
CD54HCT251 (File No. 1489)



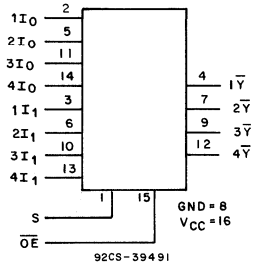
Dual 4-Input Multiplexer, 3-State

CD54HC253
CD54HCT253 (File No. 1673)



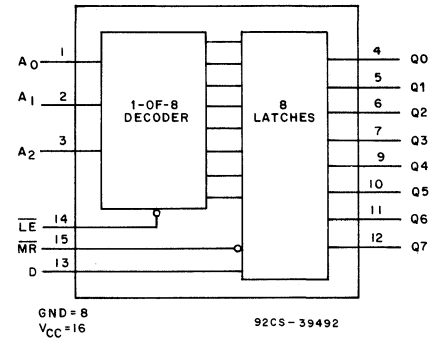
Quad 2-Input Multiplexer, 3-State

CD54HC257
CD54HCT257 (File No. 1650)



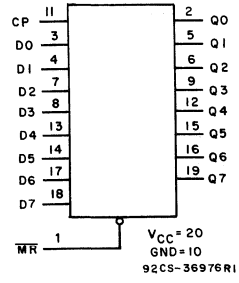
Quad 2-Line-to-4-Line Data Selector

CD54HC258
CD54HCT258



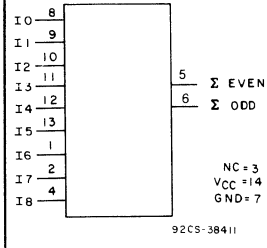
8-Bit Addressable Latch

CD54HC259
CD54HCT259 (File No. 1727)



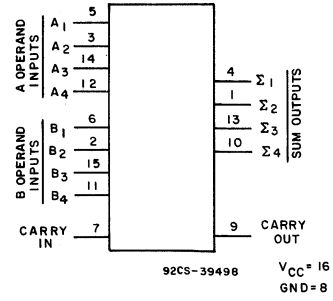
Octal D-Type Flip-Flop w/RESET

CD54HC273
CD54HCT273 (File No. 1479)



9-Bit Odd/Even Parity Generator/Checker

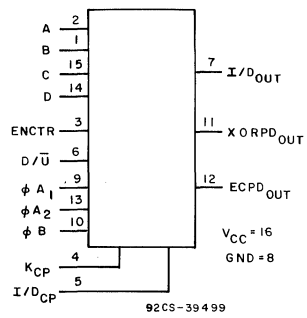
CD54HC280
CD54HCT280 (File No. 1669)



4-Bit Full Adder w/Fast Carry

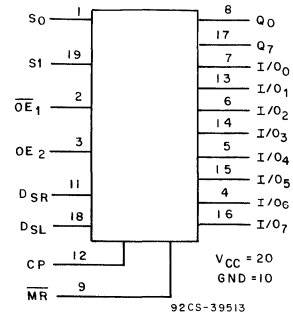
CD54HC283
CD54HCT283

Functional Diagrams



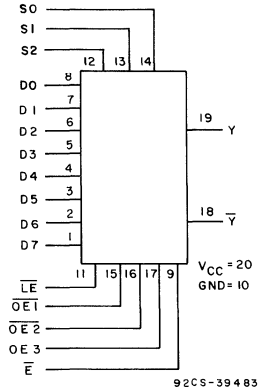
Digital Phase-Locked-Loop Filter

CD54HC297
CD54HCT297



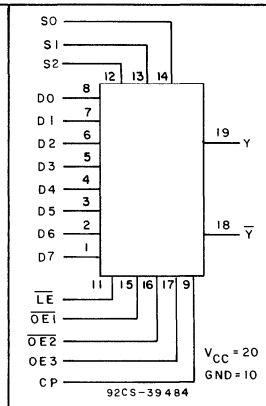
8-Bit Universal Shift Register, 3-State

CD54HC299
CD54HCT299 (File No. 1485)



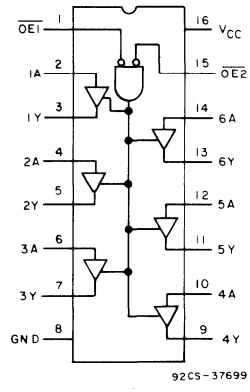
8-Input Multiplexer/Register, 3-State

CD54HC354
CD54HCT354 (File No. 1690)



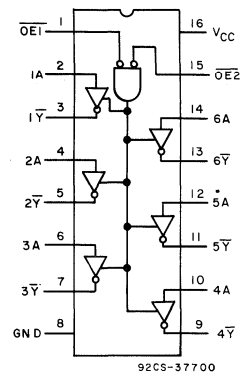
8-Input Multiplexer/Register, 3-State

CD54HC356
CD54HCT356 (File No. 1690)



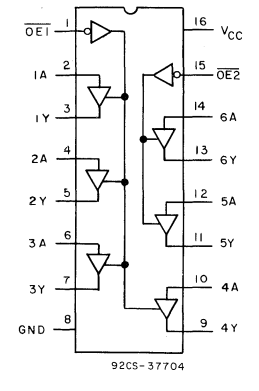
Hex Buffer/Line Driver, 3-State

CD54HC365
CD54HCT365 (File No. 1539)



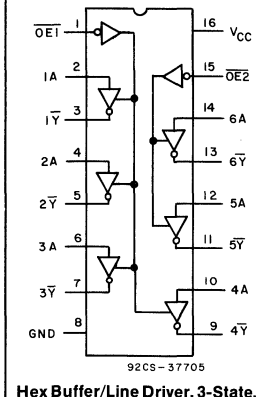
Hex Buffer/Line Driver, 3-State, Inverting

CD54HC366
CD54HCT366 (File No. 1539)



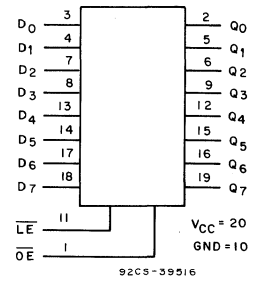
Hex Buffer/Line Driver, 3-State

CD54HC367
CD54HCT367 (File No. 1538)



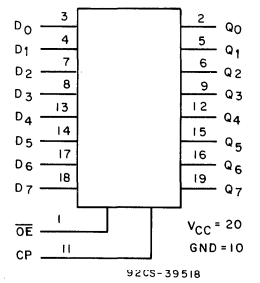
Hex Buffer/Line Driver, 3-State, Inverting

CD54HC368
CD54HCT368 (File No. 1538)



Octal Transparent Latch, 3-State

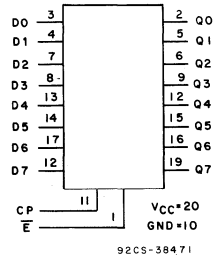
CD54HC373
CD54HCT373 (File No. 1679)



Octal D-Type Flip-Flop, 3-State

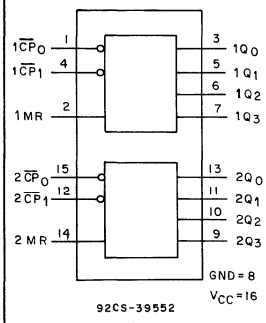
CD54HC374
CD54HCT374 (File No. 1663)

Functional Diagrams



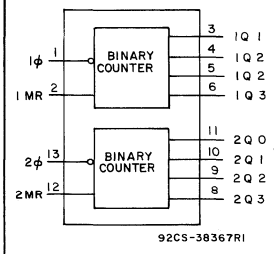
Octal D-Type Flip-Flop with Data Enable

CD54HC377
CD54HCT377 (File No. 1675)



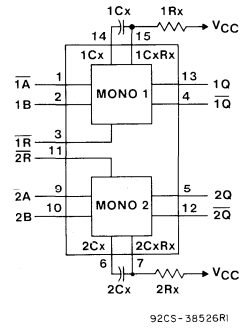
Dual Decade Ripple Counter

CD54HC390
CD54HCT390



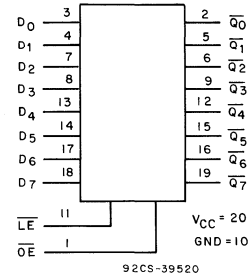
Dual 4-Bit Binary Ripple Counter

CD54HC393
CD54HCT393 (File No. 1653)



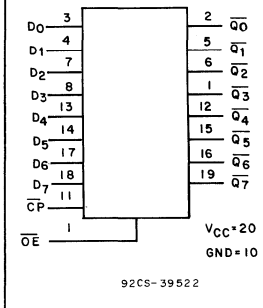
Dual Retriggerable Monostable Multivibrator w/RESET

CD54HC423
CD54HCT423



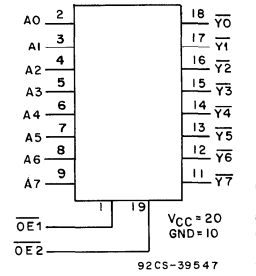
Octal Transparent Latch, 3-State, Inverting

CD54HC533
CD54HCT533 (File No. 1599)



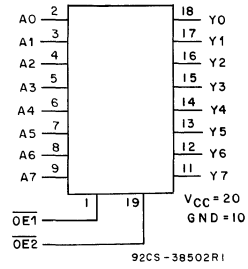
Octal D-Type Flip-Flop, 3-State, Inverting

CD54HC534
CD54HCT534 (File No. 1640)



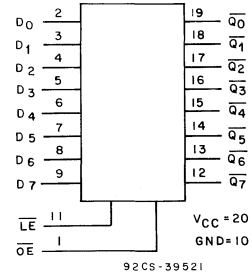
Octal Buffer/Line Driver, 3-State, Inverting

CD54HC540
CD54HCT540 (File No. 1659)



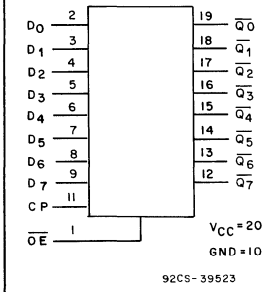
Octal Buffer/Line Driver, 3-State

CD54HC541
CD54HCT541 (File No. 1659)



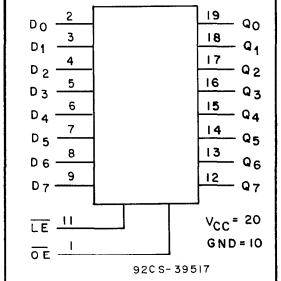
Octal Transparent Latch, 3-State, Inverting

CD54HC563
CD54HCT563 (File No. 1599)



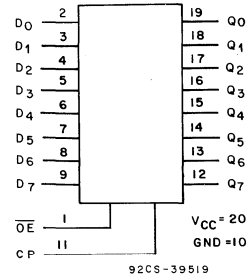
Octal D-Type Flip-Flop, 3-State, Inverting

CD54HC564
CD54HCT564 (File No. 1640)



Octal Transparent Latch, 3-State

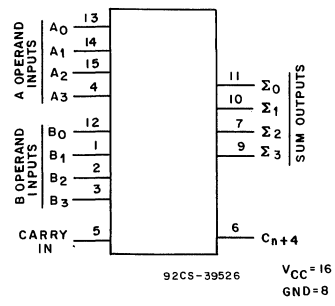
CD54HC573
CD54HCT573 (File No. 1679)



Octal D-Type Flip-Flop, 3-State

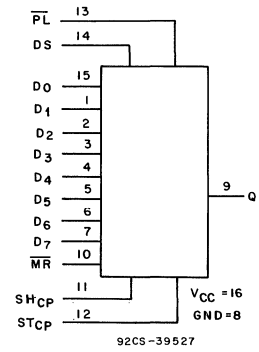
CD54HC574
CD54HCT574 (File No. 1663)

Functional Diagrams



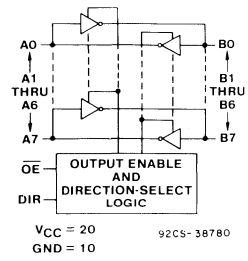
4-Bit Full Adder w/Fast Carry

CD54HC583
CD54HCT583



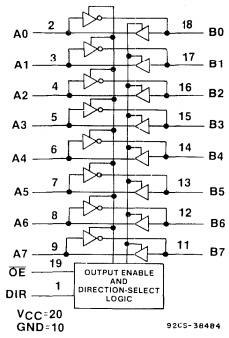
8-Bit Shift Register with I/P Latch

CD54HC597
CD54HCT597



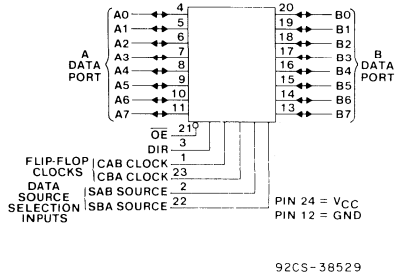
Octal Bus Transceiver, 3-State, Inverting

CD54HC640
CD54HCT640 (File No. 1677)



Octal Bus Transceiver, 3-State, True/Inverting

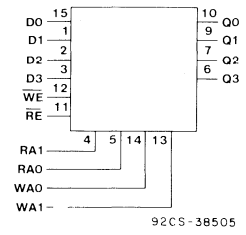
CD54HC643
CD54HCT643 (File No. 1677)



Octal Bus Transceiver/Register, 3-State, Non-Inverting

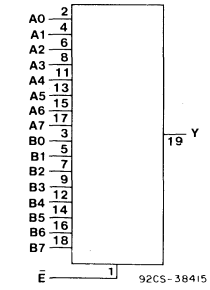
CD54HC646
CD54HCT646 (File No. 1664)

CD54HC648
CD54HCT648 (File No. 1664)



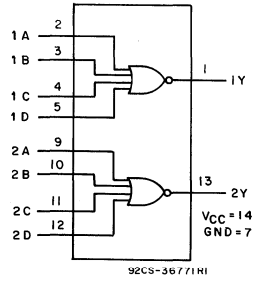
4 x 4 Register File, 3-State

CD54HC670
CD54HCT670 (File No. 1660)



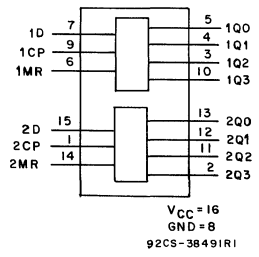
8-Bit Magnitude Comparator

CD54HC688
CD54HCT688 (File No. 1646)



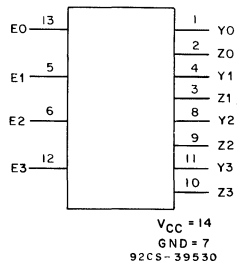
Dual 4-Input NOR Gate

CD54HC4002
CD54HCT4002



Dual 4-Bit Serial-In/Parallel Out Shift Register

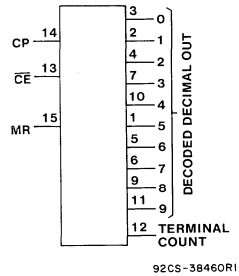
CD54HC4015
CD54HCT4015 (File No. 1678)



Quad Bilateral Switch

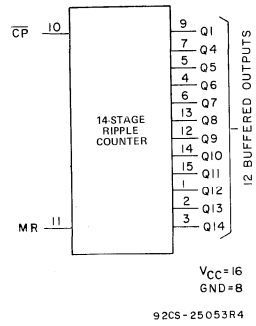
CD54HC4016
CD54HCT4016

Functional Diagrams



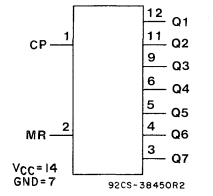
Johnson Decade Counter w/10 Decoded Outputs

CD54HC4017
CD54HCT4017 (File No. 1639)



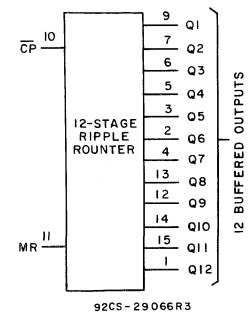
14-Stage Binary Ripple Counter

CD54HC4020
CD54HCT4020 (File No. 1484)



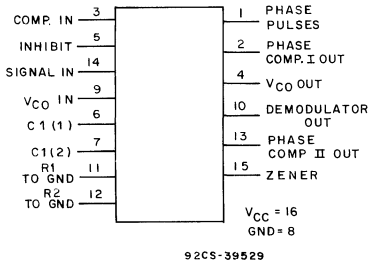
7-Stage Binary Ripple Counter

CD54HC4024
CD54HCT4024 (File No. 1638)



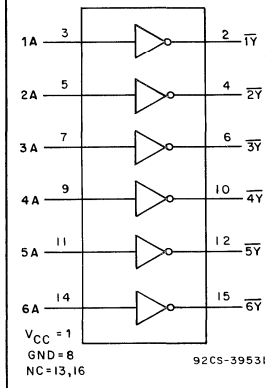
12-Bit Binary Ripple Counter

CD54HC4040
CD54HCT4040 (File No. 1483)



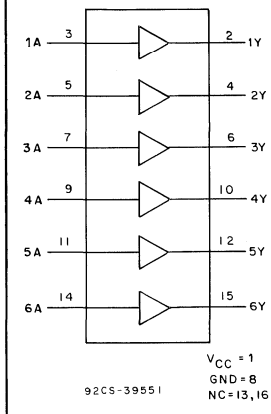
Phase-Locked Loop with VCO

CD54HC4046
CD54HCT4046



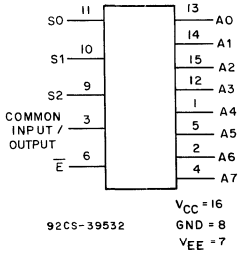
Hex Inverting HIGH-to-LOW Level Shifter

CD54HC4049 (File No. 1543)



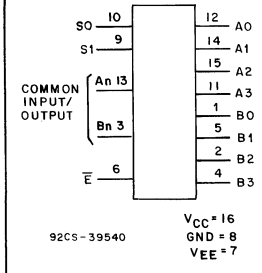
Hex HIGH-to-LOW Level Shifter

CD54HC4050 (File No. 1543)



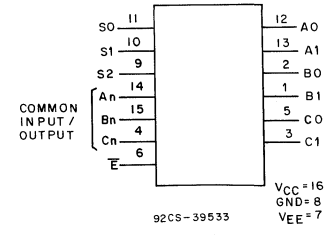
8-Channel Analog Multiplexer/ Demultiplexer

CD54HC4051
CD54HCT4051 (File No. 1676)



Dual 4-Channel Analog Multiplexer/Demultiplexer

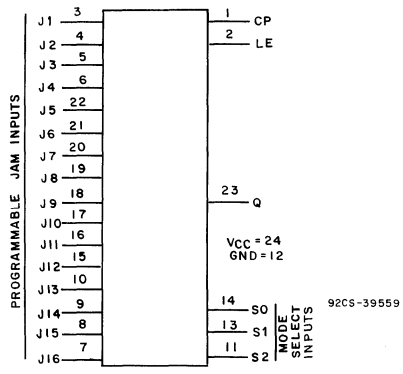
CD54HC4052
CD54HCT4052 (File No. 1676)



Triple 2-Channel Analog Multiplexer/Demultiplexer

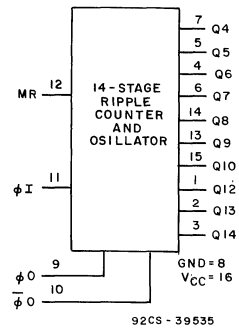
CD54HC4053
CD54HCT4053 (File No. 1676)

Functional Diagrams



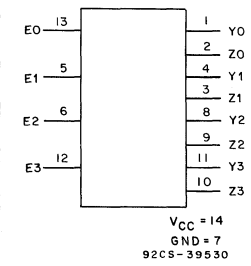
Programmable Divided-by-"N" Counter

CD54HC4059
CD54HCT4059



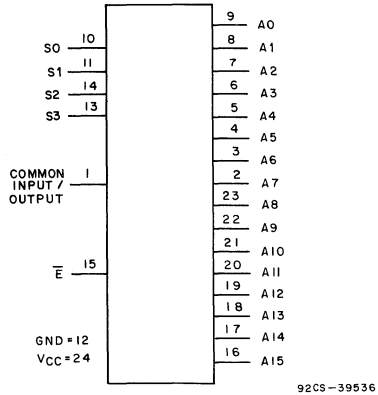
14-Stage Binary Ripple Counter w/Oscillator

CD54HC4060
CD54HCT4060



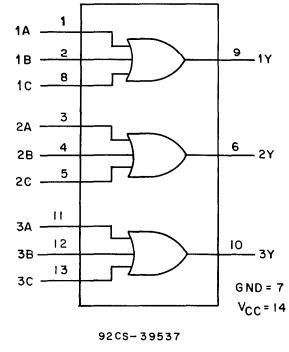
Quad Bilateral Switch

CD54HC4066
CD54HCT4066



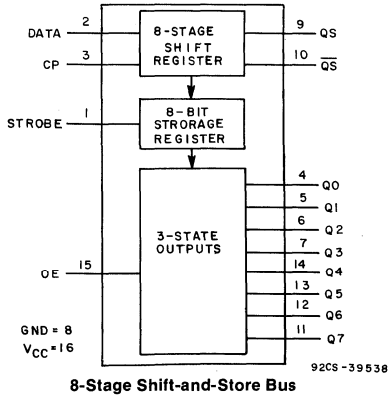
16-Channel Analog Multiplexer/ Demultiplexer

CD54HC4067
CD54HCT4067



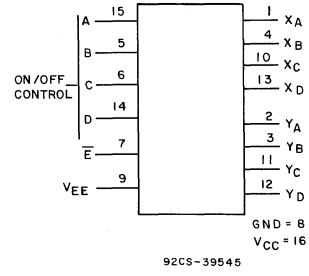
Triple 3-Input OR Gate

CD54HC4075
CD54HCT4075



8-Stage Shift-and-Store Bus Register

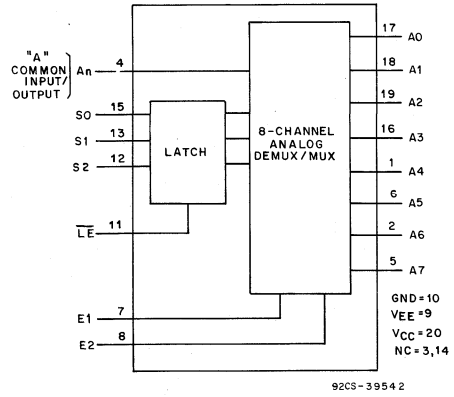
CD54HC4094
CD54HCT4094



Quad Analog Switch

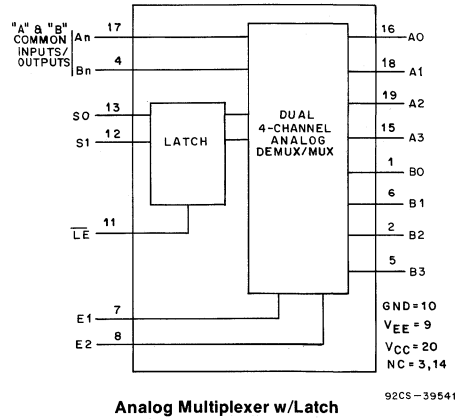
CD54HC4316
CD54HCT4316

Functional Diagrams



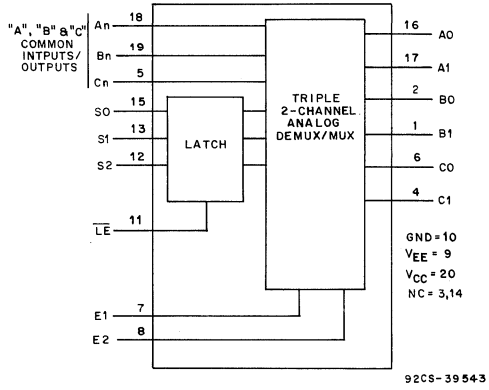
Analog Multiplexer w/Latch

CD54HC4351
CD54HCT4351



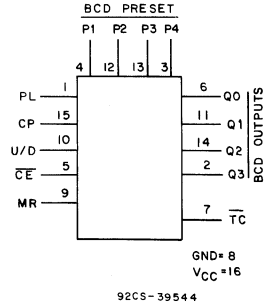
Analog Multiplexer w/Latch

CD54HC4352
CD54HCT4352



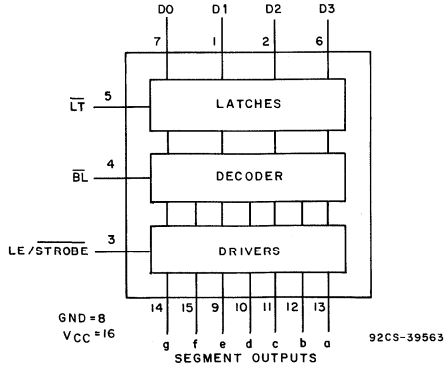
Analog Multiplexer w/Latch

CD54HC4353
CD54HCT4353



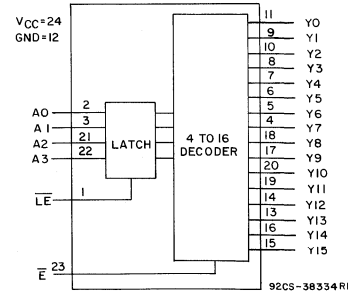
Up/Down Counter, BCD

CD54HC4510
CD54HCT4510



BCD-to-7-Segment Latch/ Decoder/Driver

CD54HC4511
CD54HCT4511

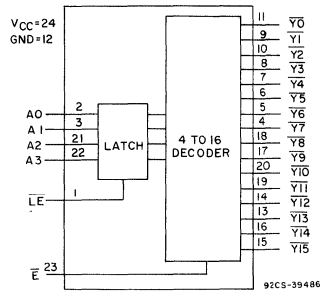


4-to-16-Line Decoder/Demultiplexer w/Input Latches

CD54HC4514
CD54HCT4514

(File No. 1597)

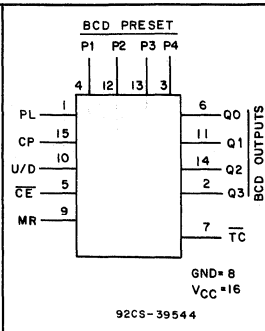
Functional Diagrams



4-to-16-Line Decoder with Input Latches

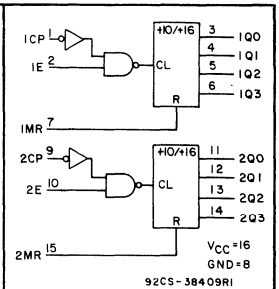
CD54HC4515
CD54HCT4515

(File No. 1597)



Up/Down Counter, Binary

CD54HC4516
CD54HCT4516

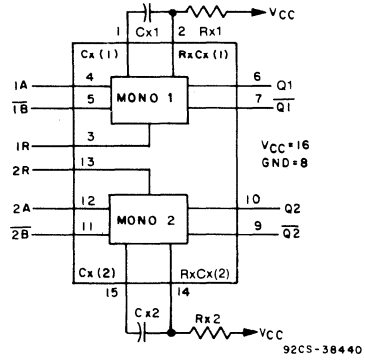


Dual Synchronous BCD Counter

CD54HC4518
CD54HCT4518

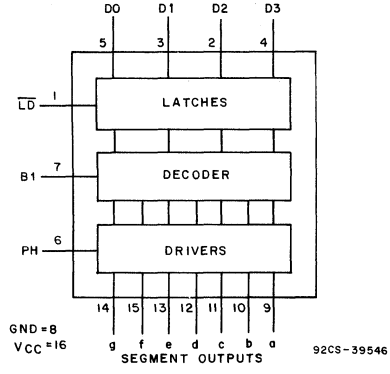
Dual 4-Bit Synchronous Binary Counter

CD54HC4520
CD54HCT4520



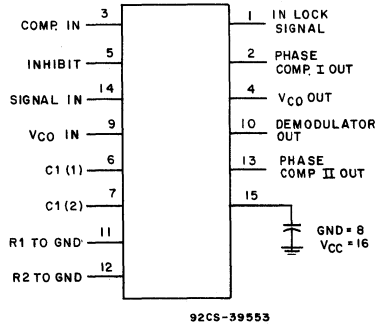
Dual Precision Monostable Multivibrator

CD54HC4538
CD54HCT4538



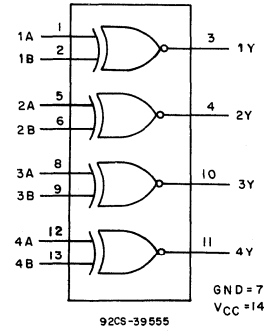
BCD-to-7-Segment Latch/Decoder/Driver for LCDs

CD54HC4543
CD54HCT4543



Phase-Locked Loop with In-Lock Detection

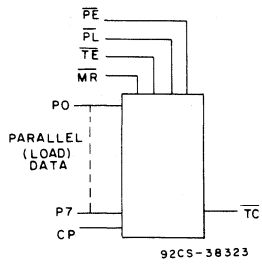
CD54HC7046
CD54HCT7046



Quad Exclusive NOR

CD54HC7266

Functional Diagrams

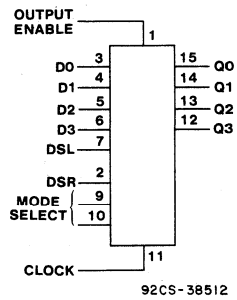


8-Bit Synchronous BCD Down Counter

CD54HC40102
CD54HCT40102

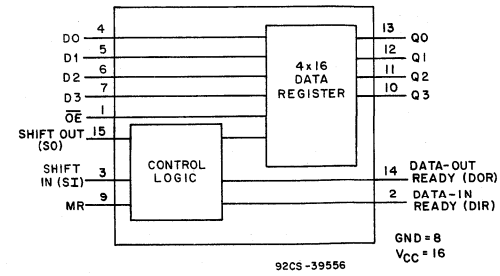
8-Bit Binary Down Counter

CD54HC40103
CD54HCT40103



4-Bit Bidirectional Universal Shift Register, 3-State

CD54HC40104
CD54HCT40104



4 Bits x 16 Words FIFO Register

CD54HC40105
CD54HCT40105

Static Burn-In Test-Circuit Connections

NOTE: Each pin except V_{CC} and V_{SS} will have a resistor of 2k-47k ohms. In most cases, V_{SS} is at pin 7 (of 14-pin IC), pin 8 (of 16-pin IC), pin 9 (of 18-pin IC), pin 10 (of 20-pin IC), or pin 12 (of 24-pin IC), while V_{CC} is at the highest numbered pin. Exceptions are noted by an asterisk (*).

	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT00	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
CD54HC/HCT02	1,4,10,13	2,3,5-9,11,12	14	1,4,10,13	7	2,3,5,6,8,9,11,12,14
CD54HC/HCT03	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
CD54HC/HCT04	2,4,6,8,10,12	1,3,5,7,9,11,13	14	2,4,6,8,10,12	7	1,3,5,9,11,13,14
CD54 HCU04	2,4,6,8,10,12	1,3,5,7,9,11,13	14	2,4,6,8,10,12	7	1,3,5,9,11,13,14
CD54HC/HCT08	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
CD54HC/HCT10	6,8,12	1-5,7,9-11,13	14	6,8,12	7	1-5,9-11,13,14
CD54HC/HCT11	6,8,12	1-5,7,9-11,13	14	6,8,12	7	1-5,9-11,13,14
CD54HC/HCT14	2,4,6,8,10,12	1,3,5,7,9,11,13	14	2,4,6,8,10,12	7	1,3,5,9,11,13,14
CD54HC/HCT20	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
CD54HC/HCT21	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
CD54HC/HCT27	6,8,12	1-5,7,9-11,13	14	6,8,12	7	1-5,9-11,13,14
CD54HC/HCT30	8-10,13	1-7,11,12	14	8-10,13	7	1-6,11,12,14
CD54HC/HCT32	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
CD54HC/HCT42	1-7,9-11	8,12-15	16	1-7,9-11	8	12-16
CD54HC/HCT73*	8,9,12,13	1-3,5-7,10,11•,14	4•	8,9,12,13	11•	1-3,4•,5-7,10,14
CD54HC/HCT74	5,6,8,9	1-4,7,10-13	14	5,6,8,9	7	1-4,10-14
CD54HC/HCT75*	1,8-11,14-16	2-4,6,7,12•,13	5•	1,8-11,14-16	12•	2-4,5•,6,7,13
CD54HC/HCT85	5-7	1-4,8-15	16	5-7	8	1-4,9-16
CD54HC/HCT86	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
CD54HC/HCT*93	4,6,7,8,9, 11-13	1-3,10•,14	5•	4,6,7,8,9, 11-13	10	1-3,5,14
CD54HC/HCT107	2,3,5,6	1,4,7-13	14	2,3,5,6	7	1,4,8-14
CD54HC/HCT109	6,7,9,10	1-5,8,11-15	16	6,7,9,10	8	1-5,11-16
CD54HC/HCT112	5-7,9	1-4,8,10-15	16	5-7,9	8	1-4,10-16
CD54HC/HCT123	4-7,12-15	1-3,8-11	16	4-7,12-15	8	1-3,9-11,16
CD54HC/HCT125	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
CD54HC/HCT126	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
CD54HC/HCT132	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
CD54HC/HCT137	7,9-15	1-6,8	16	7,9-15	8	1-6,16
CD54HC/HCT138	7,9-15	1-6,8	16	7,9-15	8	1-6,16
CD54HC/HCT139	4,7,9,12	1-3,8,13-15	16	4-7,9-12	8	1-3,13-16
CD54HC/HCT147	6,7,9,14,15	1-5,8,10-13	16	6,7,9,14,15	8	1-5,10-13,16
CD54HC/HCT151	5,6	1-4,7-15	16	5,6	8	1-4,7,9-16
CD54HC/HCT153	7,9	1-6,8,10-15	16	7,9	8	1-6,10-16
CD54HC/HCT154	1-11,13-17	12,18-23	24	1-11,13-17	12	18-24
CD54HC/HCT157	4,7,9,12	1-3,5,6,8,10,11,13-15	16	4,7,9,12	8	1-3,5,6,10,11,13-16
CD54HC/HCT158	4,7,9,12	1-3,5,6,8,10,11,13-15	16	4,7,9,12	8	1-3,5,6,10,11,13-16
CD54HC/HCT160	11-15	1-10	16	11-15	8	1-7,9,10,16
CD54HC/HCT161	11-15	1-10	16	11-15	8	1-7,9,10,16
CD54HC/HCT162	11-15	1-10	16	11-15	8	1-7,9,10,16
CD54HC/HCT163	11-15	1-10	16	11-15	8	1-7,9,10,16
CD54HC/HCT164	3-6,10-13	1,2,7-9	14	3-6,10-13	7	1,2,8,9,14
CD54HC/HCT165	7,9	1-6,8,10-15	16	7,9	8	1-6,10-16
CD54HC/HCT166	13	1-12,14,15	16	13	8	1-7,9-12,14-16
CD54HC/HCT173	3-6	1,2,7-15	16	3-6	8	1,2,7,9-16
CD54HC/HCT174	2,5,7,10, 12,15	1,3,4,6,8,9,11,13,14	16	2,5,7,10, 12,15	8	1,3,4,6,9,11,13, 14,16
CD54HC/HCT175	2,3,6,7,10, 11,14,15	1,4,5,8,9,12,13	16	2,3,6,7,10, 11,14,15	8	1,4,5,9,12,13,16

*Non-standard pin arrangement; connect pins marked (•) without using a resistor.

Static Burn-In Test-Circuit Connections

TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT181	9-11,13-17	1-8,12,18-23	24	9-11,13-17	12	1-8,18-24
CD54HC/HCT182	7,9-12	1-6,8,13-15	16	7,9-12	8	1-6,13-16
CD54HC/HCT190	2,3,6,7,12,13	1,4,5,8-11,14,15	16	2,3,6,7,12,13	8	1,4,5,9-11,14-16
CD54HC/HCT191	2,3,6,7,12,13	1,4,5,8-11,14,15	16	2,3,6,7,12,13	8	1,4,5,9-11,14-16
CD54HC/HCT192	2,3,6,7,12,13	1,4,5,8-11,14,15	16	2,3,6,7,12,13	8	1,4,5,9-11,14-16
CD54HC/HCT193	2,3,6,7,12,13	1,4,5,8-11,14,15	16	2,3,6,7,12,13	8	1,4,5,9-11,14-16
CD54HC/HCT194	12-15	1-11	16	12-15	8	1-7,9-11,16
CD54HC/HCT195	11-15	1-10	16	11-15	8	1-7,9,10,16
CD54HC/HCT221	4-7,12-15	1-3,8-11	16	4-7,12-15	8	1-3,9-11,16
CD54HC/HCT237	7,9-15	1-6,8	16	7,9-15	8	1-6,16
CD54HC/HCT238	7,9-15	1-6,8	16	7,9-15	8	1-6,16
CD54HC/HCT240	3,5,7,9,12, 14,16,18	1,2,4,6,8,10,11,13, 15,17,19	20	3,5,7,9,12, 14,16,18	10	1,2,4,6,8,11,13,15, 17,19,20
CD54HC/HCT241	3,5,7,9,12, 14,16,18	1,2,4,6,8,10,11,13, 15,17,19	20	3,5,7,9,12 14,16,18	10	1,2,4,6,8,11,13,15, 17,19.20
CD54HC/HCT242	2,8-12	1,3-7,13	14	2-6,12	7	1,8-11,13,14
CD54HC/HCT243	2,8-12	1,3-7,13	14	2-6,12	7	1,8-11,13,14
CD54HC/HCT244	3,5,7,9,12 14,16,18	1,2,4,6,8,10,11,13, 15,17,19	20	3,5,7,9,12, 14,16,18	10	1,2,4,6,8,11,13,15, 17,19,20
CD54HC/HCT245	2-9	1,10-19	20	—	10	1-9,11-18, 19,20
CD54HC/HCT251	5,6	1-4,7-15	16	5,6	8	1-4,7,9-16
CD54HC/HCT253	7,9	1-6,8,10-15	16	7,9	8	1-6,10-16
CD54HC/HCT257	4,7,9,12	1-3,5,6,8,10,11, 13-15	16	4,7,9,12	8	1-3,5,6,10,11,13-16
CD54HC/HCT258	4,7,9,12	1-3,5,6,8,10,11, 13-15	16	4,7,9,12	8	1-3,5,6,10,11,13-16
CD54HC/HCT259	4-7,9-12	1-3,8,13-15	16	4-7,9-12	8	1-3,13-16
CD54HC/HCT273	2,5,6,9,12, 15,16,19	1,3,4,7,8,10,11,13, 14,17,18	20	2,5,6,9,12, 15,16,19	10	1,3,4,7,8,11,13,14, 17,18,20
CD54HC/HCT280	3,5,6	1,2,4,7-13	14	3,5,6	7	1,2,4,8-14
CD54HC/HCT283	1,4,7,9,10,13	2,3,5,6,8,11,12, 14,15	16	1,4,7,9,10,13	8	2,3,5,6,11,12,14-16
CD54HC/HCT297	7,11,12	1-6,8-10,13-15	16	7,11,12	8	1-6,9,10,13-16
CD54HC/HCT299	8,17	1-7,9-16,18,19	20	8,17	10	1-7,9,11-16,18-20
CD54HC/HCT354	18,19	1-17	20	18,19	10	1-9,11-17,20
CD54HC/HCT356	18,19	1-17	20	18,19	10	1-9,11-17,20
CD54HC/HCT365	3,5,7,9,11,13	1,2,4,6,8,10,12, 14,15	16	3,5,7,9,11,13	8	1,2,4,6,10,12,14-16
CD54HC/HCT366	3,5,7,9,11,13	1,2,4,6,8,10,12, 14,15	16	3,5,7,9,11,13	8	1,2,4,6,10,12,14-16
CD54HC/HCT367	3,5,7,9,11,13	1,2,4,6,8,10,12, 14,15	16	3,5,7,9,11,13	8	1,2,4,6,10,12,14-16
CD54HC/HCT368	3,5,7,9,11,13	1,2,4,6,8,10,12, 14,15	16	3,5,7,9,11,13	8	1,2,4,6,10,12,14-16
CD54HC/HCT373	2,5,6,9,12, 15,16,19	1,3,4,7,8,10,11,13, 14,17,18	20	2,5,6,9,12, 15,16,19	10	1,3,4,7,8,11,13,14, 17,18,20
CD54HC/HCT374	2,5,6,9,12, 15,16,19	1,3,4,7,8,10,11,13, 14,17,18	20	2,5,6,9,12, 15,16,19	10	1,3,4,7,8,11,13,14, 17,18,20
CD54HC/HCT377	2,5,6,9,12, 15,16,19	1,3,4,7,8,10,11,13, 14,17,18	20	2,5,6,9,12, 15,16,19	10	1,3,4,7,8,11,13,14, 17,18,20
CD54HC/HCT390	3,5-7, 9-11,13	1,2,4,8,12,14,15	16	3,5-7, 9-11,13	8	1,2,4,12,14-16
CD54HC/HCT393	3-6,8-11	1,2,7,12,13	14	3-6,8-11	7	1,2,12-14
CD54HC/HCT423	4,5,12,13	1-3,6-11,14,15	16	4,5,12,13	8	1-3,6-7,9-11,14-16

*Non-standard pin arrangement; connect pins marked (•) without using a resistor.

Static Burn-In Test-Circuit Connections

TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT533	2,5,6,9,12, 15,16,19	1,3,4,7,8,10,11,13, 14,17,18	20	2,5,6,9,12, 15,16,19	10	1,3,4,7,8,11,13,14, 17,18,20
CD54HC/HCT534	2,5,6,9,12,15 16,19	1,3,4,7,8,10,11,13, 14,17,18	20	2,5,6,9,12,15 16,19	10	1,3,4,7,8,11,13, 14,17,18,20
CD54HC/HCT540	11-18	1-10,19	20	11-18	10	1-9,19,20
CD54HC/HCT541	11-18	1-10,19	20	11-18	10	1-9,19,20
CD54HC/HCT563	12-19	1-11	20	12-19	10	1-9,11,20
CD54HC/HCT564	12-19	1-11	20	12-19	10	1-9,11,20
CD54HC/HCT573	12-19	1-11	20	12-19	10	1-9,11,20
CD54HC/HCT574	12-19	1-11	20	12-19	10	1-9,11,20
CD54HC/HCT583	6,7,9-11	1-5,8,12-15	16	6,7,9-11	8	1-5,12-16
CD54HC/HCT597	9	1-8,10-15	16	9	8	1-7,10-16
CD54HC/HCT640	2-9	1,10-19	20	—	10	1-9,11-18,19,20
CD54HC/HCT643	2-9	1,10-19	20	—	10	1-9,11-18,19,20
CD54HC/HCT646	4-11	1-3,12-23	24	—	12	1-11,13-24
CD54HC/HCT648	4-11	1-3,12-23	24	—	12	1-11,13-24
CD54HC/HCT670	6,7,9,10	1-5,8,11-15	16	6,7,9,10	8	1-5,11-16
CD54HC/HCT688	19	1-18	20	19	10	1-9,11-18,20
CD54HC/HCT4002	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD54HC/HCT4015	2-5,10-13	1,6-8,9,14,15	16	2-5,10-13	8	1,6,7,9,14,15,16
CD54HC/HCT4016	1-4,8-11	5-7,12,13	14	1-4,8-11	7	5,6,12-14
CD54HC/HCT4017	1-7,9-12	8,13-15	16	1-7,9-12	8	13-16
CD54HC/HCT4020	1-7,9,12-15	8,10,11	16	1-7,9,12-15	8	10,11,16
CD54HC/HCT4024	3-6,8-13	1,2,7	14	3-6,8-13	7	1,2,14
CD54HC/HCT4040	1-7,9,12-15	8,10,11	16	1-7,9,12-15	8	10,11,16
CD54HC/HCT4046	1,2,4,6,7, 10-13,15	3,5,8,9,14	16	1,2,4,6,7 10-13,15	8	3,5,9,14,16
CD54HC4049*	2,4,6,10,12, 13,15,16	3,5,7-9,11,14	1•	2,4,6,10,12, 13,15,16	8	1•,3,5,7,9,11,14
CD54HC4050*	2,4,6,10,12, 13,15,16	3,5,7-9,11,14	1•	2,4,6,10,12, 13,15,16	8	1•,3,5,7,9,11,14
CD64HC/HCT4051*	3	1,2,4-6,7•,8•,9-15	16	3	7•,8•	1,2,4-6,9-16
CD54HC/HCT4052*	3,13	1,2,4-6,7•,8•,9-12, 14,15	16	3,13	7•,8•	1,2,4-6,9-12,14-16
CD54HC/HCT4053*	4,14,15	1-3,5,6,7•,8•,9-13	16	4,14,15	7•,8•	1-3,5,6,9-13,16
CD54HC/HCT4059	23	1-22	24	23	12	1-11,13-22,24
CD54HC/HCT4060	1-7,9,10, 13-15	8,11,12	16	1-7,9,10, 13-15	8	11,12,16
CD54HC/HCT4066	1-4,8-11	5-7,12,13	14	1-4,8-11	7	5,6,12-14
CD54HC/HCT4067	1	2-23	24	1	12	2-11,13-24
CD54HC/HCT4075	6,9,10	1-5,7,8,11-13	14	6,9,10	7	1-5,8,11-14
CD54HC/HCT4094	4-7,9-14	1-3,8,15	16	4-7,9-14	8	1-3,15,16
CD54HC/HCT4316*	1,4,10,12	2,3,5-7,8•,9•,11, 13-15	16	1,4,10,12	8•,9•	2,3,5-7,11,13-16
CD54HC/HCT4351*	3,4,14	1,2,5-13,15-19	20	3,4,14	9,10	1,2,5-13,15-20
CD54HC/HCT4352*	3,4,14,15	1,2,5-13,16-19	20	3,4,14,17	9,10	1,2,5-8,11-13, 15,16,18-20
CD54HC/HCT4353*	3,5,14,18,19	1,2,4,6-13,15,16,17	20	3,5,14,18,19	9,10	1,2,4,6-8,11-13,15-17,20
CD54HC/HCT4510	2,6,7,11,14	1,3-5,8-10,12,13,15	16	2,6,7,11,14	8	1,3-5,8-10,12,13, 15,16
CD54HC/HCT4511	9-15	1-8	16	9-15	8	1-7,16
CD54HC/HCT4514	4-11,13-20	1-3,12,21-23	24	4-11,13-20	12	1-3,21-24
CD54HC/HCT4515	4-11,13-20	1-3,12,21-23	24	4-11,13-20	12	1-3,21-24

*Non-standard pin arrangement; connect pins marked (•) without using a resistor.

Static Burn-In Test-Circuit Connections

TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT4516	2,6,7,11,14	1,3-5,8-10,12,13,15	16	2,6,7,11,14	8	1,3-5,8-10,12,13, 15,16
CD54HC/HCT4518	3-6,11-14	1,2,7-10,15	16	3-6,11-14	8	1,2,7,9,10,15,16
CD54HC/HCT4520	3-6,11-14	1,2,7-10,15	16	3-6,11-14	8	1,2,7,9,10,15,16
CD54HC/HCT4538	1,2,6,7,9,10, 14,15	3-5,8,11-13	16	1,2,6,7,9,10, 14,15	8	3-5,11-13,16
CD54HC/HCT4543	9-15	1-8	16	9-15	8	1-7,16
CD54HC/HCT40102	14	1-13,15	16	14	8	1-13,15,16
CD54HC/HCT40103	14	1-13,15	16	14	8	1-13,15,16
CD54HC/HCT40104	12-15	1-11	16	12-15	8	1-7,9-11,16
CD54HC/HCT40105	10-15	1-9	16	10-15	8	1-7,9,16
CD54HC/HCT7046	1,2,4,6,7, 10-13,15	3,5,8,9,14	16	1,2,4,6,7, 10-13,15	8	3,5,9,14,16
CD54HC7266	3,4,10,11	1,2,5,6,7,8,9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12,13,14

Dynamic Burn-In Test-Circuit Connections

NOTE: Each pin except V_{CC} AND V_{SS} will have a resistor of 2k-47k ohms. In most cases, V_{SS} is at pin 7 (of 14-pin IC), pin 8 (of 16-pin IC), pin 9 (of 18-pin IC), pin 10 (of 20-pin IC), or pin 12 (of 24-pin IC) while V_{CC} is at the highest numbered pin. Exceptions are marked by an asterisk (*)

TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	OSCILLATOR 50 KHz	OSCILLATOR 25 KHz
CD54HC/HCT00	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—
CD54HC/HCT02	—	7	1,4,10,13	14	2,3,5,6,8,9,11,12	—
CD54HC/HCT03	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—
CD54HC/HCT04	—	7	2,4,6,8,10,12	14	1,3,5,7,9,11,13	—
CD54HCU04	—	7	2,4,6,8,10,12	14	1,3,5,7,9,11,13	—
CD54HC/HCT08	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—
CD54HC/HCT10	—	7	6,8,12	14	1-5,9-11,13	—
CD54HC/HCT11	—	7	6,8,12	14	1-5,9-11,13	—
CD54HC/HCT14	—	7	2,4,6,8,10,12	14	1,3,5,9,11,13	—
CD54HC/HCT20	3,11	7	6,8	14	1,2,4,5,9,10, 12,13	—
CD54HC/HCT21	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—
CD54HC/HCT27	—	7	6,8,12	14	1-5,9-11,13	—
CD54HC/HCT30	9,10,13	7	8	14	1-6,11,12	—
CD54HC/HCT32	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—
CD54HC/HCT42	—	8,12	1-7,9-11	16	14,15	13
CD54HC/HCT73*	—	11•	8,9,12,13	2,3,4•,6, 7, 10,14	1,5	—
CD54HC/HCT74	—	7	5,6,8,9	1,4,10,13,14	3,11	2,12
CD54HC/HCT75*	—	12•	1,8-11,14-16	5•	4,13	2,3,6,7
CD54HC/HCT85	—	1,8,10,11,13	5-7	2-4,16	12,15	9,14
CD54HC/HCT86	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—
CD54HC/HCT93*	4,6,7,13	2,3,10•	8,9,11,12	5•	14	1
CD54HC/HCT107	—	7	2,3,5,6	1,4,8,10,11, 13,14	9,12	—

*Non-standard pin arrangement; connect pins marked (•) without using a resistor.

Dynamic Burn-In Test-Circuit Connections

TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	OSCILLATOR	
					50 KHz	25 KHz
CD54HC/HCT109	—	8	6,7,9,10	1-3,5,11,13-16	4,12	—
CD54HC/HCT112	—	8	5-7,9	2-4,10-12, 14-16	1,13	—
CD54HC/HCT123	—	1,6,8,9,14	4,5,12,13	7,15,16	2,3,10,11	—
CD54HC/HCT125	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—
CD54HC/HCT126	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—
CD54HC/HCT132	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—
CD54HC/HCT137	—	4,5,8	7,9-15	3,6,16	2	1
CD54HC/HCT138	—	4,5,8	7,9-15	3,6,16	2	1
CD54HC/HCT139	—	1,8,15	4-7,9-12	16	2,14	3,13
CD54HC/HCT147	15	8	6,7,9,14	16	4,5,10,11,13	1-3,12
CD54HC/HCT151	1,3,7-9,12-15	5,6	2,4,16	11	10	—
CD54HC/HCT153	—	1,3,5,8,11, 13,15	7,9	4,6,10,12,16	14	2
CD54HC/HCT154	—	12,18-21	1-11,13-17	24	23	22
CD54HC/HCT157	—	8,15	4,7,9,12	16	2,3,5,6,10,11, 13,14	1
CD54HC/HCT158	—	8,15	4,7,9,12	16	2,3,5,6,10,11, 13,14	1
CD54HC/HCT160	—	4,6,8	11-15	1,3,5,7,9, 10,16	2	—
CD54HC/HCT161	—	4,6,8	11-15	1,3,5,7,9, 10,16	2	—
CD54HC/HCT162	—	4,6,8	11-15	1,3,5,7,9, 10,16	2	—
CD54HC/HCT163	—	4,6,8	11-15	1,3,5,7,9, 10,16	2	—
CD54HC/HCT164	—	7	3-6,10-13	9,14	8	1,2
CD54HC/HCT165	—	3-6,8,11-15	7,9	1,16	2	10
CD54HC/HCT166	—	2,4,6,8,10,12	13	3,5,9,11, 14-16	7	1
CD54HC/HCT173	—	1,2,8-10,15	3-6	16	7	11-14
CD54HC/HCT174	—	8	2,5,7,10,12,15	1,16	9	3,4,6,11,13,14
CD54HC/HCT175	—	8	2,3,6,7,10, 11,14,15	1,16	9	4,5,12,13
CD54HC/HCT181	—	4-6,8,12	9-11,13-17	3,24	1,2,18-23	7
CD54HC/HCT182	—	8	7,9-12	16	1-6,14,15	13
CD54HC/HCT190	—	1,4,5,8-10,15	2,3,6,7,12,13	11,16	14	—
CD54HC/HCT191	—	1,4,5,8-10,15	2,3,6,7,12,13	11,16	14	—
CD54HC/HCT192	—	1,8-10,14,15	2,3,6,7,12,13	4,11,16	5	—
CD54HC/HCT193	—	1,8-10,14,15	2,3,6,7,12,13	4,11,16	5	—
CD54HC/HCT194	—	7,8,10	12-15	1,3-6,9,16	11	2
CD54HC/HCT195	—	8,9	11-15	1-3,16	10	4-7
CD54HC/HCT221	—	1,6,8,9,14	4,5,12,13	7,15,16	2,3,10,11	—
CD54HC/HCT237	—	4,5,8	7,9-15	3,6,16	2	1
CD54HC/HCT238	—	4,5,8	7,9-15	3,6,16	2	1
CD54HC/HCT240	—	1,10,19	3,5,7,9,12,14, 16,18	20	2,4,6,8,11,13, 15,17	—
CD54HC/HCT241	1,10	3,5,7,9,12,14, 16,18	19,20	2,4,6,8,11,13, 15,17		—

*Non-standard pin arrangement; connect pins marked (•) without using a resistor.

Dynamic Burn-In Test-Circuit Connections

TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	OSCILLATOR	
					50 KHz	25 KHz
CD54HC/HCT242	2,12	3,5,7,13	8-11	4,6,14	1	—
CD54HC/HCT243	2,12	3,5,7,13	8-11	4,6,14	1	—
CD54HC/HCT244	—	1,10,19	3,5,7,9,12,14, 16,18	20	2,4,6,8,11,13, 15,17	—
CD54HC/HCT245	—	10	11-18	1,20	2-9	19
CD54HC/HCT251	—	1-4,7,8,13,15	5,6	9,12,14,16	11	10
CD54HC/HCT253	—	1,8,15	7,9	16	3-6,10-14	2
CD54HC/HCT257	—	8,15	4,7,9,12	16	2,3,5,6,10,11, 13,14	1
CD54HC/HCT258	—	8,15	4,7,9,12	16	2,3,5,6,10,11, 13,14	1
CD54HC/HCT259	—	2,3,8,14	4-7,9-12	16	13,15	1
CD54HC/HCT273	—	10	2,5,6,9,12,15, 16,19	1,20	11	3,4,7,8,13,14, 17,18
CD54HC/HCT280	3	7	5,6	14	1,2,4,8-13	—
CD54HC/HCT283	—	8	1,4,9,10,13	16	2,6,11,15	3,5,7,12,14
CD54HC/HCT297	—	8,11,12	1,2,4,13,15	16	3,5,9,10,13,14	6,7
CD54HC/HCT299	—	2,3,10,18,19	4-8,13-17	1,9,20	12	11
CD54HC/HCT354	—	1-4,6,8-12, 15,16	18,19	5,7,17,20	14	13
CD54HC/HCT356	—	1-6,8,10-13, 15,16	18,19	7,17,20	9	14
CD54HC/HCT365	—	1,8,15	3,5,7,9,11,13	16	2,4,6,10,12,14	—
CD54HC/HCT366	—	1,8,15	3,5,7,9,11,13	16	2,4,6,10,12,14	—
CD54HC/HCT367	—	1,8,15	3,5,7,9,11,13	16	2,4,6,10,12,14	—
CD54HC/HCT368	—	1,8,15	3,5,7,9,11,13	16	2,4,6,10,12,14	—
CD54HC/HCT373	—	1,10	2,5,6,9,12,15, 16,19	20	11	3,4,7,8,13,14, 17,18
CD54HC/HCT374	—	1,10	2,5,6,9,12,15 16,19	20	11	3,4,7,8,13,14, 17,18
CD54HC/HCT377	—	1,10	2,5,6,9,12,15 16,19	20	11	3,4,7,8,13,14, 17,18
CD54HC/HCT390	—	8	3,5-7,9-11,13	2,14,16	1,4,12,15	—
CD54HC/HCT393	—	7	3-6,8-11	2,12,14	1,13	—
CD54HC/HCT423	—	2,6,8,10,14	4,5,12,13	7,15,16	1,9	3,11
CD54HC/HCT533	—	1,10	2,5,6,9,12,15, 16,19	20	11	3,4,7,8,13,14 17,18
CD54HC/HCT534	—	1,10	2,5,6,9,12,15, 16,19	20	11	3,4,7,8,13,14, 17,18
CD54HC/HCT540	—	10	11-18	20	1,19	2-9
CD54HC/HCT541	—	10	11-18	20	1,19	2-9
CD54HC/HCT563	—	1,10	12-19	20	11	2-9
CD54HC/HCT564	—	1,10	12-19	20	11	2-9
CD54HC/HCT573	—	1,10	12-19	20	11	2-9
CD54HC/HCT574	—	1,10	12-19	20	11	2-9
CD54HC/HCT583	—	8	6,7,9-11	16	4,13-15	1-3,5,12
CD54HC/HCT597	—	8,9,14	1-6,15	16	7,11,12	10,13
CD54HC/HCT640	—	10	11-18	1,20	2-9	19
CD54HC/HCT643	—	10	11-18	1,20	2-9	19
CD54HC/HCT646	—	1-3,12,21,22	4-11	24	23	13-20
CD54HC/HCT648	—	1-3,12,21,22	4-11	24	23	13-20
CD54HC/HCT670	—	8,11,12	6,7,9,10	16	1-3,5,14,15	4,13
CD54HC/HCT688	—	1,2,4,6,8,10, 11,13,15,17	19	20	3,5,7,9,12,14 16,18	—

*Non-standard pin arrangement; connect pins marked (•) without using a resistor.

Dynamic Burn-In Test-Circuit Connections

TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	OSCILLATOR 50 KHz	OSCILLATOR 25 KHz
CD54HC/HCT4002	6,8	7	1,13	14	2-5,9-12	—
CD54HC/HCT4015	—	6,8,14	2-5,10-13	16	1,9	7,15
CD54HC/HCT4016	—	7	2,3,9,10	14	5,6,12,13	1,4,8,11
CD54HC/HCT4017	—	8,13,15	1-7,9-12	16	14	—
CD54HC/HCT4020	—	8,11	1-7,9,12-15	16	10	—
CD54HC/HCT4024	8,10,13	2,7	3-6,9,11,12	14	1	—
CD54HC/HCT4040	—	8,11	1-7,9,12-15	16	10	—
CD54HC/HCT4046	1,4,6,7,10,11, 13,15	8,9	2	3,5,12,16	14	—
CD54HC4049*	13	8	2,4,6,10,12,15	1•,16	3,5,7,9,11,14	—
CD54HC4050*	13	8	2,4,6,10,12,15	1•,16	3,5,7,9,11,14	—
CD54HC/HCT4051*	—	4-6,7•,8•,9, 12,14	3	1,2,13,15,16	11	10
CD54HC/HCT4052*	—	4-6,7•,8•, 12,15	3,13	1,2,11,14,16	10	9
CD54HC/HCT4053*	—	1,5,6,7•,8•,12	4,14,15	2,3,13,16	9-11	—
CD54HC/HCT4059	—	2,4,5,8,9,11,12 16,17,20,21	23	3,6,7,10,13,14 15,18,19,22,24	1	—
CD54HC/HCT4060	—	8,12	1-7,9,10, 13-15	16	11	—
CD54HC/HCT4066	—	7	2,3,9,10	14	5,6,12,13	1,4,8,11
CD54HC/HCT4067	—	12,15	1	24	2-9,16-23	(10,11,13,14)[1]
CD54HC/HCT4075	—	7	6,9,10	14	1-5,8,11-13	—
CD54HC/HCT4094	—	8	4-7,9-14	1,15,16	3	2
CD54HC/HCT4316*	—	3,8•,9•	2,3,11,12	16	5,6,14,15	1,4,10,13
CD54HC/HCT4351*	3,14	1,2,6,7,9,10, 17-19	4	5,8,11,15,16,20	13	12
CD54HC/HCT4352*	3,14	1,2,7,9,10,16, 19	4,17	5,6,8,11,15,18, 20	13	12
CD54HC/HCT4353*	3,14	2,6,7,9,10,16	5,18,19	1,4,8,11,17,20	13,15	12
CD54HC/HCT4510	—	1,3,4,8,9, 12,13	2,6,7,11,14	10,16	15	5
CD54HC/HCT4511	9-15	5,8	—	3,4,16	1,2,7	6
CD54HC/HCT4514	—	2,3,12	4-11,13-20	21,22,24	1	23
CD54HC/HCT4515	—	2,3,12	4-11,13-20	21,22,24	1	23
CD54HC/HCT4516	—	1,3,4,8,9, 12,13	2,6,7,11,14	10,16	15	5
CD54HC/HCT4518	—	7,8,15	3-6,11-14	2,10,16	1,9	—
CD54HC/HCT4520	—	7,8,15	3-6,11-14	2,10,16	1,9	—
CD54HC/HCT4538	—	1,4,8,12,15	6,7,9,10	2,14,16	5,11	3,13
CD54HC/HCT4543	—	6-8	9-15	1,4,16	2,3,5	—
CD54HC/HCT40102	—	3,8,15	14	2,16	1,4,6,11,13	5,7,9,10,12
CD54HC/HCT40103	—	3,8,15	14	2,16	1,4,6,11,13	5,7,9,10,12
CD54HC/HCT40104	—	7,8,10	12-15	1,3-6,9,16	11	2
CD54HC/HCT40105	—	1,8,9	2,10-14	16	3,15	4-7
CD54HC/HCT7046	1,4,6,7,10, 11,13,15	8,9	2	3,5,12,16	14	—
CD54HC7266	—	7	3,4,10,11	14	1,5,8,12	2,6,9,13

*Non-standard pin arrangement; connect pins marked (•) without using a resistor.
[1]Pin 10 is at 14 kHz, pin 11 is at 7 kHz, pin 13 is at 1.7 kHz, and pin 14 is at 3.5 kHz.

Leadless-Chip-Carrier Pinout

The following table and diagrams show JEDEC standard pinout conversions from 14-, 16-, 18-, 20-, and 24-pin leaded frit packages to 20- and 28-terminal leadless-chip carriers.

RCA CD54HC/HCT slash-series products offered in leadless-chip carriers are shown below.

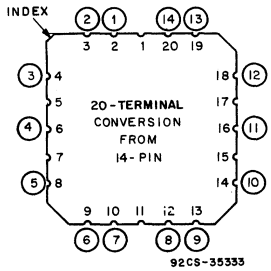
Pinout Conversion From Frit Package to Leadless-Chip Carrier

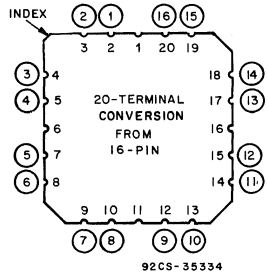
Frit Device Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
LCC Pin No. For:																								
14-Pin Frit	2	3	4	6	8	9	10	12	13	14	16	18	19	20										
16-Pin Frit	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20								
18-Pin Frit	2	3	4	5	6	7	8	9	10	12	13	14	15	16	17	18	19	20						
20-Pin Frit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20				
24-Pin Frit	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28

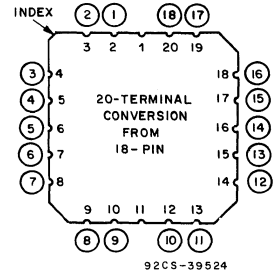
CD54HC/HCT Slash-Series Conversion Diagrams

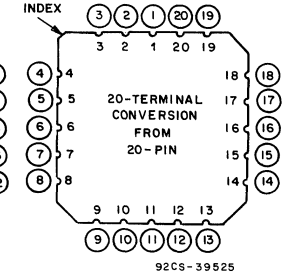
(Top Views Shown)

20-Terminal Leadless-Chip Carriers

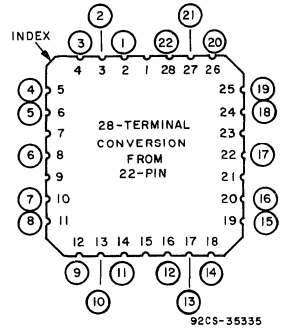








28-Terminal Leadless-Chip Carrier



High-Reliability CA3000 Slash-Series Linear ICs

RCA High-Reliability CA3000 Slash-Series Linear ICs

RCA-CAXXXX "Slash" (/) Series types are high-reliability linear integrated circuits intended for applications in aerospace, military, and industrial equipment. These devices are electrically and mechanically identical to the standard types described in commercial databook SSD-240C entitled "Linear Integrated Circuits and MOSFETs", but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microcircuit devices.

The standard package types and screening levels available for individual devices can be found in the nomenclature guide. Screening levels /1,/3, and /3W are based on guidelines established for military product. For detailed screening sequences, see the Product Quality-Assurance Procedures table. Chip versions of the standard product and quality conformance packages are offered on a custom basis only.

Electrical characteristics may be found in RCA data bulletins on specific slash (/) series types. For applications information refer to RCA databooks SSD-240C, "Linear Integrated Circuits and MOSFETs," and SSD-245, "Applications-Linear Integrated Circuits and MOSFETs."

Radiation Effects on Linear ICs

There is no dedicated process for radiation hardening of the Linear ICs. Gammacell exposure of various devices representing both the bipolar and BiMOS water technologies has resulted in information useful for design guidance when considering radiation hardness.

Devices processed under bipolar technologies tend to withstand Gamma radiation to exposure levels of 1×10^5 rads(Si) prior to experiencing significant parameter degradation, while those processed with BiMOS techniques can withstand Gamma Ray exposure levels up to 1×10^4 rads(Si) before parameter degradation takes place. RCA does not guarantee rad-hard levels for linear IC's but will conduct rad-hard testing on a custom basis.

Screening Levels for RCA High-Reliability CA3000 Slash-Series Linear ICs

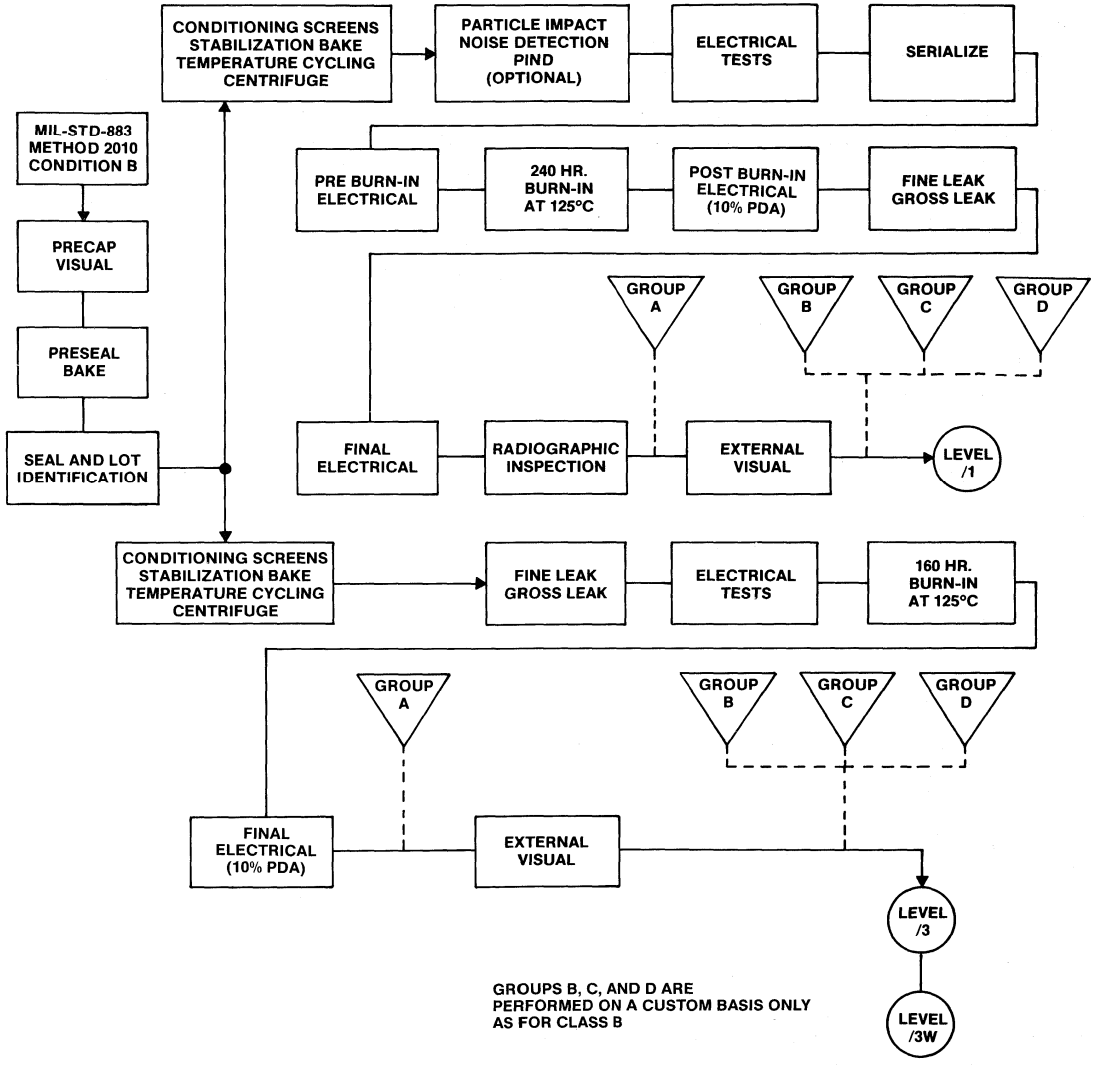
TYPE	SCREENING LEVEL (/)			PACKAGE CODE**				# OF LEADS	TYPE	SCREENING LEVEL (/)			PACKAGE CODE**				# OF LEADS
CA723	1	3	-	T	-	-	-	10	CA3082	1	3	-	-	-	-	F	16
CA741	1	3	-	T	S	-	-	8	CA3083	-	-	3W	-	-	-	F	16
CA747	1	3	-	T	S	-	-	10	CA3085	1	3	-	T	S	-	-	8
CA748	1	3	-	T	S	-	-	8	CA3085A	1	3	-	T	S	-	-	8
CA1558	1	3	-	T	S	-	-	8	CA3085B	1	3	-	T	S	-	-	8
CA3000	1	3	-	T	-	-	-	10	CA3089	-	-	3W	-	-	-	F	16
CA3001	1	3	-	T	-	-	-	12	CA3094	1	3	-	T	S	-	-	8
CA3002	1	3	-	T	-	-	-	10	CA3094A	1	3	-	T	S	-	-	8
CA3006	1	3	-	T	-	-	-	12	CA3100	1	3	-	T	S	-	-	8
CA3015	1	3	-	T	-	-	-	12	CA3118A	1	3	-	T	-	-	-	12
CA3015A	1	3	-	T	-	-	-	12	CA3130	1	3	-	T	S	-	-	8
CA3018	1	3	-	T	-	-	-	12	CA3130A	1	3	-	T	S	-	-	8
CA3018A	1	3	-	T	-	-	-	12	CA3140	1	3	-	T	S	-	-	8
CA3019	1	3	-	T	-	-	-	10	CA3140A	1	3	-	T	S	-	-	8
CA3020	1	3	-	T	-	-	-	12	CA3160	1	3	-	T	S	-	-	8
CA3020A	1	3	-	T	-	-	-	12	CA3160A	1	3	-	T	S	-	-	8
CA3026	1	3	-	T	-	-	-	12	*CA3193	1	3	-	T	S	-	-	8
CA3028B	1	3	-	T	S	-	-	8	*CA3193A	1	3	-	T	S	-	-	8
CA3038A	1	3	-	-	-	D	-	14	*CA3260	1	3	-	T	S	-	-	8
CA3039	1	3	-	T	-	-	-	12	*CA3260A	1	3	-	T	S	-	-	8
CA3040	1	-	3W	T	-	-	-	12	*CA3290A	1	3	-	T	S	-	-	8
CA3045	1	3	-	-	-	D	F	14	*CA3300	-	3	-	-	-	D	-	18
CA3049	1	3	-	T	-	-	-	12	*CA3306	-	3	3W	-	-	D	-	18
CA3058	1	3	-	-	-	D	-	14	CA6741	1	3	-	T	S	-	-	8
CA3078	1	3	-	T	S	-	-	8	HR3N187	-	-	3W	T	-	-	-	4
CA3078A	1	3	-	T	S	-	-	8	HR3N200	-	-	3W	T	-	-	-	4
CA3080	1	3	-	T	S	-	-	8									
CA3080A	1	3	-	T	S	-	-	8									
CA3081	1	3	-	-	-	-	F	16									

*Denotes type to be introduced as a High-Reliability device sometime in 1985.

**Package Designations: T = TO-5 Metal Can
S = TO-5 Metal Can with DIL Formed Leads
D = Weld-Seal DIL White Ceramic
F = Frit-Seal DIL Ceramic

Screening

Product Flow Diagram



Guide to High-Reliability Linear Integrated Circuit Nomenclature

CA3130 T /3 *

PART NUMBER	PACKAGE DESIGNATION	RELIABILITY SCREENING LEVEL
CA3130	D — DUAL-IN-LINE METAL-SEAL CERAMIC F — DUAL-IN-LINE FRIT-SEAL CERAMIC T — TO-5 METAL CAN S — DIL FORMED TO-5	/1 — MODIFIED CLASS S /3 — MODIFIED CLASS B /3W — MODIFIED CLASS B WITHOUT HIGH & LOW TEMPERATURE DC

* Example

Product Quality-Assurance Procedures

Listed Test Methods are per MIL-STD-883

Characteristic [1]	/1		/3, (/3W)[2]	
Package Options	T,S,D[3]	F	T,S,D[3]	F
Die Attach	Epoxy	Eutectic	Epoxy	Eutectic
Lead Finish	Solder Dip	Tin Reflowed	Solder Dip	Tin Reflowed
Manufacturing Location	U.S.	U.S.	Offshore	Offshore
Assembly: Precap visual - Cond. B	2010[4,5]	2010[4,5]	2010	2010
Stabilization Bake	1008 Cond. C			
Temp. Cycling	1010 Cond. C			
Centrifuge	2001 Cond. E, Y_1 direction only			
PIND TEST[6]	2020	2020	—	—
Pre-burn-in Electrical Test	Group A - Subgroup 1 Electrical tests @ 25°C			
Serialize	X	X	—	—
Electrical Tests[7]	X	X		
Burn-in[8] 240 Hrs.	X	X		
160 Hrs.			X	X
Post burn-in Electrical-tests[9]	Group A - Subgroup 1 Electrical tests @ 25°C			
PDA 10%	X	X	X	X
Final Electrical Tests[10]	Group A - Subgroups 2, 3, 4, Electrical tests			
Seal				
Fine (Cond. A)	1014			
Gross (Cond. C)	1014			
X-Ray Insp. (1 View)	2012	2012	—	—
External Visual	2009			
Quality Conformance				
Group A	EACH LOT			
Group B, C, D	AS ORDERED			

Notes:

1. Any exceptions will be called out in the applicable Device Data Sheet.
2. /3W has same procedures as /3 except no final electrical tests @ T_A+ +125 °C and T_A = -55° C.
3. As a custom option, leadless chip carrier is offered.
4. For /1 product, SEM Inspection per Method 2018 is offered as a custom option.
5. For /1 product, Visual Inspection per Method 2010 Cond. A is offered as a customer option.
6. PIND test is offered as a custom option.
7. Test and record parameters for specified delta's as part of post burn-in tests.
8. Burn-in circuits and burn-in conditions are given in applicable data sheets. D-MOS devices are burned in @ T_A = 25°C with full power dissipated.
9. For /1 devices, delta calculations are considered in evaluation of the PDA.
10. Applicable data sheets list all Group A tests. Subgroup 2 tests are done at 125°C, Subgroup 3 tests are done at -55°C, and Subgroup 4 tests are done at 25°C.

Data Supplied with Order for Packaged Devices

Product Screening Data	/1		/3, (/3W)*	
	T,S,D	F	T,S,D	F
Certificate of Compliance	X	X	X	X
Variables with Delta Calculations	X	X	—	—
Group A Attributes	X	X	—	—
Group B Attributes	as ordered			
Group C Variables	as ordered			
Group D Attributes	as ordered			
X-Ray Film	X	X	—	—
SEM - Photo	as ordered		—	—

*/3W has same procedures as /3 except no final electrical tests @ T_A = +125° C and T_A = -55° C.

High-Reliability Voltage Regulators

For Regulated Output Voltages Adjustable from 2 V to 37 V
at Currents up to 150 mA Without External Pass Transistors
In Aerospace, Military, and Critical Industrial Equipment

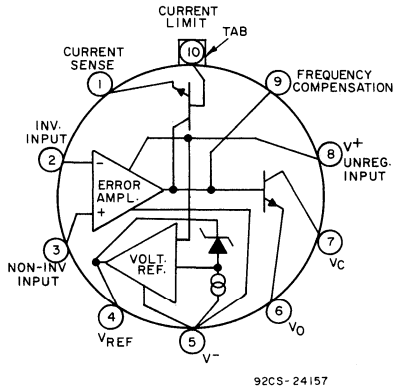
Features:

- **Up to 150 mA output current**
- **Positive and negative voltage regulation**
- **Regulation in excess of 10 A with suitable pass transistors**
- **Input and output short-circuit protection**
- **Load and line regulation: 0.03%**
- **Direct replacement for 723 industry types**
- **Adjustable output voltage: 2 to 37 V**

Applications

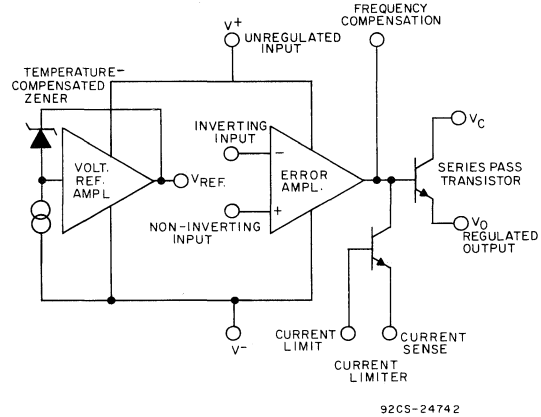
- **Series and shunt voltage regulator**
- **Floating regulator**
- **Switching voltage regulator**
- **High-current voltage regulator**
- **Temperature controller**

The CA723 is supplied in the 10-Lead TO-5 style ceramic package (T suffix), and is a direct replacement for industry type 723 in packages with similar terminal arrangements. It is also available in chip form (H suffix).



92CS-24157

Terminal arrangement of the CA723T in the TO-5 style package.



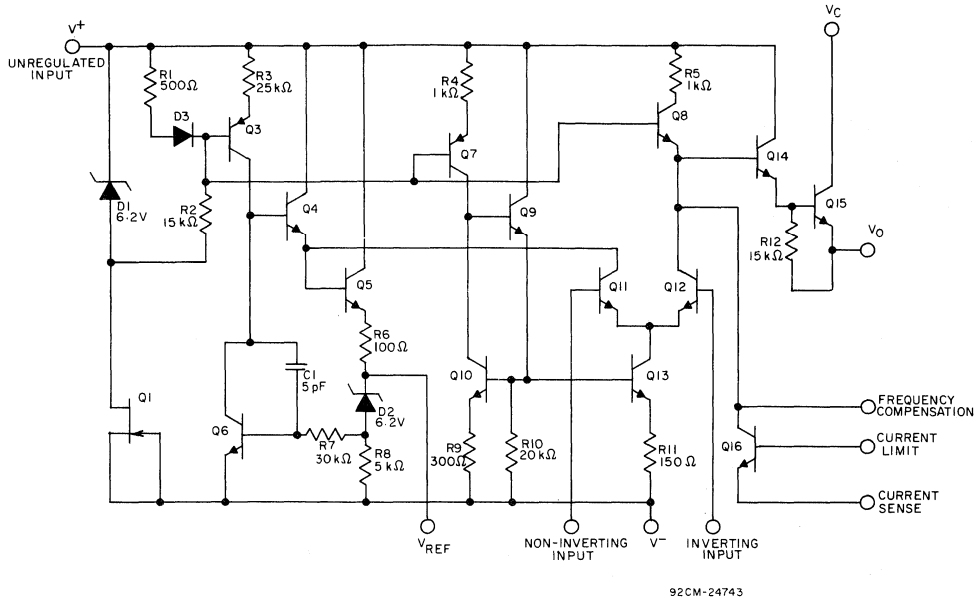
92CS-24742

Functional diagram of the CA723.

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) ..... 40 V
PULSE VOLTAGE FOR 50-ms PULSE WIDTH
(BETWEEN V^+ AND V^- TERMINALS) ..... 50 V
DIFFERENTIAL INPUT-OUTPUT VOLTAGE ..... 40 V
DIFFERENTIAL INPUT VOLTAGE:
BETWEEN INVERTING AND NON-INVERTING INPUTS ..... ±5 V
BETWEEN NON-INVERTING INPUT AND V^- ..... 8 V
CURRENT FROM VOLTAGE REFERENCE TERMINAL (V_{REF}) ..... 15 mA
DEVICE DISSIPATION:
UP TO T_A = 25°C
CA723T ..... 800 mW
ABOVE T_A = 25°C
CA723T ..... Derate linearly 6.3 mW/°C
AMBIENT TEMPERATURE RANGE:
OPERATING ..... -55 to +125°C
STORAGE ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At a distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

CA723T/...



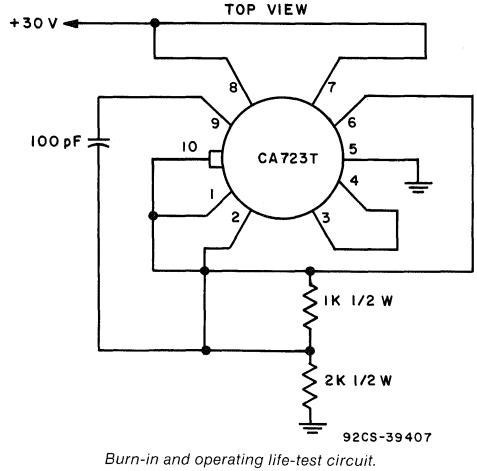
Equivalent schematic diagram of the CA723.

Table I. Pre Burn-In Electrical Post Burn-In Electrical Tests, and Delta Limits*

ELECTRICAL CHARACTERISTICS, *at T_A = 25°C*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX.Δ	
Reference Voltage	V_{REF}		6.95	7.35	±0.05	V
Quiescent Regulator Current	I_Q	I_L = 0 V_I = 30V	–	3.5	±0.5	mA

* Level /1 requires pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in test only. The burn-in and operating life test circuit is shown below.



Burn-in and operating life-test circuit.

Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS (See Note) T_A=25°C, V_I=V^+=V_C=12V, V^-=0, V_O=5V, I_L=1mA, C_I=100pF, $Z_{DIVIDER}$≤10kΩ (into error amplifier as shown in Fig. 13) unless otherwise indicated	LIMITS						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
Quiescent Regulator Current	I_Q	I_L = 0, V_I = 30 V	–	–	–	–	3.5	–	mA
Input Voltage Range	V_I		–	9.5	–	–	40	–	V
Output Voltage Range	V_O		–	2.0	–	–	37	–	V
Differential Input-Output Voltage	V_I–V_O		–	3.0	–	–	38	–	V
Reference Voltage	V_{REF}		–	6.95	–	–	7.35	–	V
Line Regulation		V_I = 12 to 40 V	–	–	–	–	0.2	–	%V_O
		V_I = 12 to 15 V	–	–	–	0.3	0.1	0.3	
Load Regulation		I_L = 1 to 50 mA	–	–	–	0.6	0.15	0.6	%V_O

Note: Line and load regulation specifications are given for condition of a constant chip temperature: for high dissipation conditions, temperature drifts must be separately taken into account.

Groups C and D Electrical Characteristics Sampling Tests (End-point Tests)
(T_A = 25° C, V_{CC} +6 V, V_{EE} = -6 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Reference Voltage	V_{REF}		6.95	7.35	V
Line Regulation		V_I = 12 to 15 V	–	0.15	%V_O
Load Regulation		I_L = 1 to 50 mA	–	0.2	%V_O
Quiescent Regulator Current	I_Q	I_L = 0 V_I = 30 V	–	3.5	mA

CA741/..., CA747/..., CA748/..., CA1558/...

High-Reliability Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers
For Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Input bias current (all types): 500 nA max.**
- **Input offset current (all types): 200 nA max.**

Applications:

- **Comparator**
- **DC amplifier**
- **Integrator or differentiator**
- **Multivibrator**
- **Narrow-band or band-pass filter**
- **Summing amplifier**

The CA741, CA748, and CA1558 Slash (/) Series types are supplied in the 8-lead TO-5 style package ("T" suffix) and in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN ("S" suffix). The CA747 is supplied in the 10-lead TO-5 style package ("T" suffix). All the types are also available in chip form ("H" suffix).

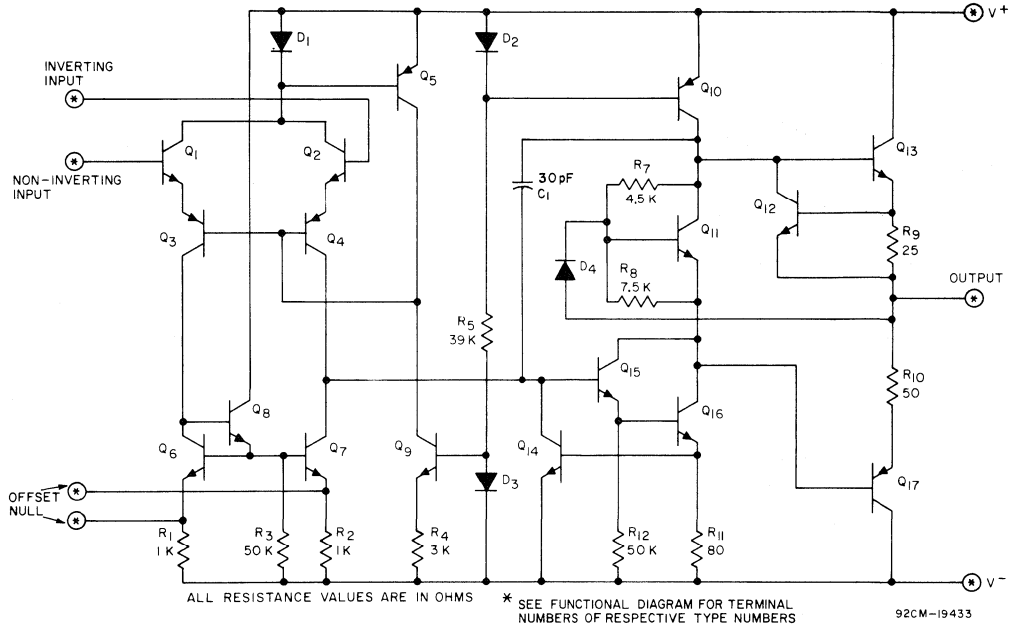
RCA* TYPE NO.	NO. OF AMPLI.	PHASE COMP.	PACKAGE TYPE	OFFSET VOLT. NULL	A_{OL} (MIN.)	V_{IO} (MAX.)	T_A OPERATING RANGE	COMPATIBLE WITH INDUSTRY TYPE(S)
CA1558T	dual	internal	8-lead TO-5	no	50,000	5 mV	−55 to 125°C	MC1558, S5558
CA741	single	internal	8-lead TO-5	yes	50,000	5 mV	−55 to 125°C	μA741
CA747	dual	internal	10-lead TO-5	no	50,000	5 mV	−55 to 125°C	μA747
CA748	single	external	8-lead TO-5	yes	50,000	5 mV	−55 to 125°C	μA748

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

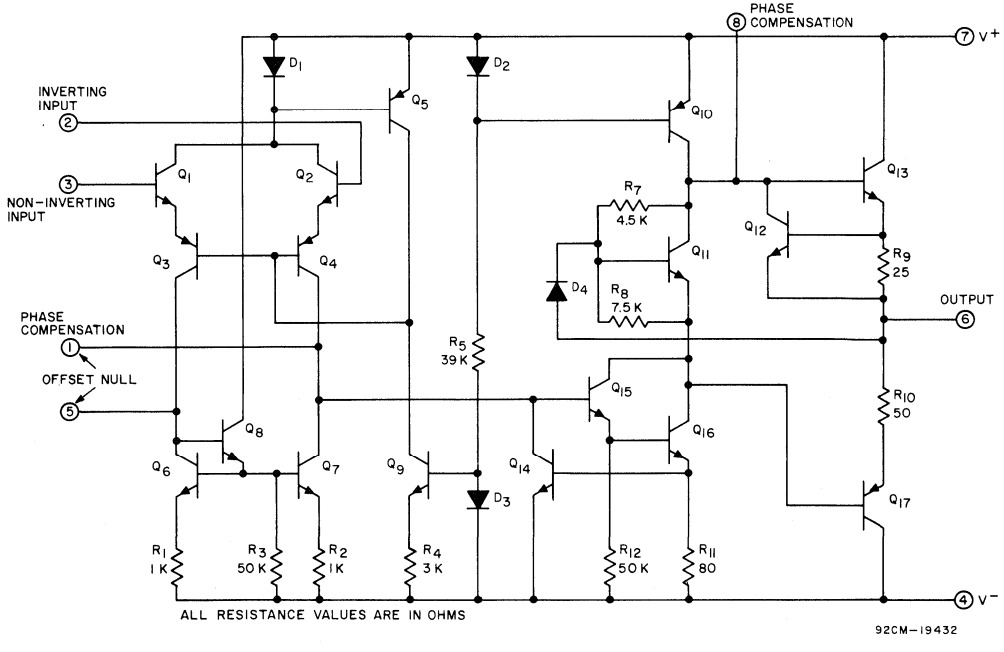
DC SUPPLY VOLTAGE (between V^+ and V^- terminals):
CA741T, CA747T▲, CA748T, CA1558T▲ . . . . . 44 V
Differential Input Voltage . . . . . ±30 V
DC Input Voltage* . . . . . ±15 V
Output Short-Circuit Duration . . . . . Indefinite
DEVICE DISSIPATION:
Up to 75°C (CA741T, CA748T) . . . . . 500 mW
Up to 30°C (CA747T) . . . . . 800 mW
Up to 30°C (CA1558T) . . . . . 680 mW
Above indicated temperatures . . . . . Derate linearly 6.67 mW/°C
Voltage between Offset Null and V^-CA741T . . . . . ±0.5 V
TEMPERATURE RANGE:
Operating . . . . . -55 to +125°C
Storage . . . . . -65 to +150 °C
LEAD TEMPERATURE (During Soldering)
At distance 1/16±1/31 inch (1.59±0.79 mm) from case for 10 seconds max . . . . . +265 °C

*If Supply voltage is less than ± 15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.
▲Voltage values apply for each of the dual operational amplifiers.

CA741/..., CA747/..., CA748/..., CA1558/...

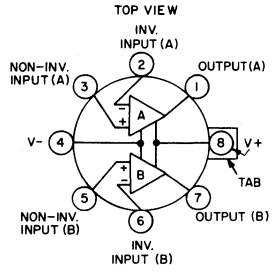


Schematic diagram of operational amplifiers with internal phase compensation for CA741T and for each amplifier of the CA747T and CA1558T.

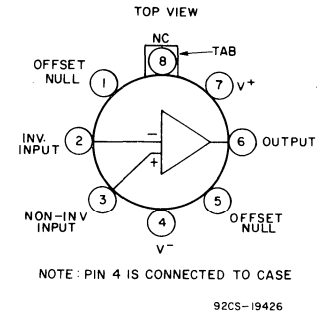


Schematic diagram of operational amplifier with external phase compensation for CA748T.

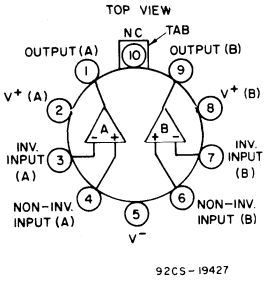
CA741/..., CA747/..., CA748/..., CA1558/...



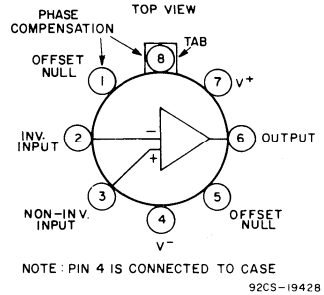
Functional diagram of CA1558T with internal phase compensation.



Functional diagram of CA741T with internal phase compensation.

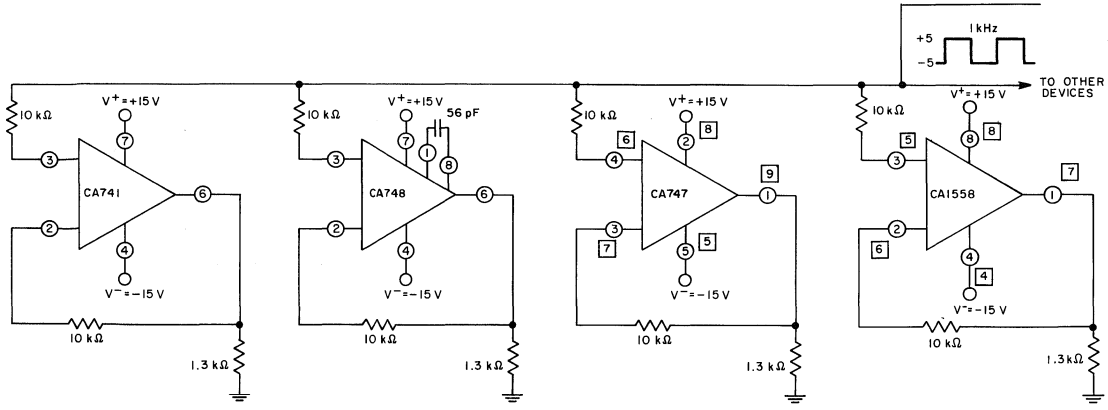


Functional diagram of CA747T with internal phase compensation.



Functional diagram of CA748T with external phase compensation

Functional diagrams of operational amplifiers.



Burn-in and operating life-test circuit for CA741, CA747, CA748, and CA1558.

CA741/..., CA747/..., CA748/..., CA1558/...

Pre Burn-in Electrical and Post Burn-in Electrical Tests, and Delta Limits* For All Types

ELECTRICAL CHARACTERISTICS, *at T_A = 25°C, V^+ = +15V, V^- = -15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Input Offset Voltage	V_{IO}		–	5	±1	mV
Input Offset Current	I_{IO}		–	200	±24	nA
Input Bias Current	I_I		–	500	±60	nA
Device Dissipation	P_D			85	±18	mW

* Level /1 requires pre burn-in electrical and post burn-in electrical tests, and data limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown on the previous page.

Group A Electrical Sampling Inspection For All Types

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+ = +15 V, V = -15 V	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
STATIC									
Input Offset Voltage	V_{IO}	–	–	–	–	6	5	6	mV
Input Offset Current	I_{IO}	–	–	–	–	500	200	200	nA
Input Bias Current	I_I	–	–	–	–	1500	500	500	nA
Supply Current		–	–	–	–	3.8	3.8	2.5	mA
Device Dissipation	P_D	–	–	–	–	100	85	75	mW
DYNAMIC									
Open-Loop Differential Voltage Gain	A_{OL}	–	25000	50000	25000	–	–	–	
Common-Mode Rejection Ratio	CMRR	–	70	70	70	–	–	–	dB
Maximum Output-Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\ k\Omega$ $R_L \geq 2\ k\Omega$	±12 ±10	±12 ±10	±12 ±10	– –	– –	– –	V
Common-Mode Input-Voltage Range	V_{ICR}	–	±12	±12	±12	–	–	–	V

Groups C and D Electrical Characteristics Sampling Tests (End-point Tests)

T_A = +25°C V_{CC} = +12V V_{EE} = -12V

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Input Offset Voltage	V_{IO}	—	—	8	mV
Input Offset Current	I_{IO}	—	—	240	μA
Input Bias Current	I_I	—	—	800	μA
Open-Loop Differential Voltage Gain	A_{OL}	f = 1 kHz	33000	—	
Supply Current			—	3	mA

CA3000/...

High-Reliability DC Amplifier

For Applications in Aerospace, Military and Critical Industrial Equipment

Features:

- **Input Impedance . . . . . 195 KΩ typ.**
- **Voltage Gain . . . . . 37 dB typ.**
- **Common-Mode Rejection Ratio . . . . . 98 dB typ.**
- **Input Offset Voltage . . . . . 1.4 mV typ.**
- **Push-Pull Input and Output**
- **Frequency Capability**
  DC to 30 MHz (with external C and R)
- **Wide AGC Range . . . . . 90 dB typ.**

Applications

- **Schmitt Trigger**
- **RC-Coupled Feedback Amplifier**
- **Mixer**
- **Comparator**
- **Modulator**
- **Crystal Oscillator**
- **Sense Amplifier**
- **See Companion Application Note ICAN-5030. "Applications of RCA-CA3000 IC DC Amplifier."**

The CA3000 Slash (/) Series type is supplied in the 10-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Absolute Maximum Voltage and Current Limits at $T_A = 25^\circ$ C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 9 is 0 to −12 volts.

Terminal No.	1	2	3	4	5	6	7	8	9	10
1		*	+16▲ 0	*	*	+4 -4	Internal Connection Do not use	*	0 -12	+1 -12
2			+16 -5	*	*	*		*	0 -16	*
3				+5 -5	+5 -10	0 -16		*	0 -16	*
4					*	*		*	0 -16	*
5						*		*	0 -16	*
6								+1 -12	0 -12	*
7	Internal Connection Do not use									
8									0 -16	*
9										+16 0
10										
Case	Connected to Terminal #3 – Do Not Ground									

Maximum Current Ratings

Terminal No.	I_{IN} mA	I_{OUT} mA
1	1	0.1
2	–	–
3	–	–
4	–	–
5	1	0.1
6	–	–
7	–	–
8	–	–
9	–	–
10	–	–

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

▲ This rating applies to the more positive of Terminals #1 or #6.

MAXIMUM RATINGS, *Absolute-Maximum Values*

OPERATING-TEMPERATURE RANGE ..... -55° C to +125° C
STORAGE-TEMPERATURE RANGE ..... -65° C to +150° C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE ..... ±2 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE ..... ±2 V
MAXIMUM DEVICE DISSIPATION ..... 300 mW
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... 265° C

Group A Electrical Sampling Inspection

Characteristics	Symbol	Test Conditions $V^+ = +6$ V, $V^- = -6$ V		Limits for Indicated Temp. (°C)						Units
				Minimum			Maximum			
				-55	+25	+125	-55	+25	+125	
STATIC										
Input Offset Voltage	V_{IO}	–		–	–	–	6.5	5	6.5	mV
Input Offset Current	I_{IO}	–		–	–	–	20	10	20	μA
Input Bias Current	I_I	–		–	–	–	70	36	25	μA
Quiescent Operating Voltage	V_8 or V_{10}	Terminal 4	Terminal 5							
		NC	NC	1.5	1.5	1.5	3.2	3.2	3.2	V
Device Dissipation	P_T	Terminal 4	Terminal 5							
		NC	NC	30	25	20	60	60	50	mW
		NC	$-V_{EE}$	25	20	15	55	55	50	mW
		$-V_{EE}$	NC	55	50	45	105	105	90	mW
		$-V_{EE}$	$-V_{EE}$	35	35	25	70	70	65	mW
DYNAMIC										
Differential Voltage Gain	A_{Diff}	*	Single-Ended Output	–	28	–	–	–	–	dB
			Double-Ended Output	–	33	–	–	–	–	dB
Maximum Output Voltage	V_{OUT} (p-p)			–	5	–	–	–	–	V_{p-p}
Bandwidth at -3 dB Point	BW			–	600	–	–	–	–	kHz
Common-Mode Rejection Ratio	CMR			–	70	–	–	–	–	dB
AGC Range (Maximum Voltage Gain to Complete Cut-off)	AGC			–	80	–	–	–	–	dB

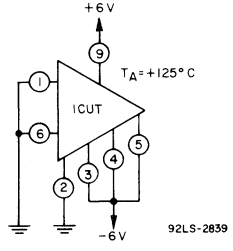
** Not tested but guaranteed.*

CA3000/...

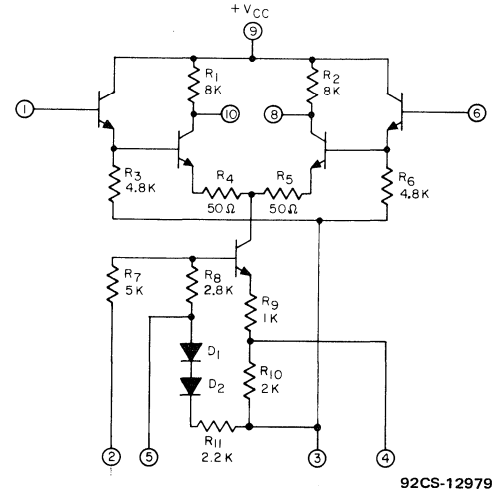
Pre Burn-in Electrical and Post Burn-in Electrical Tests, and Delta Limits*

Electrical Characteristics, at T_A = 25° C, V^+ = +6 V, V^- = -6 V						
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Input Bias Current	I_I	–	–	36	±4	μA
Quiescent Operating Voltage	V_8 or V_{10}	Terminal 4: NC Terminal 5: NC	1.5	3.2	±0.3	V
Device Dissipation	P_T	Terminal 4: NC Terminal 5: NC	25	60	±6	mW

* Level 1 requires pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level 3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown below.



Burn-in and operating life test circuit



Schematic diagram

Groups C and D Electrical Characteristics Sampling Tests (T_A=25°C)

Characteristic	Symbol	TEST CONDITIONS V^+ = +6 V, V^- = -6 V	Limits		Units
			Min.	Max.	
Input Offset Voltage	V_{IO}		–	5	mV
Input Offset Current	I_{IO}		–	10	μA
Input Bias Current	I_I		–	36	μA
Quiescent Operating Voltage	V_8 or V_{10}		1.5	3.2	V
Device Dissipation	P_T		25	60	mW
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single Ended Output f = 1 kHz	28	–	dB

High-Reliability Video Amplifier

For Applications In Aerospace, Military and Critical Industrial Equipment

Features:

- **Push-Pull Input & Output**
- **AGC Range** . . . . . **60 dB typ.**
- **Bandwidth** . . . . . **29 MHz**
- **Input Resistance** . . . . . **150 kΩ typ.**
- **Output Resistance** . . . . . **45 Ω typ.**
- **Voltage Gain** . . . . . **19 dB typ.**
- **Input Offset Voltage** . . . . . **1.5 mV typ.**

Applications

- **DC, IF, & Video Amplifier**
- **Schmitt Trigger**
- **Mixer**
- **Modulator**
- **See Companion Application Note ICAN-5038 "Applications of the RCA-CA3001 IC Video Amplifier"**

The CA3001 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS *at* $T_A = 25°C$

Indicated voltage or current limits for each terminal can be applied under the specified conditions for other terminals. All Voltages are with respect to ground (common terminal of Positive and Negative DC Supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2, 6 3, 10 9	0 -6 +6
2	-8.5	0	1, 6 3, 10 9	0 -8.5 +6
3	-10	0	1, 2, 6 9 10	0 +6 -6
4	-8.5	0	1, 2, 6 9 10	0 +6 -6
5	-6	0	1, 2, 6 3, 10 9	0 -6 +6
6	-2.5	+2.5	1, 2 3, 10 9	0 -6 +6
7	INTERNAL CONNECTION DO NOT USE			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.8 & No.10	0 -6 +6
9	0	+10	1, 2, 6, 10 3	0 -6
10	-10	0	1, 2, 6 3 9	0 -6 +6
11	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.10 & No.11	0 -6 +6
12	INTERNAL CONNECTION DO NOT USE			
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

CA3001/...

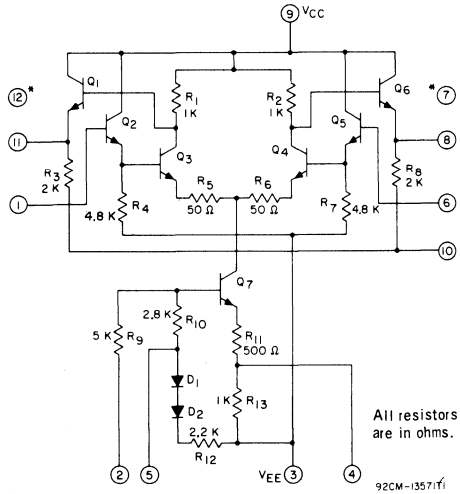
MAXIMUM RATINGS, *Absolute-Maximum Values*

OPERATING-TEMPERATURE RANGE ..... -55° C to +125° C
STORAGE—TEMPERATURE RANGE ..... -65° C to +150° C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE ..... ±2.5 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE ..... ±2.5 V
MAXIMUM DEVICE DISSIPATION ..... 300 mW
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... 265° C

Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits*

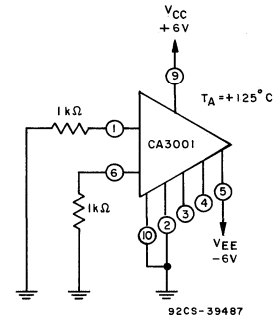
Electrical Characteristics, at T_A = 25°C, V^+ = +6 V, V^- = −6 V						
Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Max.	Max.Δ	
Input Offset Current	I_{IO}	–	–	10	±2	μA
Input-Bias Current	I_I	–	–	36	±4	μA
Output Offset Voltage	V_{OO}	–	–	300	±100	mV
Quiescent Operating Voltage	V_8 or V_{11}	Terminal 4: NC Terminal 5: NC	3.8	4.8	±0.5	V
Device Dissipation	P_T	Terminal 4: NC Terminal 5: NC	60	115	±12	mW

*Level /1 requires pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown below.



* Internal Connection – DO NOT USE

Schematic diagram.



Burn-in and operating life test circuit.

Group A Electrical Sampling Inspection

Characteristics	Symbol	Test Conditions V^+ = +6V, V^- = -6V		Limits for Indicated Temp. (°C)						Units
				Minimum			Maximum			
				-55	+25	+125	-55	+25	+125	
Static										
Input Unbalance Current	I_{IU}	–		–	–	–	23	10	5	μA
Input Bias Current	I_I	–		–	–	–	66	36	22	μA
Output Offset Voltage	V_{oo}	–		–	–	–	420	300	260	mV
Quiescent Operating Voltage	V_8 or V_{11}	Terminal 4	Terminal 5							
		NC	NC	3.8	3.8	3.8	4.8	4.8	4.8	V
Device Dissipation	P_T	Terminal 4	Terminal 5							
		NC	NC	60	60	50	125	115	110	mW
		NC	$-V^-$	55	55	45	120	105	105	mW
		$-V^-$	NC	80	80	70	175	160	155	mW
		$-V^-$	$-V^-$	60	60	50	135	125	125	mW
Common-Mode Rejection Ratio	CMRR	f = 1 kHz		–	70	–	–	–	–	dB
Dynamic										
Differential Voltage Gain (single-ended input and output)	A_{Diff}	f = 1.75 MHz		–	16	–	–	–	–	dB
		f = 20 MHz		–	10	–	–	–	–	dB
Maximum Output Voltage Swing	V_{OUT} (p-p)	f = 1.75 MHz		–	4	–	–	–	–	V_{p-p}
Noise Figure	NF	f = 1.75 MHz, R_S = 1kΩ		–	–	–	–	8	–	dB
AGC Range (max. voltage gain to complete cutoff)	AGC	f = 1.75 MHz		–	55	–	–	–	–	dB

Groups C and D Electrical Characteristics Sampling Tests (T_A = 25° C, V_C = +6 V, V_{EE} = -6 V)

Characteristic	Symbol	Test Conditions	Limits		Units
			Min.	Max.	
Input Bias Current	I_I	–	–	36	μA
Output Offset Voltage	V_{00}	–	–	300	mV
Quiescent Operating Voltage	V_8 or V_{11}	Terminal 4 / 5: NC / NC	3.8	4.8	V
Device Dissipation	P_T	Terminal 4 / 5: NC / NC	60	115	mW
Voltage Gain	A_{Diff}	f = 1.75 MHz	16	–	dB

CA3002/...

High-Reliability IF Amplifier

For Applications in Aerospace, Military and Critical Industrial Equipment

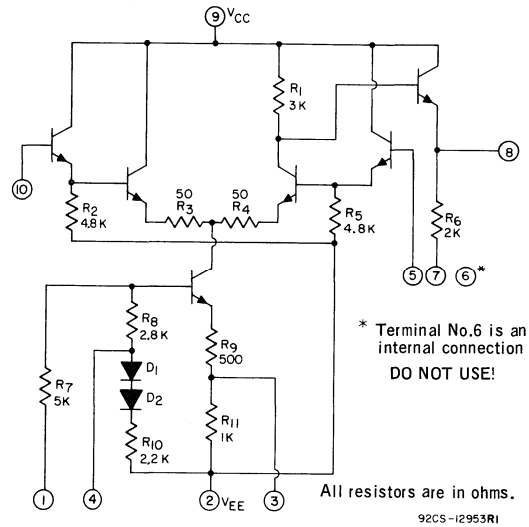
Features:

- **Input Resistance — 100 kΩ typ.**
- **Output Resistance — 70 Ω typ.**
- **Voltage Gain — 24 dB typ. @ 1.75 MHz**
- **Push-Pull Input, Single-Ended Output**
- **-3 dB Bandwidth — 11 MHz typ.**
- **AGC Range — 80 dB typ.**
- **Useful Frequency Range DC to — 15 MHz**

Applications:

- **Product Detector**
- **AM Detector**
- **IF & Video Amplifier**
- **Schmitt Trigger**
- **See Companion Application Note ICAN-5038 "Application of RCA-3002 IC IF Amplifier"**

The CA3002 Slash (/) Series type is supplied in the 10-lead TO-5 style package ("T" suffix), or in chip form ("H" suffix).



Schematic Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values*

OPERATING-TEMPERATURE RANGE	-55° C to +125° C
STORAGE-TEMPERATURE RANGE	-65° C to +150° C
MAXIMUM INPUT-SIGNAL VOLTAGE	±3.5 V
MAXIMUM DEVICE DISSIPATION	300 mW
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	265° C

Absolute-Maximum Voltage and Current Limits, at T_A = 25° C

Indicated voltage or current limits for each terminal can be applied under the specified operating conditions for other terminals.

All voltages are with respect to ground ($-V_{CC}$, $+V_{EE}$) or common terminal of Positive and Negative DC supplies).

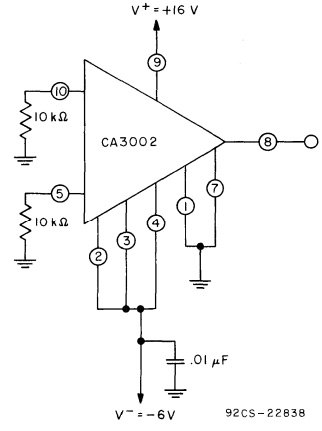
TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-8 V	0 V	2, 7 5, 10 9	-8 0 +6
2	-10 V	0 V	1, 5, 10 9	0 +6
3	-8.5 V	0 V	1, 5, 10 7 9	0 -6 +6
4	-8 V	0 V	1, 5, 10 2, 7 9	0 -8 +6
5	-3.5 V	+3.5 V	1, 10 2, 7 9	0 -6 +6
CASE	INTERNALLY CONNECTED TO TERMINAL No.2 (SUBSTRATE) DO NOT GROUND			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
6	INTERNAL CONNECTION DO NOT USE			
7	-12 V	0 V	1, 5, 10 2 9	0 -6 +6
8	20 mA		1, 5, 7, 10 2 9 200 Ω Resistor Between Terminals 7 & 8	0 -6 +6
9	0 V	+10 V	1, 5, 10 2, 3, 7	0 -6
10	-3.5 V	+3.5 V	1, 5 2, 7 9	0 -6 +6

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT T_A = 25°C, V^+ = +6 V, V^- = -6 V	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Input Bias Current	I_I	V^+ = +6 V, Terminal No. 2 = -6 V, Terminal No. 1 to ground	—	31	±10	μA
Total Drain Current	I_T	$I_2 = I_9 = I_T$	5.0	15.8	±1.5	mA

*Level /1 requires pre and post burn-in electrical tests and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown below.



Burn-in and operating life test circuit.

CA3002/...

Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +6$ V, $V^- = -6$ V	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
Static									
Input Unbalance Current	I_{IU}	$I_{IO} - I_5 = I_{IU}$	–	–	–	35	10	10	μA
Input Bias Current	I_I		–	–	–	85	35	30	μA
Total Drain Current	I_T	$I_2 + I_9 = I_T$	–	–	–	16.7	15.8	15.0	mA
Max Output Voltage	$+V_{OM}$		–	4.6	–	–	5.4	–	V
Min. Output Voltage	$+V_{OM}$	Terminal No. 1 Ground	–	–	–	–	0.05	–	V
Dynamic									
Noise Figure	NF	f = 1.75 MHz, R_S = 1 kΩ	–	–	–	–	8	–	dB
Voltage Gain	A	f = 1.75 MHz, single-ended input and output	–	19	–	–	–	–	dB
AGC Range (Maximum Voltage gain to complete cutoff)	AGC	f = 1.75 MHz	–	60	–	–	–	–	dB

Groups C and D Electrical Characteristics Sampling Tests (T_A = 25° C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +6$ V, $V^- = -6$ V	LIMITS		UNITS
			MIN.	MAX.	
Input Unbalance Current	I_{IU}	$I_{IO} - I_5 = I_{IU}$	–	10	μA
Input Bias Current	I_I		–	35	μA
Total Drain Current	I_T	$I_2 + I_9 = I_T$	5.0	15.8	mA
Voltage Gain	A	f = 1.75 MHz, single-ended input and output	19	–	dB

High-Reliability RF Amplifier

For Applications in Aerospace, Military and Critical Industrial Equipment

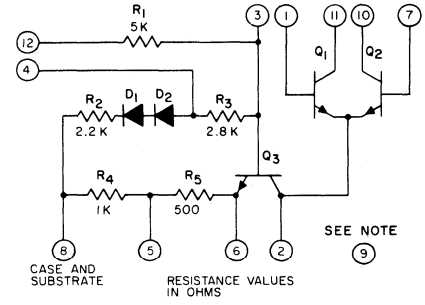
Features:

- **Input offset voltage (V_{IO}) = 1 mV (max.)**
- **AGC range = 60 dB (min.) at 1.75 MHz**
- **Cascode power gain = 20 dB (typ.) at 100 MHz**
- **Operation from dc to 100 MHz**
- **Sharp limiting characteristics**
- **Balanced input and output**
- **Uncommitted bases and collectors**

Applications:

- **Wide and narrow band amplifiers**
- **Detectors**
- **Mixers**
- **Limiters**
- **Modulators**
- **Cascode Amplifiers**

The CA3006 Slash (/) Series types are supplied in the 12-lead TO-5 style package ("T" suffix), and in chip form ("H" suffix).



NOTE: Connect Terminal No.9 to most positive dc supply voltage used for circuit.

Schematic diagram of CA3006.

Maximum Voltage Ratings at T_A = 25°C

This chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 9 with respect to terminal 5 is 0 to +18 volts.

9	10	11	12	1	2	3	4	5	6	7	8	TERMINAL No.
	*	*	+18 0	*	*	+18 0	+18 0	+18 0	+18 0	*	+18 0	9
		*	*	*	+12 0	*	*	*	*	+12 −1	+18 0	10
			*	+12 −1	+12 0	*	*	*	*	*	+18 0	11
				*	*	+18 −18	+18 −18	*	*	*	+18 −5	12
					+1 −4	*	*	*	+10 −4	+4 −4	*	1
						+12 −1	*	*	+10 0	+4 −1	*	2
							*	*	+1 −4	*	+10 −5	3
								*	*	*	+10 −5	4
									*	*	*	5
										+4 −10	*	6
											*	7
											REF. SUBSTRATE	8

Maximum Current Ratings

TERMINAL No.	I_{IN} mA	I_{OUT} mA
9	–	–
10	+20	+0.1
11	+20	+0.1
12	–	–
1	+2	+0.1
2	+20	+20
3	–	–
4	–	–
5	–	–
6	–	–
7	+2	+0.1
8	+0.1	+20

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

CA3006/...

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25°C$*

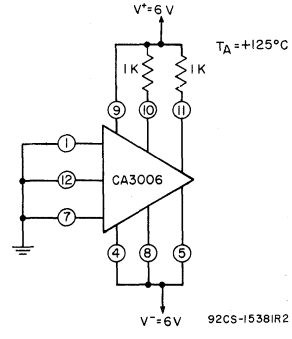
DEVICE DISSIPATION ..... 300 mW
SINGLE-ENDED INPUT-SIGNAL VOLTAGE ..... ±3.5 V
COMMON-MODE INPUT-SIGNAL VOLTAGE ..... -2.5 to +3.5 V
AMBIENT TEMPERATURE RANGE:
  OPERATING ..... -55 to +125°C
  STORAGE ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... 265°C

Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits*

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$, $V^+ = 6$ V, $V^- = 6$ V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Max.	Max.Δ	
Input-Bias Current	I_{IB}	–	–	40	±4	μA
Quiescent Operating Current	I_{10} or I_{11}	Terminal 4: NC Terminal 5: NC	0.6	1.6	±0.2	mA
Device Dissipation	P_D	Terminal 4: NC Terminal 5: NC	16	45	±5.4	mW

*Level /1 requires pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown below.



Burn-in and operating life test circuit.

Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = 6$ V, $V^- = 6$ V		Limits for Indicated Temp. (°C)						UNITS
				Minimum			Maximum			
				–55	+25	+125	–55	+25	+125	
STATIC										
Input Offset Voltage	V_{IO}	–		–	–	–	2	1	1.5	mV
Input Offset Current	I_{IO}	–		–	–	–	4	2	1	μA
Input Bias Current	I_{IB}	–		–	–	–	60	40	30	μA
Quiescent Operating Current	I_{10} I_{11}	Terminal 4	Terminal 5							
		NC	NC	0.6	0.6	0.5	1.7	1.6	1.4	mA
		NC	V^-	1.6	1.6	1.4	4.5	4.4	4	mA
		V^-	NC	0.25	0.25	0.25	0.85	0.75	0.85	mA
		V^-	V^-	0.7	0.8	0.75	2.3	2.4	2.2	mA
Device Dissipation	P_D	Terminal 4	Terminal 5							
		NC	NC	16	16	14	50	45	45	mW
		NC	V^-	45	45	40	125	120	110	mW
		V^-	NC	10	10	9	30	30	30	mW
		V^-	V^-	20	25	20	70	70	70	mW
DYNAMIC										
Power Gain	G_p	f = 100 MHz	Cascode Configuration	–	16	–	–	–	–	dB
			Differential Amplifier * Configuration	–	14	–	–	–	–	dB
Noise Figure	NF	f = 100 MHz	Cascode Configuration	–	–	–	–	9	–	dB
			Differential Amplifier * Configuration	–	–	–	–	9	–	dB
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 MHz		–	–60	–	–	–	–	dB

* Not tested but guaranteed.

Groups C and D Electrical Characteristics Sampling Tests (TA = 25° C, V+ = 6 V, V- = 6 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Max.	Max.Δ	
Input Bias Current	I_{IB}	–	–	40	±4	μA
Quiescent Operating Current	I_{10} or I_{11}	Terminal 4 | 5 / NC | NC	0.6	1.6	±0.2	mA
Device Dissipation	P_D	Terminal 4 | 5 / NC | NC	16	45	±5.4	mW
Power Gain (Differential)	G_P	f = 100 MHz	14	–	±2	dB

CA3015A/...

High-Reliability Operational Amplifier

For Applications In Aerospace, Military and Critical Industrial Equipment

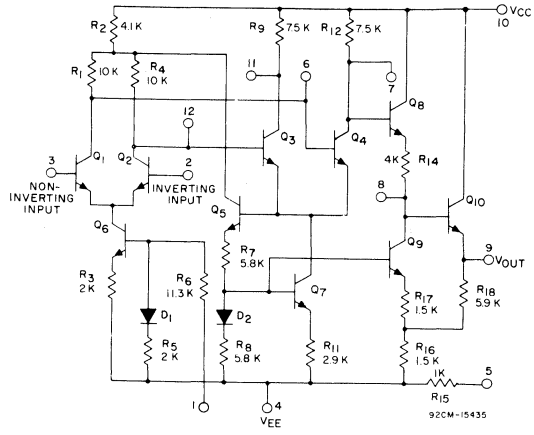
Features:

- **Open-loop voltage gain** . . . . . **70 dB typ.**
- **Common-mode rejection ratio** . . . . . **103 dB typ.**
- **Input impedance** . . . . . **10 kΩ typ.**
- **Input offset voltage** . . . . . **1 mV typ.**
- **Input offset current** . . . . . **0.5 μA typ.**
- **Input bias current** . . . . . **4.7 μA typ.**
- **Static power drain at ± 12 V** . . . . . **175 mW typ.**

Applications:

- **Narrow-band and band-pass amplifier**
- **Operational functions**
- **Feedback amplifier**
- **DC and video amplifier**
- **Multivibrator**
- **Oscillator**
- **Comparator**
- **Servo driver**
- **Scaling adder**
- **Balanced modulator-driver**

The CA3015A Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).



Schematic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

OPERATING-TEMPERATURE RANGE . . . . . -55° C to +125° C
STORAGE-TEMPERATURE RANGE . . . . . -65° C to +150° C
MAXIMUM INPUT-SIGNAL VOLTAGE . . . . . -8 V, +1 V
MAXIMUM DEVICE DISSIPATION:
AT AMBIENT TEMPERATURES
UP TO 70° C . . . . . 700 mW
ABOVE 70° C . . . . . Derate at 6.7 mW/° C
AT CASE TEMPERATURES
UP TO 125° C . . . . . 830 mW
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 mm ± 0.79 mm) from case for 10 s max. . . . . 265° C

Maximum Voltage Ratings at T_A = 25° C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 12 with respect to terminal 10 is 0 to -15 volts.

TERMINAL No.	12	1	2	3	4▲	5	6	7	8	9	10	11
12		*	+15 -1	*	*	*	+5 -5	*	*	*	0 -15	+1 -15
1			*	*	+20 -5	*	*	*	*	*	*	*
2				+5 -5	+18 -5 Note 2	*	*	*	*	*	*	*
3					+18 -5 Note 2	*	+1 -15	*	*	*	*	*
4▲						0 -30 Note 3	*	*	0 -30	0 -30	0 -32	*
5							*	*	*	*	0 -30	*
6								+1 -15	*	*	0 -20	*
7									+20 -5	*	0 -20	*
8										+1 -5	0 -30	*
9											0 -32	*
10												+20 0
11												

Maximum Current Ratings

TERMINAL No.	I_{IN} mA	I_{OUT} mA
12	1	1
1	–	–
2	1	0.1
3	1	0.1
4▲	–	–
5	–	–
6	1	1
7	3	3
8	3	3
9	30	30
10	–	–
11	3	3

▲ CA3015A Case is internally connected to the substrate (Terminal Lead #4), DO NOT GROUND.

Note 1: For normal circuit operation, external voltages should not be applied to terminals 5,6,8, and 12.

Note 2: This rating applies only to the more positive terminal of terminals 2 or 3.

Note 3: Carefully observe maximum dissipation ratings.

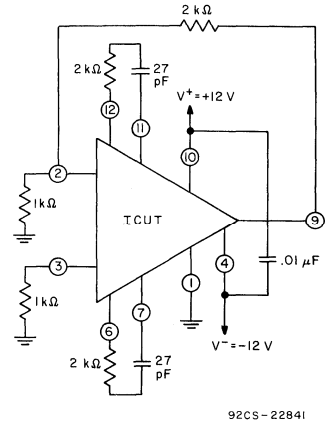
* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Pre Burn-In and Post Burn-In Electrical Tests, and Delta Limits*

ELECTRICAL CHARACTERISTICS, at T_A = V^+ = +12V, V^- = -12V						
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Max.	Max.Δ	
Input Offset Voltage	V_{IO}		–	2	±1	mV
Input Offset Current	I_{IO}		–	1.6	±1	μA
Input Bias Current	I_I		–	6	±1	μA
Device Dissipation	P_T		110	240	±25	mW
		5 shorted to 9	320	600	±50	

*Level /1 requires pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown on the next page.

CA3015A/...



Burn-in and operating life test circuit.

Group A Electrical Sampling Inspection

Characteristics	Symbol	Test Conditions V^+ = +12 V, V^- = -12 V	Limits for Indicated Temperature (°C)						Units
			Minimum			Maximum			
			-55	+25	+125	-55	+25	+125	
STATIC									
Input Offset Voltage	V_{IO}	–	–	–	–	3	2	3	mV
Input Offset Current	I_{IO}	–	–	–	–	3	1.6	2	μA
Input Bias Current	I_I	–	–	–	–	14	6	8	μA
Input Offset Voltage Sensitivity Positive	$\frac{\Delta V_{IO}}{\Delta V^+}$	–	–	–	–	–	0.5	–	mV/V
Negative	$\frac{\Delta V_{IO}}{\Delta V^-}$	–	–	–	–	–	0.5	–	mV/V
Device Dissipation	P_T	–	115	110	95	280	240	235	mW
		5 shorted to 9	330	320	–	700	600	–	mW
DYNAMIC All tests are at 1 kHz except BW_{OL}									
Open-Loop Differential Voltage Gain	A_{OL}	–	–	66	–	–	–	–	dB
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	–	–	200	–	–	–	–	kHz
Common-Mode Rejection Ratio	CMR	–	–	80	–	–	–	–	dB
Maximum Output-Voltage Swing	$V_{O(P-P)}$	–	–	12	–	–	–	–	V_{P-P}
Output Impedance	Z_{OUT}	–	–	–	–	–	120	–	Ω
Common-Mode Input-Voltage Range	V_{CMR}	–	–	+0.35 to -8	–	–	–	–	V
Noise Figure	NF	R_S = 1 k	–	–	–	–	16	–	dB

Groups C and D Electrical Sampling Tests

T_A = +25°C V^+ = +12 V V^- = -12V

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	END POINT LIMITS		UNITS
			MIN.	MAX.	
Input Offset Voltage	V_{IO}	–	–	2	mV
Input Offset Current	I_{IO}	–	–	1.6	μA
Input Bias Current	I_I	–	–	6	μA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	–	–	0.5	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$	–	–	0.5	mV/V
Device Dissipation	P_T	–	110	240	mW
		Terminal 5 shorted to 9	320	600	mW
Open-Loop Differential Voltage Gain	A_{OL}	f = 1 kHz	66	–	dB
Common-Mode Rejection Ratio	CMR	f = 1 kHz	80	–	dB

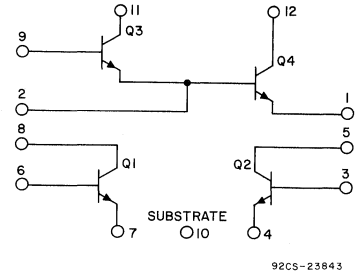
CA3018A/...

High-Reliability General-Purpose Transistor Array

For Applications in Aerospace, Military and Critical Industrial Equipment

Features:

- **Matched monolithic general-purpose transistors**
- **H_{FE} matched ± 10%**
- **V_{BE} matched ± 2 mV**
- **Operation from DC to 120 MHz**
- **Wide operating current range**
- **CA3018A performance characteristics controlled from 10 μA to 10 mA**
- **Low noise figure —— 3.2 dB typical at 1 kHz**



Schematic diagram of CA3018A.

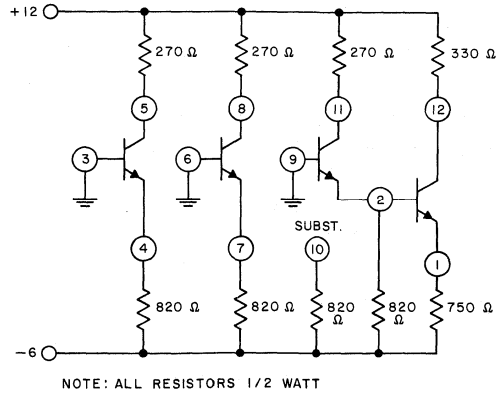
MAXIMUM RATINGS, *Absolute Maximum Values at $T_A = 25°C$*

DEVICE DISSIPATION:		
Any one transistor	300	mW
Total package	450	mW
$T_A > 85°C$	derate linearly at 5	mW/°C
AMBIENT TEMPERATURE RANGE:		
OPERATING	−55 to +125	°C
Storage	−65 to +150	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	30	V
Collector-to-Substrate Voltage, V_{CIO}*	40	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 265	°C

* *The collector of each transistor of the CA3018A/ is isolated from the substrate by an integral diode. The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*



Burn-in and operating life-test circuit.

PRE BURN-IN ELECTRICAL AND POST BURN-IN ELECTRICAL TESTS, AND DELTA LIMITS*
ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Max.	Max.Δ	
Emitter-to-Base Breakdown Volts, Q_1, Q_2	$V_{(BR)EBO}$	$I_E = 10\ \mu A$, $I_C = 0$	5	–	±0.5	V
Collector Cutoff Current, Q_1, Q_2	I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	–	0.5	±0.15	μA
Collector Cutoff Current, Q_3, Q_4	$I_{CEO(D)}$	$V_{CE} = 10$ V, $I_B = 0$	–	5	±1	μA
Input Current Q_1, Q_2	I_{IN}	$I_C = 1$ mA, $V_{CE} = 3$ V	–	16.7	±2	μA
Input Current Darlington Pair, Q_3, Q_4	$I_{IN(D)}$	$I_C = 1$ mA, $V_{CE} = 3$ V	–	0.5	±0.1	μA
Base-to-Emitter Voltage, Q_1, Q_2	V_{BE}	$I_E = 1$ mA, $V_{CE} = 3$ V	0.6	0.8	±0.1	V
Base-to-Emitter Voltage, Darlington Pair, Q_3, Q_4	$V_{BE(D)}$ ($V_{9\text{-}1}$)	$I_E = 1$ mA, $V_{CE} = 3$ V	1.1	1.5	±0.1	V

*Level /1 requires pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown above.

CA3018A/...

GROUP A ELECTRICAL SAMPLING INSPECTION

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMP.(°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
STATIC									
Collector Cutoff Current, Q_1, Q_2, Q_3, Q_4	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	–	40	–	nA
Collector-to-Base Breakdown Voltage, Q_1, Q_2, Q_3, Q_4	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	30	–	–	–	–	V
Emitter-to-Base Breakdown Voltage, Q_1, Q_2, Q_3, Q_4	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	–	–	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{C1} = 0	–	40	–	–	–	–	V
Collector-to-Emitter Breakdown Voltage, Q_1, Q_2, Q_3, Q_4	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	–	–	–	–	V
Collector Cutoff Current, Q_1, Q_2	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	–	–	–	0.5	100	μA
Collector Cutoff Current, Q_3, Q_4	$I_{CEO(D)}$	V_{CE} = 10 V, I_B = 0	–	–	–	–	5	2000	μA
Static Forward Current Transfer Ratio, Q_1, Q_2	h_{FE}	I_C = 1 mA, V_{CE} = 3 V	29	60	70	–	–	–	–
Static Forward Current Transistor Ratio, Darlington Pair	$h_{FE(D)}$	I_C = 1 mA, V_{CE} = 3 V	1000	2000	2300	–	–	–	–
Base-to-Emitter Voltage Voltage, Q_1, Q_2	V_{BE}	I_E = 1 mA, V_{CE} = 3 V	0.7	0.6	0.4		0.8	0.7	V
Static Forward Current Transfer Ratio, Q_1, Q_2	h_{FE}	I_C = 10 mA, V_{CE} = 3 V I_C = 10 μA, V_{CE} = 3 V	– –	50 30	– –	– –	– –	– –	– –
Static Forward Current Transfer Ratio, Darlington Pair	$h_{FE(D)}$	I_C = 100 μA, V_{CE} = 3 V	–	1000	–	–	–	–	–
Base-to-Emitter Voltage, Q_1, Q_2	V_{BE}	I_E = 10 mA, V_{CE} = 3 V	–	–	–	–	0.9	–	V
Input Offset Voltage	$\lvert V_{BE_1} - V_{BE_2} \rvert$	I_E = 1 mA, V_{CE} = 3 V	–	–	–	–	2	–	mV
Base-to-Emitter Voltage, Darlington Pair	$V_{BE(D)}$ $[V_{9-1}]$	I_E = 10 mA, V_{CE} = 3 V I_E = 1 mA, V_{CE} = 3 V	– –	– 1.1	– –	– –	1.6 1.5	– –	V V
Magnitude of Static Beta Ratio, Q_1, Q_2		I_{C1} = I_{C2} = 1 mA V_{CE} = 3 V	–	0.9	–	–	1.11	–	–
Collector-to-Emitter Saturation Voltage, Q_1, Q_2	V_{CES}	I_B = 1 mA, I_C = 10 mA	–	–	–	–	0.5	–	V
Static Forward Current Ratio, Darlington Pair	$h_{FE(D)}$	I_C = 10 mA, V_{CE} = 3 V	–	3000	–	–	–	–	–
DYNAMIC									
Gain Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA f = 100 MHz	–	300	–	–	–	–	MHz

GROUPS C AND D ELECTRICAL CHARACTERISTICS SAMPLING TESTS (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			Min.	Max.	
Emitter-to-Base Breakdown Volts, Q_1, Q_2, Q_3, Q_4	$V_{(BR)EBO}$	I_E = 10 mA, I_C = 0	5	–	V
Collector-to-Emitter Breakdown Volts, Q_1, Q_2, Q_3, Q_4	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	–	V
Collector Cutoff Current, Q_1, Q_2	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	0.5	μA
Collector Cutoff Current, Q_3, Q_4	$I_{CEO(D)}$	V_{CE}= 10 V, I_B = 0	–	5	μA
Input Current, Q_1, Q_2	I_{IN}	I_C = 1 mA, V_{CE} = 3 V	–	25	μA
Input Current, Darlington Pair, Q_3, Q_4	$I_{IN(D)}$	I_C = 1 mA, V_{CE} = 3 V	–	1	μA
Base-to-Emitter Voltage, Q_1, Q_2	V_{BE}	I_E = 1 mA, V_{CE} = 3 V	0.6	0.8	V
Base-to-Emitter Voltage, Darlington Pair, Q_3, Q_4	$V_{BE(D)}$	I_E = 1 mA, V_{CE} = 3 V	1.1	1.5	V

CA3019/...

High-Reliability Diode Array Diode Quad and Two Individual Diodes

For Applications In Aerospace, Military and Critical Industrial Equipment

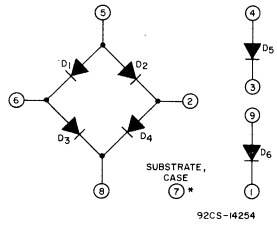
Features:

- **Excellent diode match**
- **Low leakage current**
- **Low pedestal voltage when gating**

Applications:

- **Modulator**
- **Mixer**
- **Balanced modulator**
- **Analog switch**
- **Diode gate for chopper-modulator applications**
- **See companion application note ICAN-5291 application of the RCA CA3019 IC Diode Array**

The CA3019 Slash (/) Series type is supplied in the 10-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).



* Connect to most negative circuit potential.

Schematic diagram.

Absolute-Maximum Voltage Limits at T_A = 25° C

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-3	+12	7	-6
2	-3	+12	7	-6
3	-3	+12	7	-6
4	-3	+12	7	-6
5	-3	+12	7	-6
6	-3	+12	7	-6
7	-18	0	1, 2, 3, 6, 8	0
8	-3	+12	7	-6
9	-3	+12	7	-6
10	NO CONNECTION			
CASE	INTERNALLY CONNECTED TO TERMINAL 7 **DO NOT GROUND**			

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:
- Any one diode unit ..... 20 max. mW
- Total for device ..... 120 max. mW

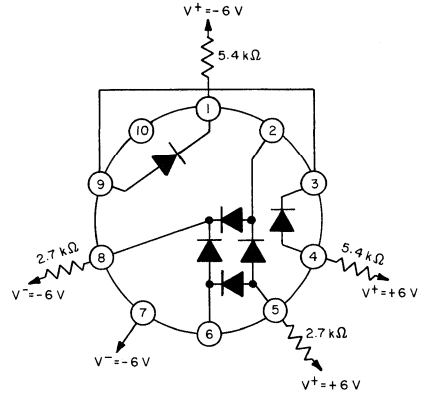
TEMPERATURE RANGE:
- Storage ..... -65 to +150° C
- Operating ..... -55 to +125° C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max. ..... 265° C

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Each Diode: DC Forward Voltage Drop	V_F	I_F = 1 mA	–	0.78	±0.010	V
		I_F = 0.2 mA	–	0.72	±0.010	V
		I_F = 20 mA	–	0.95	±0.010	V

*Level /1 requires pre and post burn-in electrical tests and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown below.



92CS-22934

Burn-In and operating life test circuit

Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
Each Diode:									
DC Forward Voltage Drop	V_F	I_F = 0.2 mA	–	–	–	–	0.72	–	V
		I_F = 1 mA	0.76	–	0.41	0.97	0.78	0.60	V
		I_F = 20 mA	–	–	–	–	0.95	–	V
DC Reverse Leakage Current	I_R	V_R = –4 V	–	–	–	–	10	–	μA
DC Reverse Leakage Current To Substrate	I_R	V_R = –4 V	–	–	–	–	10	–	μA
Between Any Two Diodes: Diode Offset Voltage	$\lvert V_{F1} - V_{F2} \rvert$	I_F = 1 mA	–	–	–	–	5	–	mV
Isolation-to-Substrate Breakdown Voltage		–50 V through a 25 KΩ to terminal 7. Ground terminal 1 through 6, 8 and 9. Measure voltage at terminal 7	–	50	–	–25	–25	–25	V

CA3019/...

Groups C and D Electrical Characteristics Sampling Tests (T_A = 25° C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT T_A = 25°C, V^+ = +6 V, V^- = −6 V	LIMITS MIN	LIMITS MAX	UNITS
Each Diode:					
DC Forward Voltage Drop	V_F	I_F = 0.2 mA	0.39	0.73	V
		I_F = 1 mA	0.49	0.79	V
		I_F = 20 mA	0.59	0.96	V
DC Reverse Leakage Current	I_R	V_R −4 V	–	10	μA
DC Reverse Leakage Current To Substrate	I_R	V_R = −4 V	–	10	μA
Between Any Two Diodes: Diode Offset Voltage	$V_{F1} - V_{F2}$	I_F = 1 mA	–	5	mV
Isolation-to-Substrate Breakdown Voltage		−50 V through a 25 KΩ to terminal 7 Ground terminal 1 through 6, 8 and 9. Measure voltage at terminal 7	−25	−25	V

High-Reliability Multipurpose Wide-Band Power Amplifier

For Applications in Aerospace, Military and Critical Industrial Equipment

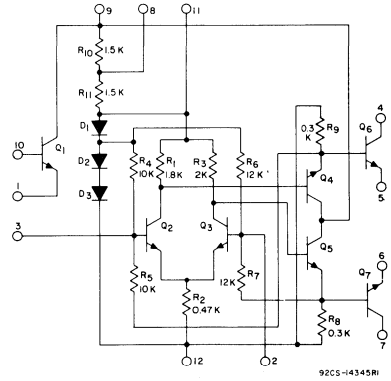
Features:

- High power output – class B amplifier. . . 1.0 W typ. at V^+ = +12 V
- Wide frequency range. . . Up to 8 MHz with resistive loads
- High power gain. . .75 dB typ.
- Single power supply for class B operation with transformer. . . 3 to 12 V
- Built-in temperature-tracking voltage regulator provides stable operation over –55°C to +125°C temperature range

The CA3020A Slash (/) Series types are supplied in the 12-lead TO-5 style package ("T" suffix), and in chip form ("H" suffix).

Applications:

- AF power amplifiers for portable and fixed sound and communications systems
- Servo-control amplifiers
- Wide-band linear mixers
- Video power amplifiers
- Transmission-line driver amplifiers (balanced and unbalanced)
- Fan-in and fan-out amplifiers for computer logic circuits
- Lamp-control amplifiers
- Motor-control amplifiers
- Power multivibrators
- Power switches
- Companion Application Note, ICAN-5766, "Application of CA3020 and CA3020A Integrated Circuit Multipurpose Wide-Band Power Amplifiers"



Schematic diagram.

CA3020A/...

MAXIMUM RATINGS, *Absolute Maximum Values at $T_A = 25^oC$:*

	Without Heat Sink	With Heat Sink
DEVICE DISSIPATION:		
At $T_A = 25^oC$	1 W	
Above $T_A = 25^oC$	derate linearly 6.7 mW/^{o}C	
At $T_C = 25^oC$		2 W
At $T_C = 25^oC$ to $T_C = 55^oC$		2 W
Above $T_C = 55^oC$		derate linearly 16.7 mW/^{o}C
AMBIENT TEMPERATURE RANGE:		
Operating		−55^{o}C to +125^{o}C
Storage		−65^{o}C to +150^{o}C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.		265 ^{o}C

Maximum Voltage Ratings at $T_A = 25^oC$

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 12 is 0 to +10 volts.

Terminal No.	1	2	3	4	5	6	7	8	9	10	11	12
1		*	*	*	*	*	*	*	0 −12	+3 Note 1		+10 0
2			*	*	*	*	*	*	*	*	*	+2 −2
3				*	*	*	*	*	*	*	*	+2 −2
4					+25 0	*	*	*	*	*	*	+25 0
5						*	*	*	*	*	*	+3 Note 2
6							0 −25	*	*	*	*	+3 Note 2
7								*	*	*	*	+25 0
8									Note 3	*	*	Note 3 0
9										+10 0	Note 1 0	+12 0
10											*	+10 0
11												*
12												Ref. Sub- Strate

Maximum Current Ratings

Terminal No.	I_{In} mA	I_{Out} mA
1	—	20
2	—	—
3	—	—
4	300	—
5	—	300
6	—	300
7	300	—
8	—	—
9	20	—
10	1	—
11	20	—
12	—	—

Note 1: This voltage is established by the maximum current rating.

Note 2: The emitters of Q_6 and Q_7 may be returned to a negative voltage supply through emitter resistors. Current into terminal No.9 should not be exceeded and the total device dissipation should not be exceeded.

Note 3: Terminal No.8 may be connected to terminals Nos.9, 11, or 12.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

PRE BURN-IN ELECTRICAL AND POST BURN-IN ELECTRICAL TESTS, AND DELTA LIMITS*

Electrical Characteristics at T_A = 25°C							
CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS			UNITS
		V^+_1▲	V^+_2▲	Min.	Max.	Max.Δ	
Peak Output Currents, Q_6 & Q_7	I_4PK, I_7PK	9 V	2 V	180	–	±15	mA
Cutoff Currents, Q_6 & Q_7	I_4 Cutoff I_7 Cutoff	9 V	2 V	–	1	±0.1	mA
Differential Amplifier Current Drain	I^+_1	9 V	9 V	6.3	12.5	±1.3	mA
Total Current Drain	$I^+_1 + I^+_2$	9 V	9 V	14	30	±3	mA

*Level /1 requires pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown on the next page.

▲ V^+_1 is the collector voltage applied to Q_1 through Q_5
V^+_2 is the collector voltage applied to Q_6 and Q_7

GROUP A ELECTRICAL SAMPLING INSPECTION

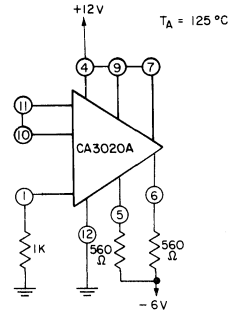
CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS FOR INDICATED TEMP.(°C)						UNITS
		DC SUPPLY VOLTAGE		MINIMUM			MAXIMUM			
		V^+_1▲	V^+_2▲	–55	+25	+125	–55	+25	+125	
STATIC										
Collector-to-Emitter Breakdown Voltage, Q_6 & Q_7 at 10 mA	$V_{(BR)CER}$	–	–	–	25	–	–	–	–	V
	$V_{(BR)CEO}$	–	–	–	21	–	–	–	–	
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1 mA	$V_{(BR)CEO}$	–	–	–	10	–	–	–	–	V
Peak Output Currents, Q_6 & Q_7	I_4PK I_7PK	9 V	2 V	–	180	–	–	–	–	mA
Cutoff Currents, Q_6 & Q_7	I_4Cutoff I_7Cutoff	9 V	2 V	–	–	–	–	1	–	mA
Differential Amplifier Current Drain	I^+_1	9 V	9 V	5.5	6.3	3.5	16.5	12.5	10	mA
Total Current Drain	$I^+_1 + I^+_2$	9 V	9 V	6	14	8	51	30	25	mA
Q_1 Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	10 V	–	–	–	–	–	100	–	μA
Emitter-to-Base	I_{EBO}	3 V	–	–	–	–	–	0.1	–	μA
Collector-to-Base	I_{CBO}	3 V	–	–	–	–	–	0.1	–	μA
Forward Current Transfer Ratio, Q_1 at 3 mA	h_{FE1}	6 V	–	–	30	–	–	–	–	
DYNAMIC										
Maximum Power Output, R_{CC} = 200 Ω	$P_{O(Max.)}$	9 V	12 V	–	800	–	–	–	–	mW
Sensitivity for P_{OUT} = 800 mW	e_{In}	9 V	12 V	–	–	–	–	100	–	mV

CA3020A/...

GROUPS C AND D ELECTRICAL CHARACTERISTICS SAMPLING TESTS at T_A = 25° C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS		UNITS
		V^+_1▲	V^+_2▲	MIN.	MAX.	
Peak Output Currents, Q_6 & Q_7	I_4PK I_7PK	9 V	2 V	180	–	mA
Cutoff Currents, Q_6 & Q_7	$I_4Cutoff$ $I_7Cutoff$	9 V	2 V	–	1	mA
Differential Amplifier Current Drain	I^+_1	9 V	9 V	6.3	12.5	mA
Total Current Drain	$I^+_1 + I^+_2$	9 V	9 V	14	30	mA
Sensitivity for P_{OUT} = 800 mW	e_{IN}	9 V	12 V	–	100	mV

▲ V^+_1 is the collector voltage applied to Q_1 through Q_5
V^+_2 is the collector voltage applied to Q_6 and Q_7



Burn-in and operating life test circuit.

High-Reliability
Transistor Array
Dual Independent Differential Amplifier

For Applications In Aerospace, Military and Critical Industrial Equipment

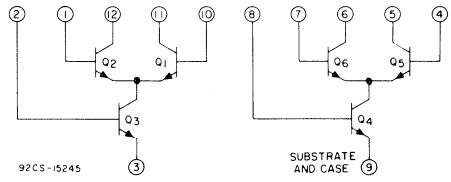
Features:

- **Two differential amplifiers on a common substrate**
- **Independently accessible inputs and outputs**
- **Maximum input offset voltage ± ±5 mV**
- **Full military temperature range capability — -55°C to +125°C**

The CA3026 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Applications:

- **Dual sense amplifiers**
- **Dual Schmitt triggers**
- **Multifunction combinations — RF/Mixer/Oscillator; Converter/IF**
- **IF amplifiers (differential and/or cascode)**
- **Product detectors**
- **Doubly balanced modulators and demodulators**
- **Balanced quadrature detectors**
- **Cascade limiters**
- **Synchronous detectors**
- **Pairs of balanced mixers**
- **Synthesizer mixers**
- **Balanced (push-pull) cascode amplifiers**



Schematic Diagram

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

MAXIMUM RATINGS, *Absolute-Maximum Values, at T_A = 25°C*

POWER DISSIPATION,		
Any one transistor	300	mW
Total package	600	mW
For T_A > 55°C	Derate at 5	mW/°C
TEMPERATURE RANGE:		
Operating	−55 to +125	°C
Storage	−65 to +200	°C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 s max.	265	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3026 is isolated from the substrate by an integral diode. *The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.*

CA3026/...

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 1 and horizontal terminal 3 is +15 to −5 volts.

CA3026→ TERMINAL No. ↓	10	11	12	1	2	3	4	5	6	7	8	Note 1 9
10		0 -20	*	+5 -5	*	+15 -5	*	*	*	*	*	*
11			*	*	*	+20 0	*	*	*	*	*	+20 0
12				+20 0	*	+20 0	*	*	*	*	*	+20 0
1					*	+15 -5	*	*	*	*	*	*
2						+1 -5	*	*	*	*	*	*
3							*	*	*	*	*	*
4								0 -20	*	+5 -5	*	+15 -5
5									*	*	*	+20 0
6										+20 0	*	+20 0
7											*	+15 -5
8												+1 -5
9												*
9												Ref Sub-strate

Maximum Current Ratings

CA3026 TERMINAL No.	I_{IN} mA	I_{OUT} mA
10	5	0.1
11	50	0.1
12	50	0.1
1	5	0.1
2	5	0.1
3	0.1	-50
4	5	0.1
5	50	0.1
6	50	0.1
7	5	0.1
8	5	0.1
9	0.1	50

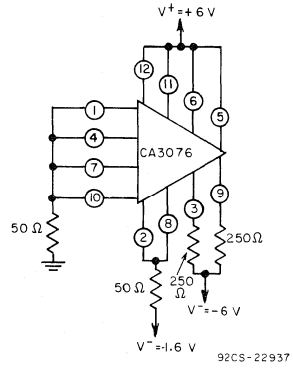
*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Note 1: In the CA3026 terminal No. 9 is connected to the emitter of Q4, the reference substrate, and the case; therefore, should not be grounded.

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Input Bias Current For Each Transistor Q1, Q2, Q5, and Q6	I_I	V_{CE} = 3V, I_E = 2mA	–	24	±6.0	μA
Base-to-Emitter Voltage For Each Transistor Q3 and Q4	V_{BE}	V_{CE} = 3V, I_E = 1mA	0.7	0.8	±0.1	V
Input Offset Voltage For Each Differential Amplifier	V_{IO}	V_{CE} = 3V, I_E = 2mA	–	5	±2	mV

*Level /1 requires pre and post burn-in electrical tests and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown on the next page.



Burn-in and operating life test circuit.

Group A Electrical Sampling Inspection Tests and Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
For Each Transistor:									
Collector Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	0.1	0.1	20	μA
Collector To-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10μA, I_E = 0	–	20	–	–	–	–	V
Emitter-To-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0	–	5	–	–	–	–	V
Collector-To-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10μA, I_{C1} = 0	–	20	–	–	–	–	V
Collector-To-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	–	–	–	–	V
Input Bias Current For Transistors Q3 and Q4	I_I	V_{CE} = 3 V, I_E = 2mA	–	–	–	100	50	40	μA
Input Bias Current For Transistors Q1, Q2, Q5, and Q6	I_I	V_{CE} = 3 V, I_E = 2mA	–	–	–	100	50	40	μA
Base-To-Emitter Voltage For Transistors Q3 and Q4	V_{BE}	V_{CE} = 3 V, I_E = 1mA	0.7	0.7	0.4	1.05	0.8	0.75	V
For Each Differential Amplifier									
Input Offset Current	I_{IO}	V_{CE} = 3 V, I_E = 2mA	–	–	–	–	2	–	μA
Input Offset Voltage	V_{IO}	V_{CE} = 3 V, I_E = 2mA	–	–	–	–	5	–	mV

Groups C and D Electrical Characteristics Sampling Tests (T_A = 25° C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
For Each Transistor: Collector Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	0.2	μA
Input Bias Current For Transistors Q1, Q2, Q5, & Q6	I_I	V_{CE} = 3 V, I_E = 2mA	–	28	μA
Base-to-Emitter Voltage For Transistors Q3 and Q4	V_{BE}	V_{CE} = 3 V, I_E = 1mA	0.65	0.85	V
For Each Differential Amplifier: Input Offset Voltage	V_{IO}	V_{CE} = 3 V, I_E = 2mA	–	6	mV

CA3028B/...

High-Reliability Differential/Cascode Amplifier

For Applications In Aerospace, Military and Critical Industrial Equipment

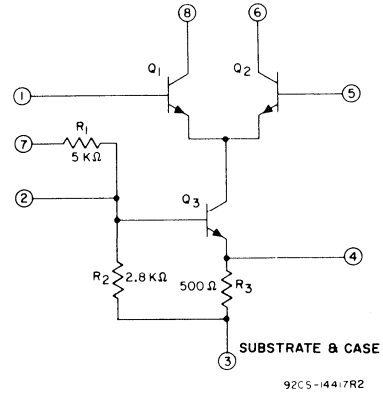
Features:

- **Controlled for input offset voltage, input offset current, and input bias current**
- **Balanced differential amplifier configuration with controlled constant-current source to provide unexcelled versatility**
- **Single- and dual-ended operation**
- **Operation from DC to 120 MHz**
- **Balanced-AGC capability**
- **Wide operating-current range**

Applications:

- **RF and IF amplifiers (differential or cascode)**
- **DC, audio, and sense amplifiers**
- **Converter in the Commerical FM Band**
- **Oscillator ■ Mixer ■ Limiter**
- **See Application Note, ICAN 5337 "Application of the RCA CA3028 integrated circuit amplifier in the HF and VHF ranges."**

The CA3028B Slash (/) Series type is supplied in the 8-lead TO-5 style package ("T" suffix), in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix), or in chip form ("H" suffix).



Schematic diagram.

ABSOLUTE-MAXIMUM RATINGS at T_A = 25° C:

DISSIPATION:
- At T_A up to 85° C ..... 450 mW
- At T_A > 85° C derate linearly ..... 5 mW/° C

AMBIENT TEMPERATURE RANGE:
- Operating ..... -55 to +125° C
- Storage ..... -65 to +150° C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max. ..... 265° C

CA3028B/...

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL No.	1	2	3	4	5	6	7	8
1		0 to -15	0 to -15	0 to -15	+5 to -5	*	*	+20 to 0
2			+5 to -11	+5 to -1	+15 to 0	*	+15 to 0	*
3‡				+10 to 0	+15 to 0	+30● to 0	+15 to 0	+30● to 0
4					+15 to 0	*	*	*
5						+20 to 0	*	*
6							*	*
7								*
8								

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is -1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

● Limit is +24V

MAXIMUM CURRENT RATINGS

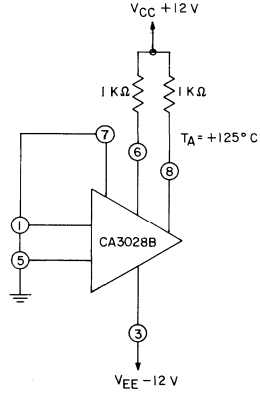
TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

PRE BURN-IN ELECTRICAL AND POST BURN-IN ELECTRICAL TESTS, AND DELTA LIMITS*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Max.	Max.△	
Input Bias Current	I_1		-	80	± 8	μA
Input Offset Voltage	V_{10}		-	5	± 2	mV
Quiescent Oper. Current	I_6 or I_8		2.5	4	± 0.4	mA
Input Current (term. 7)	I_7		1.0	2.1	± 0.2	mA
Device Dissipation	P_T		120	220	± 24	mW

*Level /1 requires pre burn-in electrical and post burn-in electrical tests, and delta limits.

Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown below.



92CS-15831

Burn-in and operating life test circuit.

CA3028B/...

GROUP A ELECTRICAL SAMPLING INSPECTION

Characteristics	Symbol	Test Conditions		Limits for Indicated Temp. (°C)						Units
				Minimum			Maximum			
		V_{CC}	V_{EE}	-55	+25	+125	-55	+25	+125	
Static										
Input Offset Voltage	V_{IO}	+6	-6	—	—	—	7	5	7.5	mV
		+12	-12	—	—	—	5	5	6	
Input Offset Current	I_{IO}	+6	-6	—	—	—	10	5	7.5	μA
		+12	-12	—	—	—	12	6	9	
Input Bias Current	I_I	+6	-6	—	—	—	70	40	35	μA
		+12	-12	—	—	—	130	80	55	
Quiescent Oper. Current	I_6 or I_8	+6	-6	0.5	1.0	0.5	2.0	1.5	2.0	mA
		+12	-12	2.0	2.5	1.5	4.5	4.0	4.0	
Input Current (terminal 7)	I_7	+6	-6	0.5	0.5	0.35	1.5	1.0	1.2	mA
		+12	-12	1.0	1.0	0.75	2.5	2.1	2.0	
Device Dissipation	P_T	+6	-6	20	24	20	45	42	45	mW
		+12	-12	120	120	105	230	220	210	
		V_{CC}	V_{EE}		R_L KΩ					
Voltage Gain (Differential)	A	+6	-6		2	—	35	—	—	42	—	dB
		+12	-12		1.6	—	40	—	—	45	—	
Max. Peak-to-Peak Output Voltage	$V_{O(P-P)}$	+6	-6		2	—	7	—	—	—	—	$V_{(P-P)}$
		+12	-12		1.6	—	15	—	—	—	—	
Common-Mode Input-Voltage Range	V_{CMR}	+6	-6			—	-2.5 to +4	—	—	—	—	V
		+12	-12			—	-5 to +7	—	—	—	—	
Common-Mode Rejection Ratio	CMRR	+6	-6			—	60	—	—	—	—	dB
		+12	-12			—	60	—	—	—	—	
Dynamic												
Power Gain	G_P *	V_{CC} = +9V, f = 100 MHz	Cascode	—	16	—	—	—	—	dB
			Diff-Ampl	—	14	—	—	—	—	
Noise Figure	NF *	V_{CC} = +9V, f = 100 MHz	Cascode	—	—	—	—	9	—	dB
			Diff-Ampl	—	—	—	—	9	—	

* Not Tested but Guaranteed

GROUPS C AND D ELECTRICAL CHARACTERISTICS SAMPLING TESTS (T_A = 25°C, V^+ = +12V, V^- = -12V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			Min.	Max.	
Input Offset Voltage	V_{IO}		-	5	mV
Input Bias Current	I_I		-	80	μA
Quiescent Oper. Current	I_6 or I_8		2.5	4.0	mA
Input Current (term. 7)	I_7		1.0	2.1	mA
Device Dissipation	P_T		120	220	mW
Power Gain	G_P	V_{CC} = +9V, f = 10.7 MHz Diff.-Ampl. Config.	28	-	dB

CA3039/...

High-Reliability Diode Array

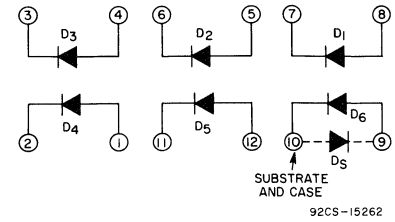
Six Ultra-Fast Low-Capacitance Diodes for Applications in Communications and Switching Systems of Aerospace, Military, and Critical Industrial Equipment

Features:

- **Excellent reverse recovery time—1 ns typ.**
- **Matched monolithic construction— V_F matched within 5 mV**
- **Low diode capacitance— C_D = 0.65 pF typical at V_R = -2 V**

Applications:

- **Balanced modulators or demodulators**
- **Ring modulators**
- **High speed diode gates**
- **Analog switches**



Schematic Diagram

The CA3039 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

ABSOLUTE-MAXIMUM RATINGS at T_A = 25° C

DISSIPATION:
- Any one diode unit ..... 100 mW
- Total for device ..... 600 mW
- For $T_A > 55°C$ ..... derate linearly 6.67 mW/° C

TEMPERATURE RANGE:
- Operating ..... -55 to +125° C
- Storage ..... -65 to +150° C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max. ..... 265° C

Peak Inverse Voltage, PIV for: D_1-D_5 ..... 5 V
D_6 ..... 0.5 V

Peak Diode-to-Substrate Voltage, V_{DI} for D_1-D_5 (term. 1,4,5,8 or 12 to term 10) ..... +20, -1 V

DC Forward Current, I_F ..... 25 mA

Peak Recurrent Forward Current, I_f ..... 100 mA

Peak Forward Surge Current, I_f (surge) ..... 100 mA

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT T_A = 25° C	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Each Diode DC Forward Voltage Drop	V_F	I_F = 3 mA	0.69	0.81	±0.010	V

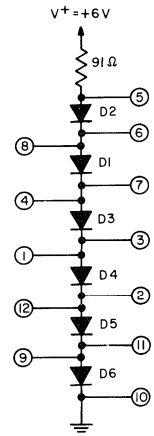
*Level /1 requires pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown on the next page.

Final Electrical Tests and Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
Each Diode: DC Forward Voltage Drop	V_F	I_F = 3 mA	0.82	0.69	0.47	1.0	0.86	0.63	V
DC Reverse Leakage Current	I_R	V_R = −4 V	–	–	–	–	100	–	nA
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = 40 μA	–	5	–	–	–	–	V
Between Any Two Diodes: Diode Offset Voltage	$\lvert V_{F1} - V_{F2} \rvert$	I_F = 1 mA	–	–	–	–	8	–	mV
Breakdown Voltage Isolation-to-Substrate		−50 V through a 25 kΩ resistor to terminal 10. Ground terminals 1 through 9, 11 and 12. Measure voltage at terminal 10.	–	–	–	−25	−25	−25	V

Groups C and D Electrical Characteristics Sampling Tests (T_A = 25° C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Each Diode: DC Forward Voltage Drop	V_F	I_F = 3 mA	0.69	0.81	V
DC Reverse Leakage Current	I_R	V_R = −4 V	–	100	nA
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = 40 μA	5	–	V
Between Any Two Diodes: Diode Offset Voltage	$\lvert V_{F1} - V_{F2} \rvert$	I_F = 1 mA	–	8	mV



92CS-22936

Burn-in and operating life-test circuit.

CA3045/...

High-Reliability General-Purpose Transistor Array

Three Isolated Transistors and One Differentially-Connected Transistor Pair For Low-Power Applications at Frequencies Through the VHF Range In Aerospace, Military, and Critical Industrial Equipment

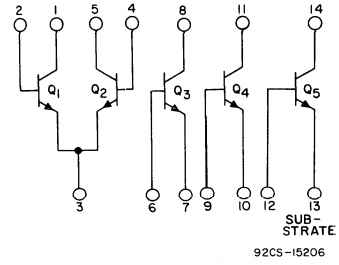
Features:

- **Two matched pairs of transistors**
  V_{BE} matched ±5 mV
  Input offset current 2 μA max. at I_C = 1 mA
- **5 general purpose monolithic transistors**
- **Operation from DC to 120 MHz**
- **Wide operating current range**
- **Low noise figure – 3.2 dB typ. at 1 kHz**
- **Full military temperature range**
  -55 to +125°C

Applications:

- **General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF**
- **Custom designed differential amplifiers**
- **Temperature compensated amplifiers**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.**

The CA3045 Slash (/) Series type is supplied in the 14-lead dual-in-line ceramic package ("D" suffix) or in chip form ("H" suffix).



ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C:

	EACH TRANSISTOR	TOTAL PACKAGE	
POWER DISSIPATION:			
At T_A up to 75°C	300	750	mW
At T_A > 75°C		Derate at 8 mW/°C	
Collector-to-Emitter Voltage, V_{CEO}	15	—	V
Collector-to-Base Voltage, V_{CBO}	20	—	V
Collector-to-Substrate Voltage, V_{CIO}*	20	—	V
Emitter-to-Base Voltage, V_{EBO}	5	—	V
Collector Current, I_C	50	—	mA
TEMPERATURE RANGE:			
Operating		-55 to +125	°C
Storage		-65 to +150	°C
LEAD TEMPERATURE (During Soldering):			
At distance 1/6" ± 1/32" (1.59 mm ±0.79 mm) from case for 10 s max	265°C		

*The collector of each transistor of the CA3045 is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits*

Electrical Characteristics, at $T_A = 25^oC$ For Each Transistor (Except where otherwise indicated)						
Characteristics	Symbol	Test Conditions	Limits			Units
			Min.	Max.	Max.Δ	
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$ (Except Q_5)	5	-	±0.5	V
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	-	0.5	±0.15	μA
Input Current	I_I	$I_C = 1mA$, $V_{CE} = 3V$	5	25	±3	μA
Base-to-Emitter Voltage	V_{BE}	$I_C = 1mA$, $V_{CE} = 3V$	0.6	0.8	±0.10	V

*Level/1 requires pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level 3 requires pre burn-in test only. The burn-in and operating life test circuit is shown on the next page.

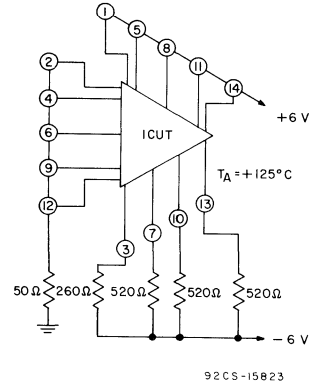
Group A Electrical Sampling Inspection

Characteristics	Symbol	Test Conditions	Limits for Indicated Temperature (°C)						Units
			Minimum			Maximum			
			-55	+25	+125	-55	+25	+125	
STATIC									
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	-	20	-	-	-	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	-	15	-	-	-	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_{CI} = 0$	-	20	-	-	-	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$ (Except Q_5)	-	5	-	-	-	-	V
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	-	-	-	-	40	-	nA
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	-	-	-	-	0.5	100	μA
Static Forward Current-Transfer Ratio	h_{FE}	$V_{CE} = 3V$, $I_C = 10mA$	-	30	-	-	-	-	-
		$V_{CE} = 3V$, $I_C = 1mA$	18	40	45	-	-	200	-
		$V_{CE} = 3V$, $I_C = 10\mu A$	-	15	-	-	-	-	-
Input Offset Current for Differential Pair, (Q_1, Q_2)	$\lvert I_{IO_1} - I_{IO_2} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	-	2	μA
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V$, $I_C = 1mA$	0.7	0.6	0.4	1.0	0.8	0.70	V
		$V_{CE} = 3V$, $I_C = 10mA$	-	-	-	-	1.0	-	V
Input Offset Voltage for Differential Pair, (Q_1, Q_2)	$\lvert V_{BE_1} - V_{BE_2} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	5	-	mV
Input Offset Voltage for Isolated Transistors $\lvert Q_3 - Q_4 \rvert$, $\lvert Q_4 - Q_5 \rvert$, $\lvert Q_5 - Q_3 \rvert$	V_{IO}	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	5	-	mV
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1mA$, $I_C = 10mA$	-	-	-	-	0.5	-	V
DYNAMIC									
Gain-Bandwidth Product (Q_3)	f_T	$V_{CE} = 3V$, $I_C = 3mA$, $f = 100$ MHz	-	300	-	-	-	-	MHz

CA3045/...

Groups C and D Electrical Characteristics Sampling Tests
(T_A = 25° C, V_{CC} = +6 V, V_{EE} = -6 V)

Characteristic	Symbol	Test Conditions	Limits		Units
			Min.	Max.	
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA I_C = 0 (Except Q5)	5	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA I_B = 0	15	-	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V I_B = 0	-	0.5	μA
Input Current	I_I	V_{CE} = 3 V I_C = 1 mA	5	25	μA
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V I_C = 1 mA	0.6	0.8	V



Burn-in and operating life-test circuit.

High-Reliability Dual High-Frequency Differential Amplifier

For Low-Power Applications at Frequencies up to 500 MHz in Aerospace, Military and Critical Industrial Equipment

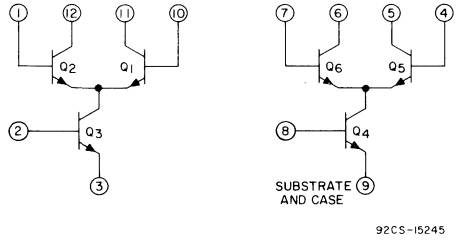
Features:

- **Power Gain 23 dB (typ.) at 200 MHz**
- **Noise Figure 4.6 dB (typ.) at 200 MHz**
- **Two differential amplifiers on a common substrate**
- **Independently accessible inputs and outputs**

The CA3049 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Applications

- **VHF amplifers**
- **VHF mixers**
- **Multifunction combinations – RF/Mixer/Oscillator; Converter/IF**
- **IF amplifiers (differential and/or cascode)**
- **Product detectors**
- **Doubly balanced modulators and demodulators**
- **Balanced quadrature detectors**
- **Cascade limiters**
- **Synchronous detectors**
- **Balanced mixers**
- **Synthesizers**
- **Balanced (push-pull) cascode amplifiers**
- **Sense amplifiers**



Schematic Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

POWER DISSIPATION, P:		
Any one transistor	300	mW
Total package	600	mW
For T_A>55°C Derate at:	6.67	mW/°C
TEMPERATURE RANGE:		
Operating	-55 to +125	°C
Storage	-65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16 ± 1/32" (1.59 mm ±0.79 mm) from case for 10 s max	265	°C

The following ratings apply for each transistor in the devices

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

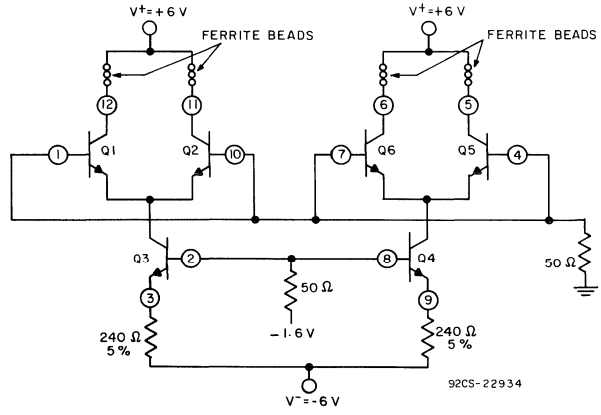
**The collector of each transistor of the CA3049T is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

CA3049/...

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS at $T_A = 25°C$	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Input Bias Current Q1, Q2, Q5, Q6	I_I	$I_3 = I_9 = 2mA$ $V^+ = +6\ V$	–	25.2	±6	μA
Input Bias Current Q3, Q4	I_I	$I_3 = I_9 = 2mA$ $V^+ = +6\ V$	–	50.4	±12	μA
Emitter-to Base Breakdown Voltage Q3, Q4	V_{EBO}	$I_E = 10\mu A$ $I_C = 0$	-5.3	–	±1.0	V
Collector Cutoff Current Q1 to Q6	I_{CBO}	$V_{CB} = 10\ V$ $I_E = 0$	–	95	±50	nA

* Level /1 requires pre and post burn-in electrical tests and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown below.



Burn-in and operating life-test circuit.

Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			-55	+25	+125	-55	+25	+125	
STATIC (Each Differential Ampifer)									
Input Offset Voltage	V_{IO}		—	—	—	7	5	7.5	mV
Input Offset Current	I_{IO}	$I_3 = I_9 = 2mA$ $V^+ = +6$ V	—	—	—	9	3	3	μA
Input Bias Current	I_I	$I_3 = I_9 = 2mA$ $V^+ = +6$ V	—	—	—	41	25.2	18	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	—	—	—	—	100	—	nA
Forward Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6$V, $I_C = 1mA$	—	—	—	—	874	—	mV
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	—	15	—	—	—	—	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	—	20	—	—	—	—	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_B = I_E = 0$	—	20	—	—	—	—	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	—	5	—	—	—	—	V
DYNAMIC									
Power Gain	P_G	f = 200 MHz	—	19	—	—	28	—	dB
Noise Figure	NF	f = 200 MHz	—	—	—	—	6.5	—	dB

Groups C and D Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Current Q_1, Q_2, Q_5, Q_6	I_C	$I_9 = I_3 = 2$ mA	0.77	1.25	mA
Input Bias Current Q_1, Q_2, Q_5, Q_6	I_I	$I_3 = I_9 = 2$ mA, $V^+ = +6$ V	–	25.2	μA
Input Bias Current Q_3, Q_4	I_I	$I_3 = I_9 = 2$ mA, $V^+ = +6$ V	–	50.4	μA
Power Gain	P_G		19	26	dB

CA3058/...

High-Reliability Zero - Voltage Switch

For 50/60 and 400-Hz Thyristor Control Applications
In Aerospace, Military and Critical Industrial Equipment

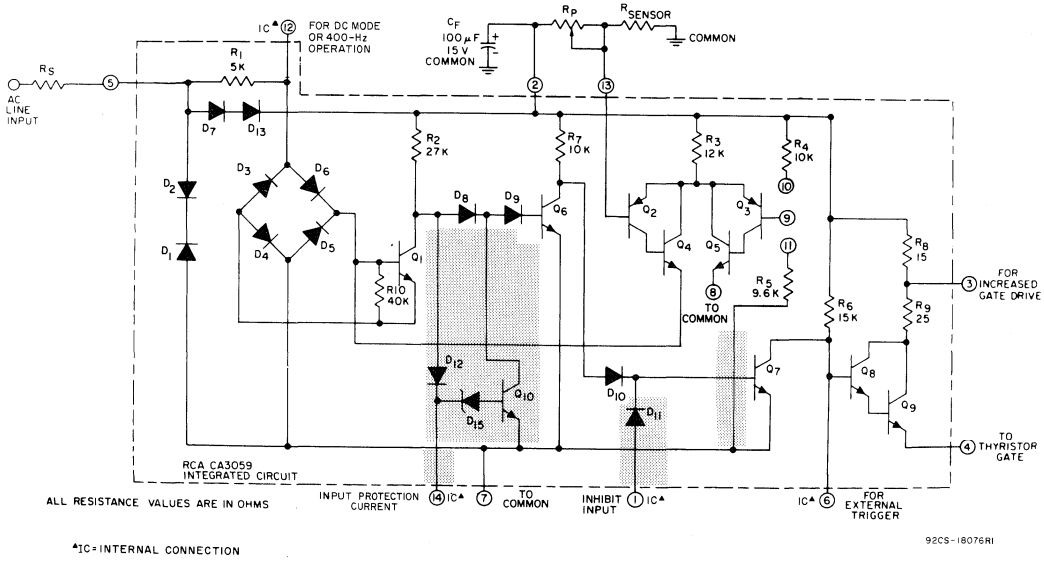
Features:

- **24 V, 120 V, 208/230 V, 277 V at 50 60, or 400 Hz operation**
- **Differential input**
- **Low balance input current (max.)1μA**
- **Built-in protection circuit for opened or shorted sensor (term. 14)**
- **Sensor range (R_X) - 2 to 100 kΩ**
- **DC mode (term 12)**
- **External trigger (term. 6)**
- **External inhibit (term. 1)**
- **DC supply volts (max.) 14**

Applications

- **Relay control ■ Heater control ■ Photosensitive control**
- **Valve control ■ Lamp control ■ Power one-shot control**
- **Synchronous switching of flashing lights**
- **On-off motor switching**
- **Differential comparator with self-contained power supply for industrial applications**
- **For detailed application information, see application note 1CAN-6182 "Applications of RCA Integrated Circuit Zero-Voltage Switches (CA3058, CA3059, CA3079)"**

The CA3058 Slash (/) Series type is supplied in the 14-Lead dual-in-line ceramic package ("D" suffix), or in chip form ("H" Suffix).



Schematic diagram of CA3058 zero-voltage switch. See also the functional block diagram.

MAXIMUM RATINGS, *Absolute Maximum Values, at T_A = 25°C*

DC Supply Voltage (between Terms. 2 and 7) ..... 14 V

DC Supply Voltage (between Terms. 2 and 8) ..... 14 V

Peak Supply Current (Terms. 5 and 8) ..... ±50 mA

Output Pulse Current (Term. 4) ..... 150 mA

Power Dissipation:

Up to T_A = 75°C ..... 700 mW

Above T_A = 75°C ..... Derate Linearly 8 mW/°C

Ambient Temperature Range:

Operating ..... -55 to +125°C

Storage ..... -65 to +150°C

Lead Temperature (During soldering)

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max ..... 265 °C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL NO.	1 Note 3	2	3	4	5 Note 1	6 Note 3	7	8	9	10	11	12 Note 3	13	14 Note 2,3
1 Note 3		*	*	*	*	15 0	10 -2	*	*	*	*	*	*	*
2			0 -15	0 -15	2 -14	0 -14	0 -14	0 -14	0 -14	0 -14	0 -14	*	0 -14	0 -14
3				0 -15	*	*	*	*	*	*	*	*	*	*
4					*	2 -10	*	*	*	*	*	*	*	*
5 Note 1						*	7 -7	*	*	*	*	*	*	*
6 Note 3							14 0	*	*	*	*	*	*	*
7								*	14 0	*	20 0	2.5 -2.5	14 0	6 -6
8									10 0	*	*	*	*	*
9										*	*	*	*	*
10											*	*	*	*
11												*	*	*
12 Note 3													*	*
13														*
14 Note 3														

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to -10 volts.

Note 1 – Resistance should be inserted between Term. 5 and external supply or line voltage for limiting current into Term. 5 to less than 50 mA.

Note 2 – Resistance should be inserted between Term. 14 and external supply for limiting current into Term. 14 to less than 2 mA.

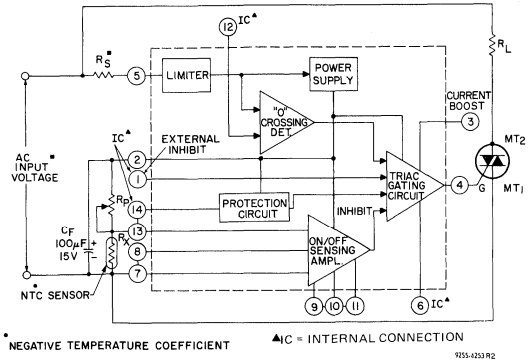
NOTE 3: For the CA3079 indicated terminal is internally connected and therefore, should not be used.

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

MAXIMUM CURRENT RATINGS

I_{IN} mA	I_{OUT} mA
10	0.1
150	10
*	*
0.1	150
50	10
*	*
*	*
0.1	2
*	*
*	*
*	*
50	50
*	*
2	2

CA3058/...



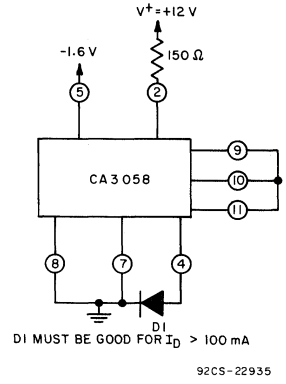
Functional block diagram.

AC Input Voltage (50/60 to 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS at T_A = 25°C	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
DC Supply Voltage	V_S	R_S = 10 kΩ, I_L = 0	6.0	7.0	±0.2	V
Output Leakage Current (Inhibit Mode)	I_4		–	10	±0.5	μA
Peak Output Current (Pulsed) With Internal Power Supply	I_{OM}(4)	Terminal 3 Open, V_{GT}=0	50	–	±10	mA
Input Bias Current	I_I		–	1.0	±0.2	μA

*Level /1 requires pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown below.



Burn-in and operating life test circuit.

Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS f = 50/60 Hz	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
DC Supply Voltage	V_S	R_S = 10 kΩ, I_L = 0	5.5	6.0	5.5	7.5	7.0	7.5	V
Output Leakage Current (Inhibit Mode)	I_4		–	–	–	20	10	20	μA
Input Bias Current	I_I		–	–	–	1.0	1.0	1.0	μA
Inhibit Input Ratio	V_G/V_Z	Voltage ratio of terminal 9 to terminal 2.	0.450	0.465	0.450	0.520	0.520	0.520	
Peak Output Current (Pulsed) With Internal Power Supply	I_{OM} (4)	Terminal 3 open, V_{GT} = 0	–	50	–	–	–	–	mA
		Terminals 2 and 3 shorted, V_{GT} = 0	–	90	–	–	–	–	mA
Pulse Duration After Zero Crossing:									
For Positive dv/dt		C external = 0	–	70	–	–	140	–	μS
For Negative dv/dt		R external = 0	–	70	–	–	140	–	μS

Groups C and D Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS f = 50/60 Hz	LIMITS		UNITS
			MIN.	MAX.	
DC Supply Voltage	V_S	R_S = 10 kΩ, I_L = 0	5.9	7.1	V
Output Leakage Current (Inhibit Mode)	I_4		–	11	μA
Peak Output Current (Pulsed) With Internal Power Supply	I_{OM} (4)	Terminal 3 Open, V_{GT} = 0	45	–	mA
Input Bias Current	I_I		–	1.2	μA

CA3078A/...

High-Reliability Micropower Operational Amplifier

For Applications in Aerospace, Military, and Critical Industrial Equipment

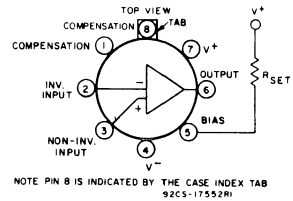
Features:

- **Low standby power: as low as 700 nW**
- **Wide supply voltage range: ±0.75 to ±15 V**
- **High peak output current: 6.5 mA min.**
- **Adjustable quiescent current**
- **Output short-circuit protection**

Applications:

- **Portable electronics**
- **Medical electronics**
- **Instrumentation**
- **Telemetry**

The CA3078A is supplied in the standard 8-lead TO-5 package ("T" suffix), the 8-lead dual-in-line formed-lead "DIL-CAN" package ("S" suffix), or in chip form ("H" suffix).

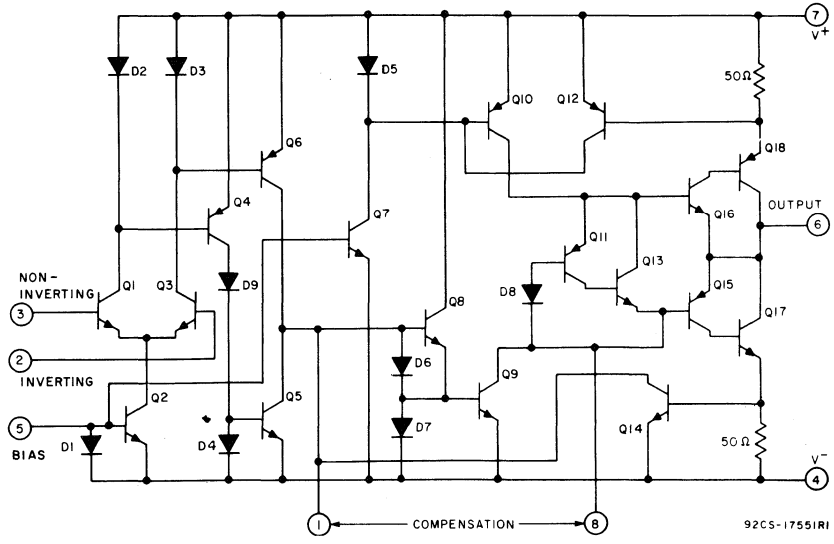


Functional diagram of the CA3078AS and CA3078AT.

MAXIMUM RATINGS, *Absolute Maximum Values at* $T_A = 25°C$

DC SUPPLY VOLTAGE (Between V+ and V- terminal)	36V
DIFFERENTIAL INPUT VOLTAGE	±6V
DC INPUT VOLTAGE	V+ to V-
INPUT SIGNAL CURRENT	0.1 mA
OUTPUT SHORT-CIRCUIT DURATION*	No limitation
DEVICE DISSIPATION	250mW (up to 125°C)
TEMPERATURE RANGE:	
Operating	-55 to +125°C
Storage	-65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59±0.79mm) from case for 10 s max.	+265°C

**Short circuit may be applied to ground or to either supply.*

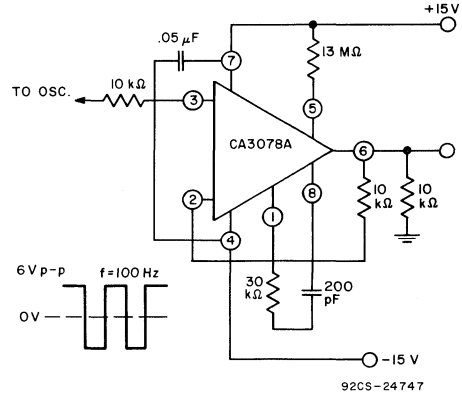


Schematic diagram of the CA3078A.

Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits*
ELECTRICAL CHARACTERISTICS, *at T_A = 25°C, V+ = +6V, V- = -6V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX.▲	
Input Offset Voltage	V_{IO}	$R_S = \leqslant 10K$	–	3.5	±1	mV
Input Offset Current	I_{IO}		–	2.5	±0.4	nA
Input Bias Current	I_I		–	12	±1.5	nA
Maximum Output Current	I_{OM}^+ or I_{OM}^-		6.5	–	±1	mA

*Level /1 requires pre burn-in electrical tests, post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown below.



Burn-in and operating life-test circuit.

CA3078A/...

Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS Rset = 5.1 MΩ I_Q = 20 μA						UNITS
					MINIMUM			MAXIMUM			
		V^+ & V^-	R_S KΩ	R_L KΩ	-55	+25	+125	-55	+25	+125	
Input Offset Voltage	V_{IO}	6	≤10	–	–	–	–	4.5	3.5	4.5	mV
Input Offset Current	I_{IO}		–	–	–	–	–	10	2.5	5	nA
Input Bias Current	I_{IB}		–	–	–	–	–	50	12	50	nA
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10	90	92	90	–	–	–	dB
Total Quiescent Current	I_Q		–	–	–	–	–	45	25	45	μA
Device Dissipation	P_D		–	–	–	–	–	540	300	540	μW
Maximum Output Voltage	V_{OM}		–	≥10	±5	±5.1	±5	–	–	–	V
Common-Mode Input Voltage Range	V_{ICR}		≤10	–	-5 to +5	-5 to +5	-5 to +5	–	–	–	V
Common-Mode Rejection Ratio	CMRR		≤10	–	–	80	–	–	–	–	dB
Maximum Output Current	I_{OM}^+ or I_{OM}^-		–	–	6.5	6.5	6.5	30	30	30	mA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$		≤10	–	–	76	–	–	150	–	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$			–	–	76	–	–	150	–	
					R_{SET} = 13MΩ, I_Q = 20 μA						
Input Offset Voltage	V_{IO}	15	≤10	–	–	–	–	4.5	3.5	4.5	mV
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10	88	92	88				dB
Total Quiescent Current	I_Q		–	–	–	–	–	50	30	50	μA
Device Dissipation	P_D		–	–	–	–	–	1350	750	1350	μW
Maximum Output Voltage	V_{OM}		–	≥10	±13.5	±14.1	±13.5	–	–	–	V
Common-Mode Rejection Ratio	CMRR		≤10	–	–	80	–	–	–	–	dB
Input Bias Current	I_{IB}		–	–	–	–	–	55	14	55	nA
Input Offset Current	I_{IO}		–	–	–	–	–	10	2.7	5.5	nA

Groups C and D Electrical Characteristics Sampling Tests at T_A = +25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS R_{SET} = 5.1 MΩ I_Q = 20 μA		UNITS
		V+ and V−	R_S	R_L	MIN.	MAX.	
Input Offset Voltage	V_{IO}	6	≤ 10 KΩ		–	4.5	mV
Input Offset Current	I_{IO}				–	4	nA
Input Bias Current	I_I				–	28	nA
Open-Loop Differential Voltage Gain	A_{OL}			≥ 10 KΩ	84	–	dB
Maximum Output Voltage	V_{OM}			≥ 10 KΩ	±4.0	–	V
		R_{SET} = 13 mΩ I_Q = 20 μA					
Input Offset Voltage	V_{IO}	15	≤ 10 KΩ		–	4.5	mV
Large-Signal Voltage Gain	A_{OL}			≥ 10 KΩ	84	–	dB
Maximum Output Voltage	V_{OM}			≥ 10 KΩ	±10	–	V

High-Reliability Operational Transconductance Amplifiers Gateable-Gain Blocks

For Applications In Aerospace, Military and Critical Industrial Equipment

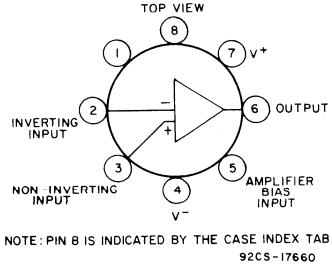
Features:

- **Slew rate (unity gain, compensated): 50 V/μs**
- **Adjustable power consumption: 10 μW to 30 mW**
- **Flexible supply voltage range: ±2 V to ±15 V**
- **Fully adjustable gain: 0 to $g_m R_L$ limit**
- **Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1)**
- **Extended g_m linearity: 3 decades**
- **Hermetic package: 8-lead TO-5 style**

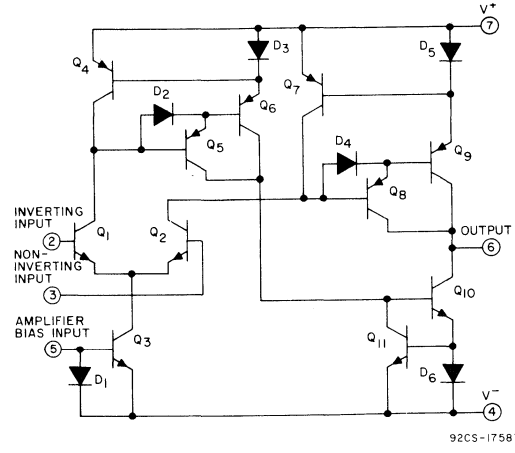
Applications:

- **Sample and hold**
- **Multiplex**
- **Voltage follower**
- **Multiplier**
- **Comparator**

The CA3080 and CA3080A Slash (/) Series types are supplied in the 8-lead TO-5 style package ("T" suffix), in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix), or in chip form ("H" suffix).



Functional diagram of CA3080 and CA3080A.



Schematic diagram for CA3080 and CA3080A.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C*

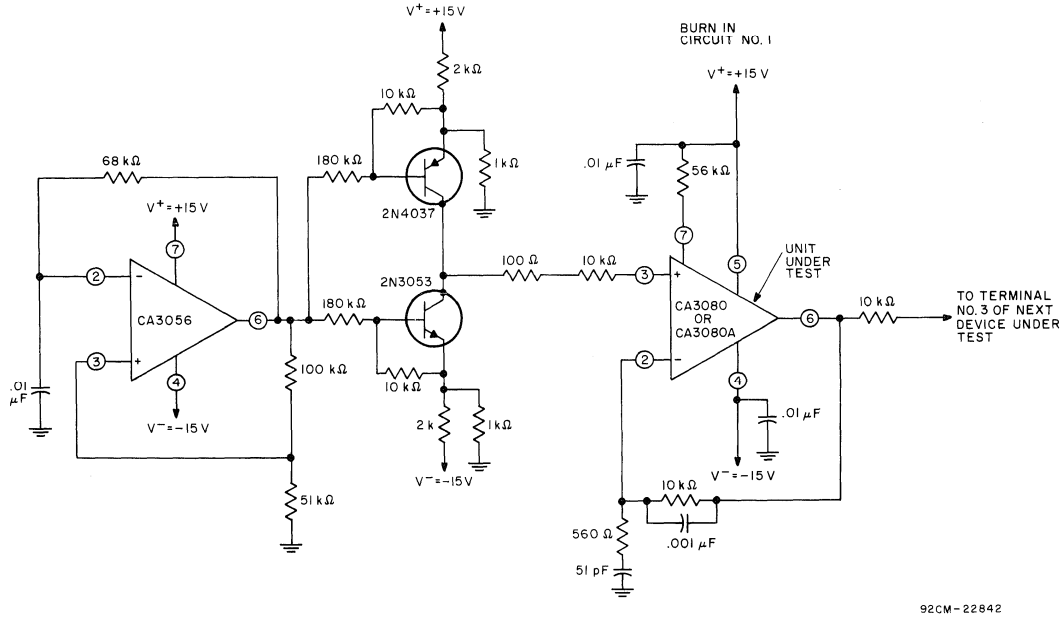
DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V
DIFFERENTIAL INPUT VOLTAGE	± 5 V
DC INPUT VOLTAGE	V^+ to V^-
INPUT SIGNAL CURRENT	1 mA
AMPLIFIER BIAS CURRENT	2 mA
OUTPUT SHORT-CIRCUIT DURATION	INDEFINITE
DEVICE DISSIPATION	125 mW
TEMPERATURE RANGE:	
Operating	
CA3080	0 to 70 °C
CA3080A	-55 to +125° C
Storage	65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max.	265° C

CA3080/..., CA3080A/...

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT T_A = 25° C V^+ = +15 V, V^- = −15 V	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Input Offset Voltage	V_{IO}	CA3080	–	5	±0.2	mV
		CA3080A	–	2	±0.15	
Input Offset Current	I_{IO}	CA3080	–	0.6	±0.05	μA
		CA3080A	–	0.6	±0.05	
Input Bias Current	I_I	CA3080	–	5	±0.25	μA
		CA3080A	–	5	±0.25	
Forward Transconductance	g_m	CA3080	6700	13000	±3000	umho
		CA3080A	7700	12000	±3000	

*Level /1 requires pre and post burn-in electrical tests and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown below.



Burn-in and operating life test circuit.

Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^- = -15$ V, $V^+ = +15$ V, $I_{ABC} = 0.5$ mA		LIMITS FOR INDICATED TEMPERATURES (°C) MINIMUM −55	MINIMUM +25	MINIMUM +125	MAXIMUM −55	MAXIMUM +25	MAXIMUM +125	UNITS
Input Offset Voltage	V_{IO}		CA3080	–	–	–	6	5	6	mV
			CA3080A	–	–	–	5	2	5	
Input Offset Current	I_{IO}		CA3080	–	–	–	1.2	0.6	0.7	μA
			CA3080A	–	–	–	1.2	0.6	0.7	
Input Bias Current	I_I		CA3080	–	–	–	8	5	5	μA
			CA3080A	–	–	–	8	5	5	
Forward Transconductance	g_m		CA3080	5400	6700	5400	13000	13000	20000	umho
			CA3080A	4000	4000	4000	9000	12000	18000	
Peak Output Voltage Positive	$+V_{OM}$	$R_L = \infty$	CA3080 CA3080A	11.6	12	12	–	–	–	V
Peak Output Voltage Negative	$-V_{OM}$	$R_L = \infty$	CA3080 CA3080A	11.8	12	12	–	–	–	V
Peak Output Current	$\lvert I_{OM} \rvert$	$R_L = 0$	CA3080	350	350	320	750	650	750	μA
		$R_L = 0$	CA3080A	350	350	320	750	650	750	
Amplifier Supply Current	I_A		CA3080	0.7	0.8	0.7	1.4	1.2	1.4	mA
			CA3080A	0.7	0.8	0.7	1.4	1.2	1.4	
Common-Mode Rejection Ratio	C_{MRR}		CA3080	80	80	80	–	–	–	dB
			CA3080A	80	80	80	–	–	–	
Supply Voltage Rejection Ratio	V_{RR}		CA3080	–	–	–	150	150	150	μV/V
			CA3080A	–	–	–	150	150	150	
Differential Input Current		$I_{ABC} = 10$ mA, $V_{DIFF} = 4$ V	CA3080	–	–	–	–	7	–	nA
		$I_{ABC} = 10$ mA, $V_{DIFF} = 4$ V	CA3080A	–	–	–	–	5	–	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	CA3080	–	–	–	–	7	–	nA
		$I_{ABC} = 0$, $V_{TP} = 0$	CA3080A	–	–	–	–	5	–	
		$I_{ABC} = 0$, $V_{TP} = 36$	CA3080	–	–	–	–	7	–	nA
		$I_{ABC} = 0$, $V_{TP} = 36$	CA3080A	–	–	–	–	5	–	

Groups C and D Electrical Characteristics Sampling Tests ($T_A = 25°C$)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V		LIMITS MIN.	LIMITS MAX.	UNITS
Input Offset Voltage	V_{IO}		CA3080	–	6.5	mV
			CA3080A	–	5.5	
Input Offset Current	I_{IO}		CA3080	–	1.2	μA
			CA3080A	–	1.2	
Input Bias Current	I_I		CA3080	–	10	μA
			CA3080A	–	10	
Forward Transconductance to Terminal No. 1	g_m		CA3080	6500	14000	umho
			CA3080A	7000	13000	
Peak Output Current	$\lvert I_{OM} \rvert$		CA3080	300	700	μA
			CA3080A	300	700	
Peak Output Voltage	$+V_{OM}$		CA3080	11	–	V
			CA3080A	11	–	
	$-V_{OM}$		CA3080	−11	–	
			CA3080A	−11	–	

High-Reliability General-Purpose High-Current N-P-N Transistor Arrays

CA3081F-Common-Emitter Array
CA3082F-Common-Collector Array

For Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Directly Drive 7-Segment Incandescent Displays and Light-Emitting-Diode (LED) Displays

Features:
- *7 transistors permit a wide range of applications in either a common-emitter (CA3081F) or common-collector (CA3082F) configuration*
- *High I_C: 100 mA max.*
- *Low V_{CE}(sat) (at 50 mA): 0.4 V typ.*

Applications:
- *Drivers for:*
  - *Incandescent display devices*
  - *LED (e.g. RCA-40736R GaAs High-Efficiency Emitting Diode)*
  - *Relay control*
  - *Thyristor firing*

The RCA-CA3081F and CA3082F "Slash"(/) Series types are supplied in a 16-lead dual-in-line frit-seal ceramic (CERDIP) package (F suffix) that conforms to MIL-M-38510 Case Outline D-2. This package includes a separate substrate connection for maximum flexibility in circuit design. Both types are also available in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25° C*

POWER DISSIPATION:
- ANY ONE TRANSISTOR ..... 500 mW
- TOTAL PACKAGE ..... 750 mW
- ABOVE 55° C ..... DERATE LINEARLY 6.67 mW/° C

AMBIENT TEMPERATURE RANGE:
- OPERATING ..... -55 to +125 °C
- STORAGE ..... -65 to +150 °C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 in.(1.59 ± 0.79 mm) from case for 10 s max. ..... 265 °C

THE FOLLOWING RATINGS APPLY FOR EACH TRANSISTOR IN THE DEVICE:

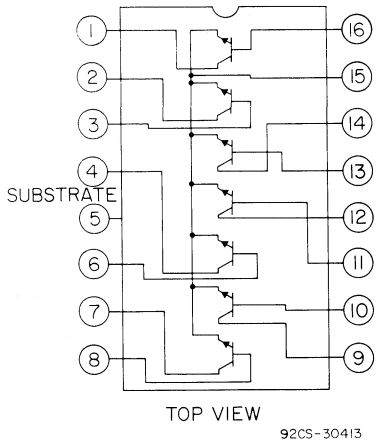
COLLECTOR-TO-EMITTER VOLTAGE (V_{CEO}) ..... 16 V
COLLECTOR-TO-BASE VOLTAGE (V_{CBO}) ..... 20 V
COLLECTOR-TO-SUBSTRATE VOLTAGE (V_{CIO})■ ..... 20 V
EMITTER-TO-BASE VOLTAGE (V_{EBO}) ..... 5 V
COLLECTOR CURRENT (I_C) ..... 100 mA
BASE CURRENT (I_B) ..... 20 mA

■The collector of each transistor of the CA3081F/ and CA3082F/ is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

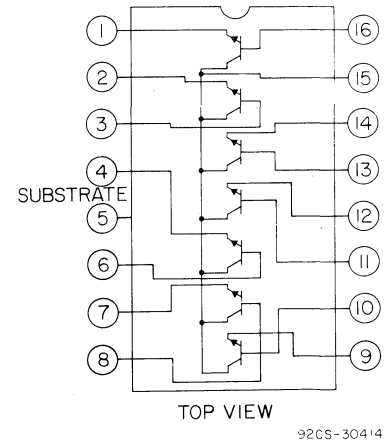
PRE-BURN-IN ELECTRICAL AND POST BURN-IN ELECTRICAL TESTS AND (Δ) DELTA LIMITS, T_A=25° C[1]

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Max.	Max. Δ[2]	
Emitter-to-Base Breakdown Voltage	$V_{BR(EBO)}$	I_E=0.5 mA	5	—	±0.6	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=0.5 V, I_C=50 mA	—	1.25	±0.15	mA
Base-to-Emitter Saturation Voltage	V_{BE}(sat)	I_C=30 mA, I_B=1 mA	—	1.0	±0.2	V
Collector-Cutoff-Current	I_{CEO}	V_{CE}=10 V, I_B=0	—	10	±4	μA

NOTES:
1. For each transistor.
2. Applicable for level /1 only.

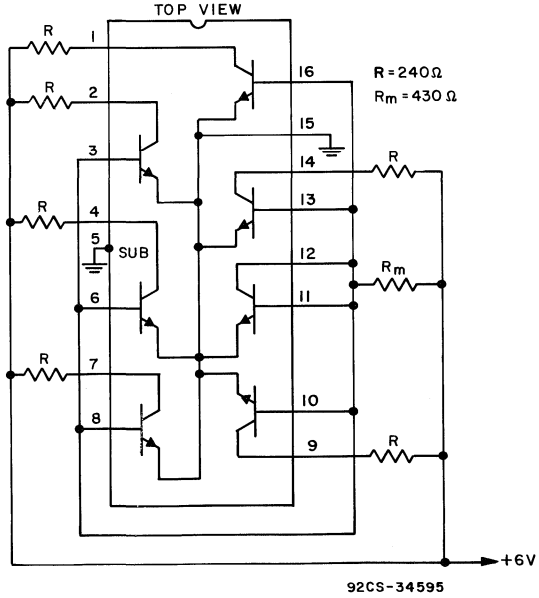


CA3081
Common-Emitter Configuration

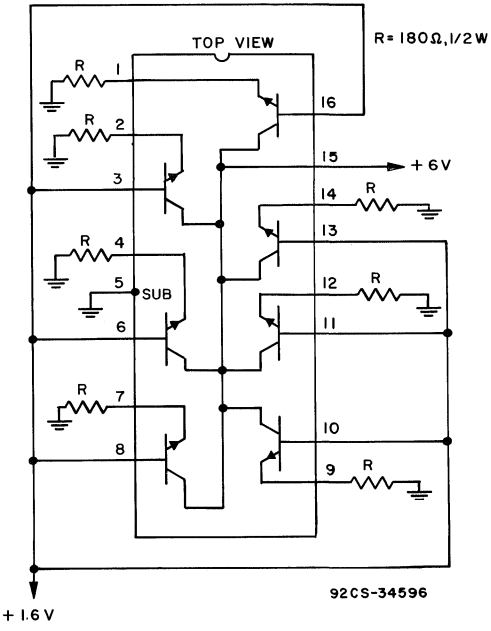


CA3082
Common-Collector Configuration

Functional diagrams of types CA3081F and CA3082F.



Burn-in and operating life-test circuit for CA3081F.



Burn-in and operating life-test circuit for CA3082F.

CA3081/..., CA3082/...

GROUP A ELECTRICAL SAMPLING INSPECTION

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURE (°C)						UNITS
			MIN.			MAX.			
			-55	+25	+125	-55	+25	+125	
Collector-to-Base Breakdown Voltage	$V_{(BR)CES}$	I_C=500 μA, I_E=0	—	20	—	—	—	—	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C=500 μA, I_E=0, I_B=0	—	20	—	—	—	—	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1 mA, I_B=0	—	16	—	—	—	—	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=0.5 mA	—	5	—	—	—	—	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=0.5 V, I_C=30 mA	15	30	—	—	—	—	
		V_{CE}=0.8 V, I_C=50 mA	—	40	—	—	—	—	
Base-to-Emitter Saturation Voltage	V_{BE}(sat)	I_C=30 mA, I_B=1 mA	—	—	—	1.2	1.0	0.9	V
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)								
CA3081F, CA3082F		I_C=30 mA, I_B=1 mA	—	—	—	—	0.5	0.7	
CA3081F		I_C=50 mA, I_B=5 mA	—	—	—	—	0.7	—	V
CA3082F		I_C=50 mA, I_B=5 mA	—	—	—	—	0.8	—	
Collector-Cutoff-Current	I_{CEO}	V_{CE}=10 V, I_B=0	—	—	—	—	10	500	μA
	I_{CBO}	V_{CB}=10 V, I_E=0	—	—	—	—	1	—	

TABLE II - GROUP C AND D ELECTRICAL ENDPOINT TESTS, T_A=25° C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			Min.	Max.	
Collector-to-Base Breakdown Voltage	$V_{(BR)CES}$	I_C=500 μA, I_E=0	18.5	—	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1 mA, I_B=0	16	—	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=0.5 V, I_C=50 mA	—	1.8	mA

CA3085/..., CA3085A/..., CA3085B/...

High-Reliability Positive Voltage Regulators

For Regulated Voltages from 1.7 V to 46 V at Currents up to 100 mA for Application in Aerospace, Military and Critical Industrial Equipment

Features

- **Up to 100 mA output current**
- **Input and output short-circuit protection**
- **Load and line regulation: 0.025%**
- **Pin compatible with LM100 Series**
- **Adjustable output voltage**

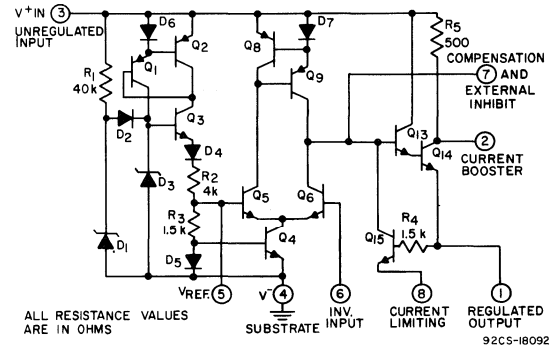
Type	V_{IN} Range V	V_{OUT} Range V	Max. I_{OUT} mA	Max. Load Regulation % V_{OUT}
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

*This value may be extended to 100mA; however, regulation is not specified beyond 12mA.

Applications

- **Shunt voltage regulator**
- **Current regulator**
- **Switching voltage regulator**
- **High-current voltage regulator**
- **Combination positive and negative voltage regulator**
- **Dual tracking regulator**

The CA3085, CA3085A, and CA3085B Slash (/) Series type are supplied in the 8-lead TO-5 style package ("T" suffix) in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix), or in chip form ("H" suffix).



Schematic diagram of CA3085 Series.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at T_A = 25°C

Power Dissipation: Without Heat Sink	With Heat Sink
up to T_A = 55 °C ..... 630 mW	up to T_C = 55° C .....1.6 W
above T_A = 55°C derate linearly @ 6.67 mW/°C	above T_C = 55°C .....derate linearly at 16.7 mW/°C

Unregulated Input Voltage:

CA3085 ..... 30 V
CA3085A ..... 40 V
CA3085B ..... 50 V

TEMPERATURE RANGE

Operating ..... -55 to +125°C
Storage ..... -65 to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max. ..... 265°C

CA3085/..., CA3085A/..., CA3085B/...

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

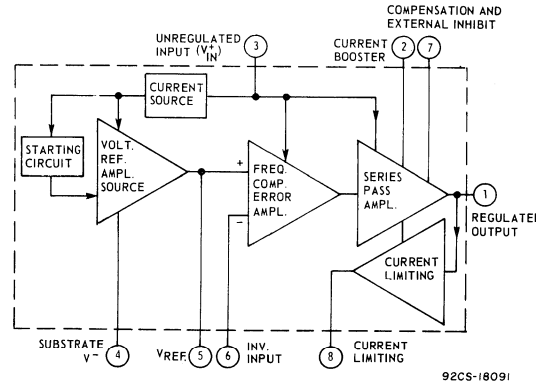
TERMINAL No.	5	6	7	8	1	2	3	4
5	–	+5 −5	*	*	*	*	*	+10 0
6	–	–	*	*	*	*	*	*
7	–	–	–	+3 −10	+3 −10	*	*	+‡ 0
8	–	–	–	–	+5 −1	*	*	*
1	–	–	–	–	–	+10 −‡	0 −‡	+‡ 0
2	–	–	–	–	–	–	0 –	+‡ 0
3	–	–	–	–	–	–	–	+‡ 0
4	–	–	–	–	–	–	–	Substrate & Case

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡30 V for CA3085
40 V for CA3085A
50 V for CA3085B

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	−0.1
7	1.0	−1.0
8	0.1	10
1	20	150
2	150	60
3	150	60
4	–	–



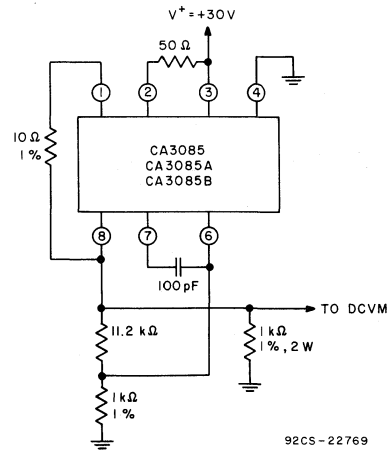
Block diagram of CA3085 Series.

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $T_A = 25°C$	LIMITS MIN.	LIMITS MAX.	LIMITS MAX. Δ	UNITS
Reference Voltage	V_{REF}		1.4	1.8	±0.05	V
Output Voltage Minimum Value	$V_{O(min)}$	V^+_{IN} = 7.5 V or 30 V	–	1.8	±0.1	V
Output Voltage Maximum Value	$V_{O(max)}$	V^+_{IN} = 30 V	26	–	±0.5	V
Limiting Current	I_{LIM}	V^+_{IN} = 7.5 V, R_{SCP} = 7Ω, R_L = 10Ω	–	115	±10	mA
Output Drift Voltage			16	22	±0.5	V

*Level /1 requires pre burn-in and post burn-in electrical tests and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown on the next page.

CA3085/..., CA3085A/..., CA3085B/...



Burn-in and operating life-test circuit.

Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
Reference Voltage	V_{REF}		1.3	1.4	1.4	1.8	1.8	1.9	V
Output Voltage Minimum Value	$V_{O(min)}$	V^+_{IN} = 7.5 V, or 30 V	1.9	1.7	1.7	–	–	–	V
Maximum Value	$V_{O(max)}$	V^+_{IN} = 30 V, CA3085	25	26	24	–	–	–	
		V^+_{IN} = 40 V, CA3085A	35	36	34	–	–	–	V
		V^+_{IN} = 50 V, CA3085B	45	46	44	–	–	–	
Load Regulation		I_L = 1 to 100 mA, R_{SCP} = 0, CA3085A	–	–	–	0.75	0.15	0.75	%/V_{OUT}
		R_{SCP} = 0, CA3085B	–	–	–	0.75	0.15	0.75	%/V_{OUT}
		I_L = 1 to 12 mA, CA3085	–	–	–	0.15	0.10	0.15	%/V_{OUT}
Line Regulation		I_L = 1 mA, CA3085	–	–	–	0.2	0.1	0.2	%/V
		R_{SCP} = 0, CA3085A	–	–	–	0.15	0.075	0.15	%/V
		R_{SCP} = 0, CA3085B	–	–	–	0.12	0.04	0.12	%/V

Groups C and D Electrical Characteristics Sampling Tests (T_A=25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Reference Voltage	V_{REF}		1.4	1.8	V
Minimum Output Voltage	$V_{O(min)}$	V^+_{IN} = 30 V, CA3085	–	1.9	V
		V^+_{IN} = 40 V, CA3085A	–	1.9	V
		V^+_{IN} = 50 V, CA3085B	–	2.0	V
Load Regulation		I_L = 1 to 100 mA, R_{SCP} = 0, CA3085A	–	0.3	%/V_{OUT}
		R_{SCP} = 0, CA3085B	–	0.75	
		I_L = 1 to 12 mA, CA3085	–	0.15	
Line Regulation		I_L = 1 mA, CA3085	–	0.25	%/V
		R_{SCP} = 0, CA3085A	–	0.1	
		R_{SCP} = 0, CA3085B	–	0.05	

*Level /1 requires pre burn-in and post burn-in electrical tests and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown on the next page.

CA3094/..., CA3094A/...

High-Reliability Programmable Power Switch/Amplifiers

For Control & General-Purpose Applications

In Aerospace, Military, and Critical Industrial Equipment

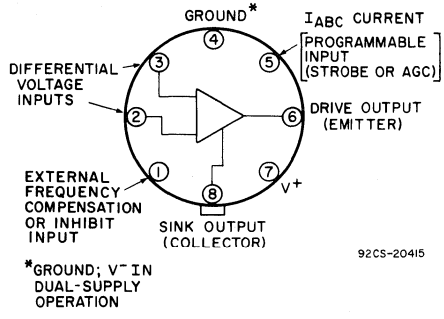
Features:

- Designed for *single* or dual power supply
- Programmable: strobing, gating, squelching, AGC capabilities
- Can deliver 3 watts (avg.) or 10 W (peak) to external load (in switching mode)
- High-power, single-ended class A amplifier will deliver power output of 0.6 watt (1.6 W device dissipation)
- Total harmonic distortion (THD) @ 0.6 W in class A operation — 1.4% typ.
- High current-handling capability — 100 mA (avg.), 300 mA (peak)
- Sensitivity controlled by varying bias current
- Output: "sink" or "drive" capability

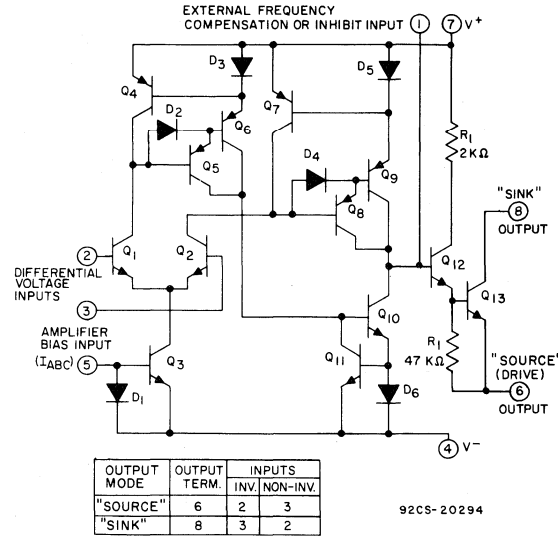
Applications:

- Error-signal detector: temperature control with thermistor sensor; speed control for shunt wound dc motor
- Over-current, over-voltage, over-temperature protectors
- Dual-tracking power supply with RCA-CA3085
- Wide-frequency-range oscillator ■ Analog timer
- Level detector ■ Alarm systems ■ Voltage follower
- Ramp-voltage generator ■ High-power comparator
- Ground-fault interrupter (GFI) circuits

The CA3094 and CA3094A "Slash" (/) Series types are supplied in the 8-lead TO-5 style ceramic package ("T" Suffix), in 8-lead TO-5 style ceramic package with dual-in-line formed leads - ("S" Suffix DIL-CAN) - or in chip form ("H" Suffix).



Terminal Connections (Bottom View, Terminal End)



OUTPUT MODE	OUTPUT TERM.	INPUTS	
		INV.	NON-INV.
"SOURCE"	6	2	3
"SINK"	8	3	2

Schematic diagram of CA3094 and CA3094A Slash (/) Series Types.

CA3094/..., CA3094A/...

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C*

	CA3094/Series	CA3094A/Series	
DC Supply Voltage:			
Dual Supply	± 12 V	± 18 V	V
Single Supply	24 V	36 V	V
DC Differential Input Voltage (Terminals 2 and 3)	± 5*		V
DC Common-Mode Input Voltage	Pin 4 ≤ Pins 2 & 3 ≤ Pin 7		
Peak Input Signal Current (Terminals 2 and 3)	± 1		mA
Peak Amplifier Bias Current (Terminal 5)	2		mA
Output Current:			
Peak	300		mA
Average	100		mA
Device Dissipation:			
Up to T_A = 55°C:			
Without heat sink	630		mW
With heat sink	1.6		W
Above T_A = 55°C:			
Without heat sink derate linearly	6.67		mW/°C
With heat sink derate linearly	16.7		mW/°C
Thermal Resistance (Junction to Air)	140		°C/W
Ambient Temperature Range:			
Operating	–55 to +125		°C
Storage	–65 to +150		°C
Lead Temperature (During Soldering): At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	265		°C

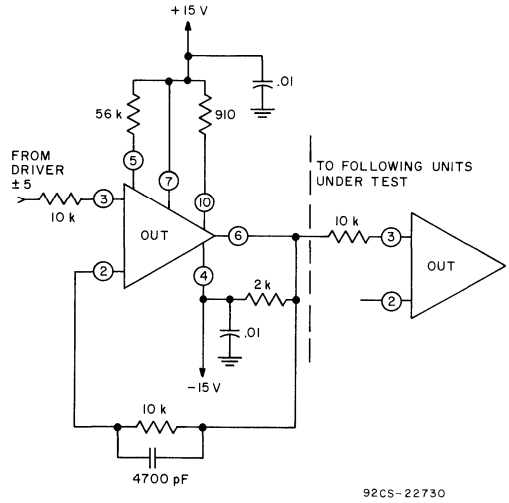
*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.

Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits *

Characteristic	Symbol	Test Conditions V^+ = 30 V, I_{ABC} = 100 μA T_A = 25°C	Limits Min	Limits Max	Limits Max△	Units
Input Offset Voltage	V_{IO}		–	0.6	±0.2	V
Input Offset Current	I_{IO}		–	0.22	±0.02	μA
Input Bias Current	I_I		0.04	1.1	±0.1	μA
Forward Transconductance To Terminal No.1	g_m		1850	4000	±660	μmho
Collector-to-Emitter Saturation Voltage (Terminal No.8)	$V_{CE(sat)}$	I_C = 50 mA Terminal No.6 grounded	0.05	1.0	±0.02	V

* Level /1 requires pre and post burn-in electrical tests and delta limits.
Level /3 requires pre-burn in electrical test only. The burn-in circuit is shown on the next page.

CA3094/..., CA3094A/...



Burn-in and life-test circuit.

Group A Electrical Sampling Inspection

Characteristic	Symbol	Test Conditions V^+ = 30 V, I_{ABC} = 100 μA Unless Otherwise Specified	Limits For Indicated Temperatures (°C) Minimum −55	Minimum +25	Minimum +125	Maximum −55	Maximum +25	Maximum +125	Units
Input Offset Voltage	V_{IO}		–	–	–	7	5	7	mV
Input Offset Current	I_{IO}		–	–	–	0.85	0.2	0.22	μA
Input Bias Current	I_I		–	–	–	3.2	0.5	1.1	μA
Forward Transconductance To Terminal No. 1	g_m		910	1650	1850	2100	2750	4000	μmho
Input Offset Voltage Change	$\lvert\triangle V_{IO}\rvert$	Change in V_{IO} between I_{ABC} = 100 μA and I_{ABC} = 5 μA	–	–	–	–	8	–	mV
		Change in V_{IO} between I_{ABC} = 100 μA and I_{ABC} = 15 μA	–	–	–	3.2	–	3.2	mV
Peak Output Voltage (Terminal No.6) with Q_{13} "ON"	V^+_{OM}	R_L = 2 kΩ to ground	26	26	26	–	–	–	V
Common Mode Rejection Ratio	CMRR		70	70	70	–	–	–	dB
Supply Current	I^+_{Supply}		–	–	–	400	400	400	μA
Power Supply Rejection	$\triangle V_{IO}/\triangle V$		–	–	–	150	150	150	μV/V
Collector-to-Emitter Saturation Voltage (Terminal No. 8)	$V_{CE(sat)}$	I_C = 50 mA Terminal No.6 Grounded	0.05	0.05	0.05	0.8	0.8	1.0	V
Output Leakage Current Q_{13} "OFF"	$-I_{OL}$	V^+ = 25 V	−10	−10	−10	0.1	0.1	0.1	μA
Max. Output Current Q_{13} "ON"	$-I_{OM}$	I_{ABC} = 15 μA	−140	−140	−140	−98	−98	−98	mA

Groups C and D Electrical Characteristics Sampling Tests (T_A = 25°C)

Characteristic	Symbol	TEST CONDITIONS V^+ = 30 V, I_{ABC} = 100 μA Unless Otherwise Specified	LIMITS Min	LIMITS Max	Units
Input Offset Voltage	V_{IO}		–	0.6	V
Input Offset Current	I_{IO}		–	0.25	μA
Forward Transconductance to Terminal No. 1	g_m		1420	3350	μmho
Peak Output Voltage (Terminal No.6) with Q_{13} "ON"	$+V_{OM}$	R_L = 2 kΩ to ground	25	–	V
Supply Current	I^+_{Supply}		–	400	μA
Output Leakage Current Q_{13} "OFF"	$-I_{OL}$	V^+ = 25 V	–15	–	μA
Max. Output Current Q_{13} "ON"	$-I_{OM}$	I_{ABC} = 3 μA	–	–45	mA

CA3100/...

High-Reliability Wideband Operational Amplifiers

For Applications in Aerospace, Military, and Critical Industrial Equipment

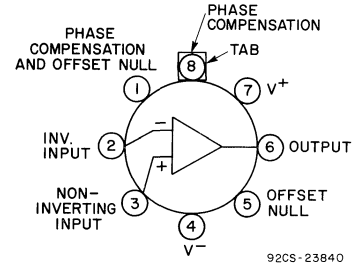
Features:

- **High unity-gain crossover frequency (f_T) – 38 MHz typ.**
- **Wide power Bandwidth – V_O = 18 V p-p typ. at 1.2 MHz**
- **High slew rate – 70 V/μs (typ.) in 20 dB amplifier**
  25 V/μs (typ.) in unity-gain amplifier
- **Fast settling time – 0.6 μs typ.**
- **High open-loop gain at video frequencies –**
  42 dB typ. at 1 MHz
- **High output current – ±15 mA min.**
- **LM118, 748/LM101 pin compatibility**
- **Single capacitor compensation**
- **Offset null terminals**

Applications:

- **Video amplifiers**
- **Fast peak detectors**
- **Meter-driver amplifiers**
- **Video pre-drivers**
- **Oscillators**
- **Multivibrators**
- **High-frequency feedback amplifiers**

The CA3100 is supplied in the standard 8-lead TO-5 package (T suffix), the 8-lead TO-5 dual-in-line formed-lead "DIL-CAN" package (S suffix), or in chip form (H suffix).



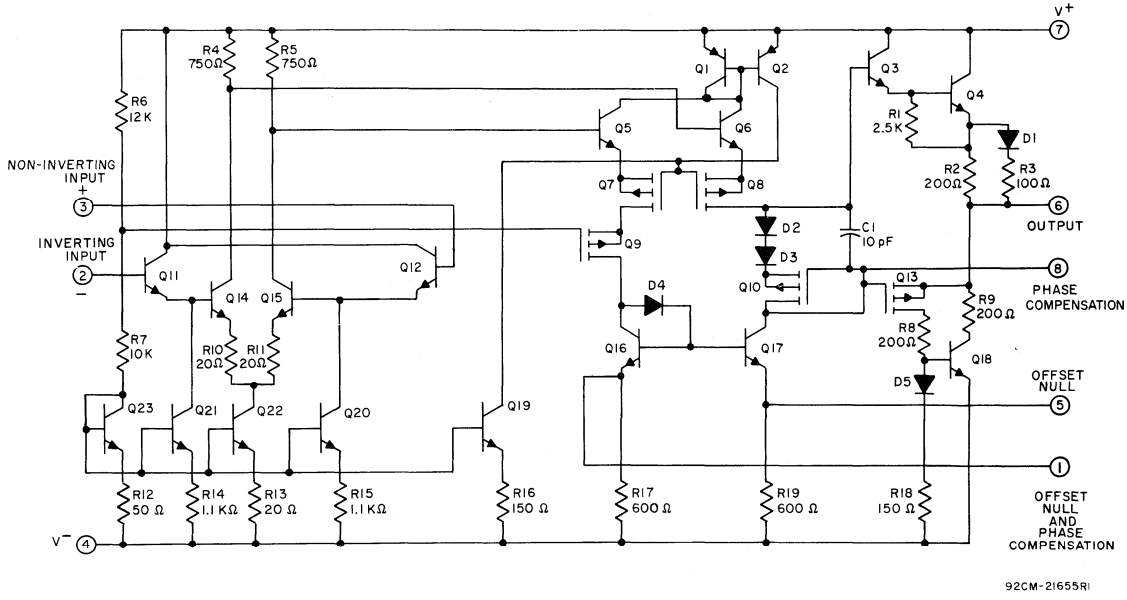
Functional diagram of CA3100S, CA3100T.

Maximum Ratings, Absolute-Maximum Values at T_A = 25°C

Supply Voltage (between V^+ and V^- terminals)	36	V
Differential Input Voltage	±12	V
Input Voltage to Ground*	±15	V
Offset Terminal to V^- Terminal Voltage	±0.5	V
Output Current	50	mA•
Device Dissipation:		
Up to T_A = 55°C	630	mW
Above T_A = 55°C Derate Linearly at	6.67	mW/°C
Ambient Temperature Range:		
Operating		-55 to +125°C
Storage		-65 to +125°C
Lead Temperature (During Soldering):		
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max.	265	°C

** If supply voltage is less than ±15 volts, the maximum input voltage to ground is equal to the supply voltage*

• CA3100S, CA3100T does not contain circuitry to protect against short circuits in the output.



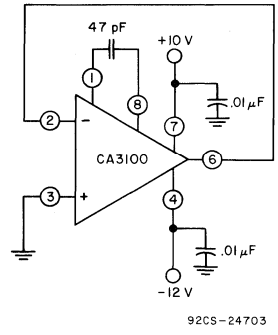
Schematic diagram for CA3100.

Table I. Pre Burn-in Electrical and Post Burn-in Electrical Tests, and Delta Limits.●

ELECTRICAL CHARACTERISTICS, *at T_A = 25°C, V^+ = 15V, V^- = −15V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX.Δ	
Input Offset Voltage	V_{IO}	V_O = 0 ±0.1 V	–	5	±1	mV
Input Offset Current	I_{IO}	V_O = 0 ±1V	–	400	±40	nA
Input Bias Current	I_{IB}	V_O = 0 ±1V	–	2	±0.5	μA
Supply Current	I^+	V_O = 0 ±1V	–	10.5	±1.5	mA

● Level /1 requires pre burn-in electrical and post burn-in electrical tests and delta limits.
Level /3 requires final electrical test only, after burn-in. The burn-in and operating life test circuit is shown below.



Burn-in and operating life-test circuit.

CA3100/...

Table II. Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS SUPPLY VOLTAGE (V^+,V^-)=15V UNLESS OTHERWISE SPECIFIED	LIMITS MINIMUM –55	+25	+125	MAXIMUM –55	+25	+125	UNITS
STATIC									
Input Offset Voltage	V_{IO}	V_O = 0 ±0.1 V	–	–	–	6	5	6	mV
Input Bias Current	I_{IB}	V_O = 0 ±1 V	–	–	–	4	2	2	μA
Input Offset Current	I_{IO}		–	–	–	1000	400	600	nA
Low-Frequency Open-Loop Voltage Gain●	A_{OL}	V_O = ±1 V Peak	50	56	50	–	–	–	dB
Common-Mode Input Voltage Range	V_{ICR}	CMRR ⩾ 76 dB	–	±12	–	–	–	–	V
Common-Mode Rejection Radio	CMRR	V_I Common Mode = ±12 V	–	76	–	–	–	–	dB
Maximum Output Voltage Positive	V_{OM}^+	Differential Input Voltage =0 ± 0.1V	+9	+9	+9	–	–	–	V
Negative	V_{OM}^-	R_L = 2 KΩ	–9	–9	–9	–	–	–	
Maximum Output Current Positive	I_{OM}^+	Differential Input Voltage = 0 ±0.1V	+15	+15	+12	–	–	–	mA
Negative	I_{OM}^-	R_L = 500 Ω	–15	–15	–12	–	–	–	
Supply Current	I^+	V_O = 0 ±0.1 V, R_L ⩾ 10 KΩ	–	–	–	10.5	10.5	—	mA
Power Supply Rejection Ratio	PSRR	ΔV^+ = ±1 V, ΔV^- = ±1 V	60	60	60	–	–	–	dB
DYNAMIC									
Output Voltage Swing	V_O(p-p)	f=2 MHz, V_I=370 mV (p-p)	–	11	–	–	–	–	V (p-p)

● Low-frequency dynamic characteristic

Groups C and D Electrical Characteristics Sampling Tests

T_A = +25°C V^+ = +15 V V^- = –15 V

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS MIN.	MAX.	UNITS
Input Offset Voltage	V_{IO}	V_O = 0 ±0.1 V	–	5	mV
Input Offset Current	I_{IO}	V_O = 0 ±0.1 V	–	400	nA
Input Bias Current	I_I	V_O = 0 ±0.1 V	–	2	μA
Large-Signal Voltage Gain	A_{OL}	V_O = ±1V Peak	56	–	dB
Supply Current	I^+	V_O = 0 ±0.1 V	–	10.5	mA

High-Reliability High-Voltage Transistor Arrays

For Applications in Aerospace, Military, and Critical Industrial Equipment

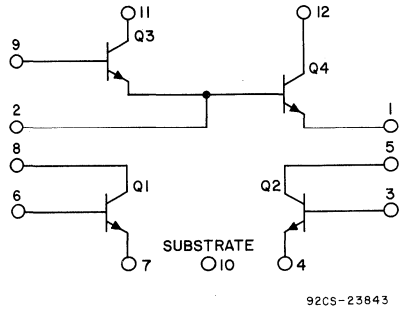
Features:

- **Matched general-purpose transistors**
- **V_{BE} matched ±5 mV max.**
- **Operation from DC to 120 MHz (CA3118AT, T).**
- **Low-noise figure: 3.2 dB typ. at 1 kHz (CA3118AT, T).**

Applications:

- **General use in signal processing systems in DC through VHF range**
- **Custom designed differential amplifiers**
- **Temperature compensated amplifiers**

Types CA3118AT and CA3118T consist of four transistors with two of the transistors connected in a Darlington configuration. These types are well suited for a wide variety of applications in low-power systems in the DC through VHF range. Both types are supplied in a hermetically sealed 12-lead TO-5 type package, ("T" suffix), and in chip form ("H" suffix), and operate over the full military temperature range. (CA3118AT and CA3118T are high-voltage versions of the popular predecessor type CA3018.)



CA3118AT, CA3118T

Schematic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

POWER DISSIPATION:		
Any one transistor —		
CA3118AT, CA3118T	300	mW
Total package —		
Up to 85°C (CA3118AT, CA3118T)	450	mW
Above 85°C (CA3118AT, CA3118T)	derate linearly 5	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating —		
CA3118AT, CA3118T	−55 to +125	°C
Storage (all types)	−65 to +150	°C
THE FOLLOWING RATINGS APPLY FOR EACH TRANSISTOR IN THE DEVICE:		
Collector-to-Emitter Voltage (V_{CEO}):		
CA3118AT	40	V
CA3118T	30	V
Collector-to-Base Voltage (V_{CBO}):		
CA3118AT	50	V
CA3118T	40	V
Collector-to-Substrate Voltage (V_{CIO}):■		
CA3118AT	50	V
CA3118T	40	V
EMITTER-TO-BASE VOLTAGE (V_{EBO}) all types	5	V
Collector Current —		
CA3118AT, CA3118T	50	mA

■The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

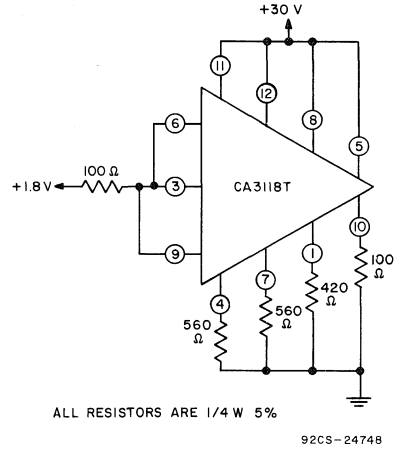
CA3118/..., CA3118A/...

Pre Burn-In Electrical and Post Burn-In Electrical Tests and Delta Limits*

ELECTRICAL CHARACTERISTICS, *at* $T_A = 25^oC$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX△	
Emitter-to-Base Breakdown Volts Q1, Q2	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	–	±0.5	V
Collector Cutoff Current Q1, Q2	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	5	±1	μA
Collector Cutoff Current Q3, Q4	$I_{CEO(D)}$	V_{CE} = 10 V, I_B = 0	–	5	±1	μA
Input Current Q1, Q2	I_I	I_C = 1 mA, V_{CE} = 5 V	–	33	±3	μA
Input Current Q3, Q4	$I_{I(D)}$	I_C = 1 mA, V_{CE} = 5 V	–	0.66	±0.1	μA
Base to Emitter Voltage Q1, Q2	V_{BE}	I_E = 1 mA, V_{CE} = 3 V	0.63	0.83	±0.1	V

* Level /1 requires pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown below.



Burn-in and operating life test circuit.

Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS NOTE – Unless otherwise specified, limits apply to both CA3118 and CA3118A		LIMITS MINIMUM -55	LIMITS MINIMUM +25	LIMITS MINIMUM +125	LIMITS MAXIMUM -55	LIMITS MAXIMUM +25	LIMITS MAXIMUM +125	UNITS
For Each Transistor:										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	CA3118	–	40	–	–	–	–	V
			CA3118A	–	50	–	–	–	–	
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	CA3118	–	30	–	–	–	–	V
			CA3118A	–	40	–	–	–	–	
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 10 μA, I_B = 0, I_E = 0	CA3118	–	40	–	–	–	–	V
			CA3118A	–	50	–	–	–	–	
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0		–	5	–	–	–	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	–	–	5	100	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		–	–	–	–	100	–	mA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 5 V, I_C = 1 mA		15	30	40	–	–	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 1 mA		.7	0.63	0.43	1.3	0.83	0.73	V
For transistors Q3 and Q4 (Darlington Configuration):										
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	–	–	5	2000	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 5 V, I_C = 1 mA		750	1500	2000	–	–	–	
For transistors Q1 and Q2 (As a Differential Amplifier):										
Magnitude of Input Offset Voltage $\lvert V_{BE1} - V_{BE2} \rvert$	$\lvert V_{IO} \rvert$	V_{CE} = 5 V, I_E = 1 mA		–	–	–	–	5	–	mV
Magnitude of h_{FE}		V_{CE} = 5 V, $I_{C1} = I_{C2}$ = 1 mA		–	0.9	–		1.1	–	

Groups C and D Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Emitter-to-Base Breakdown Volts, Q_1, Q_2, Q_3, Q_4	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	4	–	V
Collector-to-Emitter Breakdown Volts, Q_1, Q_2, Q_3, Q_4	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	28	–	V
Input Current, Q_1, Q_2	I_{IN}	I_C = 1 mA, V_{CE} = 5V	–	50	μA
Input Current, Darlington Pair, Q_3, Q_4	$I_{IN(D)}$	I_C = 1 mA, V_{CE} = 5V	–	1	μA
Base-to-Emitter Voltage, Q_1, Q_2	V_{BE}	I_E = 1 mA, V_{CE} = 3V	0.63	0.83	V

CA3130/..., CA3130A/...

High-Reliability BiMOS Operational Amplifiers

With MOSFET Input, CMOS Output
For Aerospace, Military, and Critical Industrial Applications

Features:

- *MOSFET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 x 10^{12} Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  = 2 pA typ. at 5 V operation
- *Common-mode input-voltage range includes negative supply rail, input terminals can be swung 0.5 V below negative supply rail*
- *CMOS output stage permits signal swing to either (or both) supply rails*

Ideal for single-supply applications

- *Wide BW: 15 MHz typ. (unity-gain crossover)*
- *High SR: 10 V/μs typ. (unity-gain follower)*
- *High output current (I_O): 20 mA typ.*
- *High A_{OL}: 320,000 (110 dB) typ.*
- *Compensation with single external capacitor*

Applications:

- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *High-input-impedance comparators (ideal interface with digital CMOS)*
- *High-input-impedance wideband amplifiers*
- *Voltage followers (e.g., follower for single-supply D/A converter)*
- *Voltage regulators (permits control of output voltage down to zero volts)*
- *Peak detectors*
- *Single-supply full-wave precision rectifiers*
- *Photo-diode sensor amplifiers*

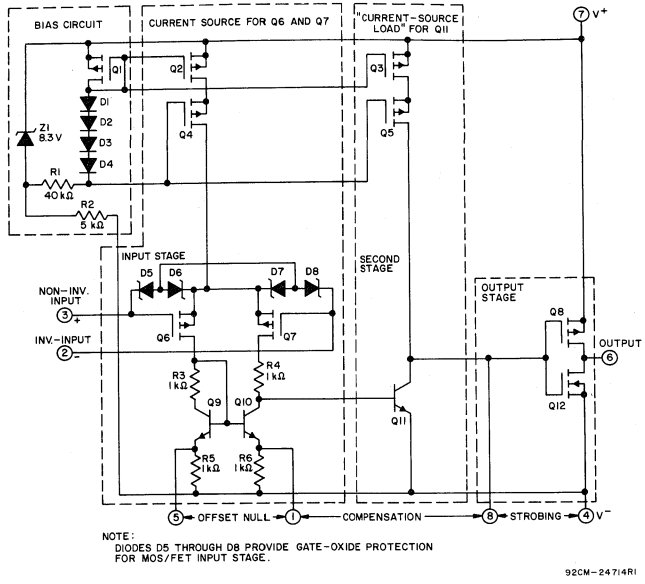
The CA3130 and CA3130A Slash (/) Series types are supplied in the 8-lead TO-5 style package ("T" suffix), in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values*

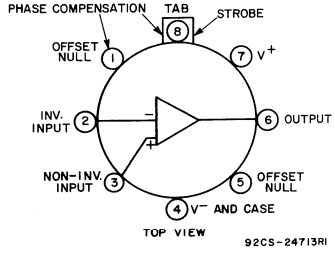
DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE ..... V^+ to (V^- -0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
Without Heat Sink -
Up to 55°C ..... 630 mW
Above 55°C ..... Derate linearly 6.67 mW/°C
With Heat Sink -
Up to 90°C ..... 4 W
Above 90°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
Operating ..... -55 to +125°C
Storage ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT
DURATION* ..... INDEFINITE
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

* Short circuit may be applied to ground or to either supply.

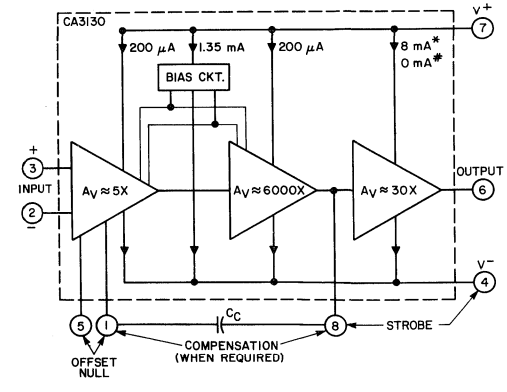
CA3130/..., CA3130A/...



Schematic diagram of the CA3130 Series.



Functional diagram of the CA3130 Series.



Block diagram of the CA3130 Series.

CA3130/..., CA3130A/...

Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+=+15 V, V^-= 0 V Unless Otherwise Specified	LIMITS						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
Input Offset Voltage:									
CA3130	V_{IO}	$V^{\pm}$ = ±7.5 V	–	–	–	40	25	40	mV
CA3130A			–	–	–	20	12	20	
Input Offset Current:									
CA3130	I_{IO}	$V^{\pm}$ = ±7.5 V	–	–	–	500	30	5000	pA
CA3130A			–	–	–	300	20	3000	
Input Current:									
CA3130	I_I	$V^{\pm}$ = ±7.5 V	–	–	–	50	0.05	50	nA
CA3130A			–	–	–	40	0.03	40	
Large Signal Voltage Gain:									
CA3130	A_{OL}	V_O = 8 V_{p-p} (–55, +125°C)	86	94	86	–	–	–	dB
CA3130A		V_O = 10 V_{p-p} (25°C)	88	94	88	–	–	–	
Common-Mode Rejection Ratio:									
CA3130	CMRR		64	70	64	–	–	–	dB
CA3130A			74	80	74	–	–	–	
Common-Mode Input Voltage Range	V_{ICR}		0	0	0	10	10	10	V
Power Supply Rejection Ratio:									
CA3130	PSRR	$V^{\pm}$ = ± 7.5 V	–	–	–	400	320	400	μV/V
CA3130A			–	–	–	200	150	200	
Maximum Output Voltage	V_{OM}^+	R_L = 2 kΩ	10	12	10	–	–	–	V
	V_{OM}^-		–	–	–	0.05	0.01	0.05	
Maximum Output Voltage	V_{OM}^+	R_L = ∞	14.95	14.99	14.95	–	–	–	V
	V_{OM}^-		–	–	–	0.05	0.01	0.05	
Maximum Output Current	I_{OM}^+	V_O = 0 V	–	12	–	–	45	–	mA
	I_{OM}^-	V_O = 15 V	–	12	–	–	45	–	
Supply Current	I^+	V_O = 7.5V, R_L=∞	–	–	–	–	15	–	mA
		V_O = 0V, R_L=∞	–	–	–	–	3	–	

Group C Electrical Characteristics Sampling Tests at T_A = 25°C, V^+ = +15 V, V^- = −15 V

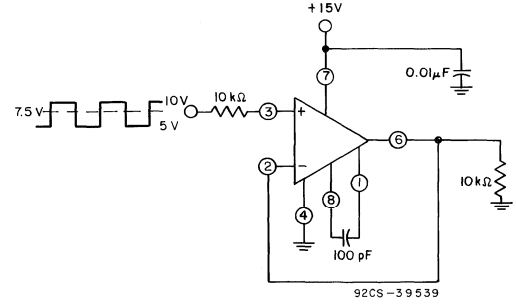
CHARACTERISTIC		SYMBOL	LIMITS		UNITS
			MIN.	MAX.	
Input Offset Voltage	CA3130	V_{IO}	–	25	mV
	CA3130A		–	12	
Input Offset Current	CA3130	I_{IO}	–	30	pA
	CA3130A		–	20	
Input Current	CA3130	I_I	–	50	pA
	CA3130A		–	30	
Large Signal Voltage Gain	CA3130	A_{OL}	91	–	dB
	CA3130A		91	–	

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = +7.5 V, V^- = −7.5 V

CHARACTERISTIC		SYMBOL	LIMITS		UNITS
			MAX.	MAX.Δ	
Input Offset Voltage	CA3130	V_{IO}	15	±8	mV
	CA3130A		5	±3	
Input Offset Current	CA3130	I_{IO}	30	±15	pA
	CA3130A		20	±8	
Input Current	CA3130	I_I	50	±10	pA
	CA3130A		30	±10	

* Level /1 requires pre-burn-in electrical and post burn-in electrical tests, and delta limits. Level /3 requires final electrical test only. The burn-in and operating life test circuit is shown below.



Burn-In and Life Test Circuit.

CA3140/..., CA3140A/...

High-Reliability BiMOS Operational Amplifiers

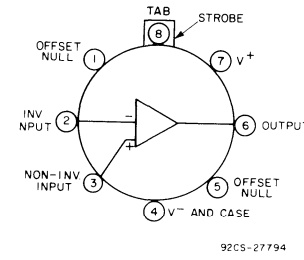
With MOSFET Input, Bipolar Output
For Aerospace, Military, and Critical Industrial Applications

Features:

- **MOSFET Input Stage**
  - (a) Very high input impedance (Z_{IN}) – 1.5 TΩ typ.
  - (b) Very low input current (I_I) – 10 pA typ. at ± 15 V
  - (c) Low input-offset voltage (V_{IO}) – to 2 mV max.
  - (d) Wide common-mode input-voltage range (V_{ICR}) – can be swung 0.5 volt below negative supply-voltage rail
  - (e) Output swing complements input common-mode range
  - (f) Rugged input stage – bipolar diode protected
- Directly replaces industry type 741 in most applications
- Includes numerous industry operational amplifier categories such as general-purpose, FET input, wideband (high slew rate)
- Operation from 4-to-44 volts Single or Dual supplies
- Internally compensated
- Characterized for ± 15-volt operation and for TTL supply systems with operation down to 4 volts
- Wide bandwidth – 4.5 MHz unity gain at ± 15 V or 30 V; 3.7 MHz at 5 V
- High voltage-follower slew rate – 9 V/μs
- Fast settling time – 1.4 μs typ. to 10 mV with a 10-V_{p-p} signal
- Output swings to within 0.2 volt of negative supply
- Strobable output stage

Applications:

- Ground-referenced single-supply amplifiers in automobile and portable instrumentation
- Sample and hold amplifiers
- Long-duration timers/multivibrators (microseconds–minutes–hours)
- Photocurrent instrumentation
- Peak detectors
- Active filters
- Comparators
- Portable instruments
- Interface in 5 V TTL systems & other low-supply voltage systems
- All standard operational amplifier applications
- Function generators
- Tone controls
- Power supplies
- Intrusion alarm systems



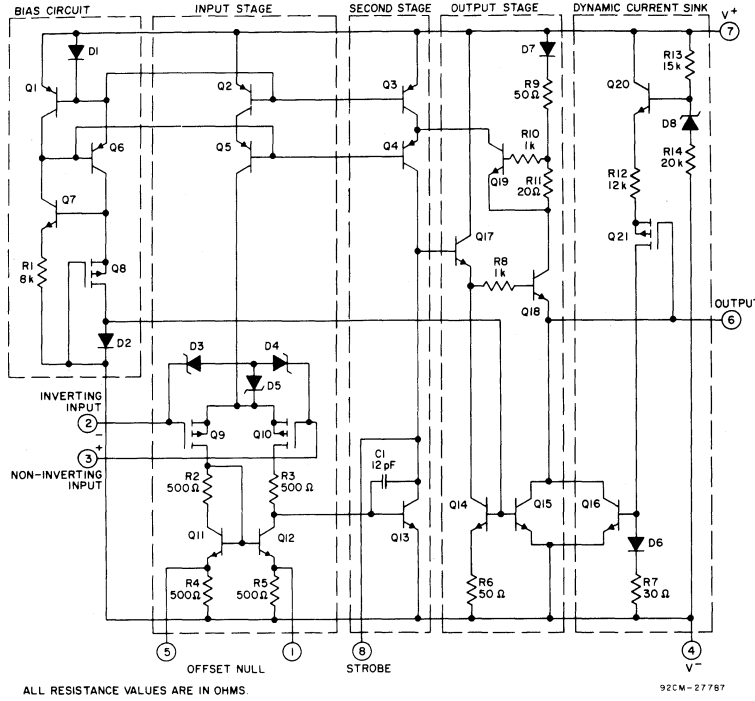
Functional diagram of the CA3140 series.

The CA3140 and CA3140A Slash (/) Series types are supplied in the 8-lead TO-5 style package ("T" suffix), in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) ..... 36 V
DIFFERENTAIL-MODE INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8 V) to (V^- -0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate linearly 6.67 mW/°C
TEMPERATURE RANGE:
OPERATING ..... -55 to +125°C
STORAGE ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX. ..... +265°C

*Short circuit may be applied to ground or either supply.

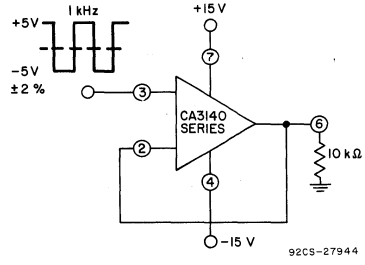


Schematic diagram of CA3140 series.

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT T_A = 25°C V^+ = +15 V, V^- = −15 V		LIMITS Max	LIMITS ΔMax	UNITS
Input Offset Voltage	V_{IO}		CA3140A	5	±1	mV
			CA3140	15	±2	
Input Offset Current	I_{IO}		CA3140A	20	±4	pA
			CA3140	30	±6	
Input Bias Current	I_I		CA3140A	40	±10	pA
			CA3140	50	±10	

* Level /1 requires pre burn-in electrical and post burn-in electrical tests and delta limits. Level /3 requires pre burn-in electrical tests only. The burn-in and operating life-test circuit is shown below.



Burn-in and operating life-test circuit.

CA3140/..., CA3140A/...

FINAL ELECTRICAL TESTS AND GROUP A SAMPLING INSPECTION

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+,=15 V, V^-=15 V Unless Otherwise Specified	LIMITS MINIMUM -55	MINIMUM +25	MINIMUM +125	MAXIMUM -55	MAXIMUM +25	MAXIMUM +125	UNITS
Input Offset Voltage:									
CA3140A	$\lvert V_{IO}\rvert$		—	—	—	20	12	20	mV
CA3140			—	—	—	40	25	40	
Input Offset Current:									
CA3140A	$\lvert I_{IO}\rvert$		—	—	—	4	0.02	4	nA
CA3140			—	—	—	5	0.03	5	
Input Current:									
CA3140A	$\lvert I_I\rvert$	V_O = 26 V_{p-p}	—	—	—	7	0.04	40	nA
CA3140		(+12 V, -14 V)	—	—	—	8	0.05	50	
Large Signal Voltage Gain:									
CA3140A	A_{OL}	V_O = 26 V_{p-p} (+ 12 V, -14 V)	80	86	80	—	—	—	dB
CA3140		R_L = 2 kΩ	80	86	80	—	—	—	
Common-Mode Rejection Ratio:									
CA3140A	CMRR		64	70	64	—	—	—	dB
CA3140			64	70	64	—	—	—	
Common-Mode Input Voltage Range:									
CA3140A	V_{ICR}		-15	-15	-15	+11	+12	+12	V
CA3140			-15	-15	-15	+10	+11	+11	
Power Supply Rejection Ratio:									
CA3140A	PSRR		72	76	72	—	—	—	dB
CA3140			72	76	72	—	—	—	
Maximum Output Voltage (All Types)	V_{OM}^+ V_{OM}^-	R_L = 2 kΩ	+11 -14	+12 -14	+12 -14	—	—	—	V
Supply Current	I^+		—	—	—	7	6	6	mA

Group C Electrical Characteristics Sampling Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT T_A = 25°C V^+ = +15 V, V^- = −15 V		LIMITS Min	LIMITS Max	UNITS
Input Offset Voltage	V_{IO}		CA3140A	–	12	mV
			CA3140	–	25	
Input Offset Current	I_{IO}		CA3140A	–	20	pA
			CA3140	–	30	
Input Bias Current	I_I		CA3140A	–	40	pA
			CA3140	–	50	
Large Signal Voltage Gain	A_{OL}		CA3140A	86	–	dB
			CA3140	86	–	

High-Reliability BiMOS Operational Amplifiers

With MOSFET Input, CMOS Output

Features:

- Similar to CA3130 but has internal compensation
- MOSFET input stage provides:
  very high Z_I = 1.5 TΩ (1.5 x 10^{12} Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  2 pA typ. at 5 V operation
- Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
- CMOS output stage permits signal swing to either (or both) supply rails

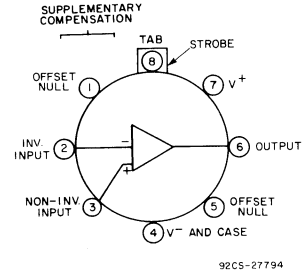
} Ideal for single-supply applications

- Wide BW: 4 MHz typ. (unity-gain crossover)
- High SR: 10 V/μs typ. (unity-gain follower)
- High output current (I_O): 20 mA typ.
- High A_{OL}: 320,000 (110 dB) typ.
- Internal phase compensation for unity gain (With terminal access for supplementary external phase compensation network if desired)

The CA3160 and CA3160A Slash (/) Series types are supplied in the 8-lead TO-5 style package ("T" suffix).

Applications:

- Ground-referenced single-supply amplifiers
- Fast sample-hold amplifiers
- Long-duration timers/monostables
- Ideal interface with digital CMOS
- High-input-impedance wideband amplifiers
- Voltage followers
  (e.g., follower for single-supply D/A converter)
- Voltage regulators
  (permits control of output voltage down to zero volts)
- Wien-Bridge oscillators
- Voltage-controlled oscillators
- Photo-diode sensor amplifiers



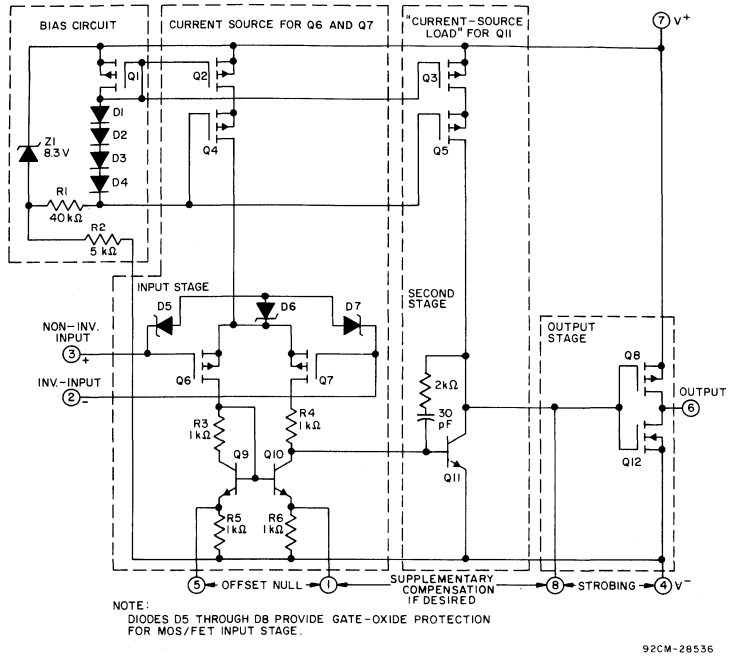
Functional diagram of the CA3160 Series.

MAXIMUM RATINGS, *Absolute-Maximum Values*

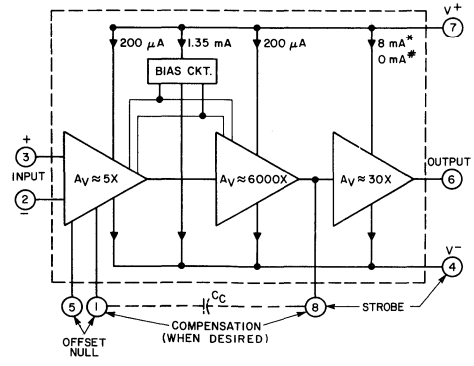
DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE ..... V^+ to (V^- -0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
Without Heat Sink -
Up to 55°C ..... 630 mW
Above 55°C ..... Derate linearly 6.67 mW/°C
With Heat Sink -
Up to 55°C ..... 418 mW
Above 55°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
Operating ..... -55 to + 125°C
Storage ..... -65 to + 150°C
OUTPUT SHORT-CIRCUIT
DURATION* ..... INDEFINITE
LEAD TEMPERATURE (During Soldering):
At Distance 1/16 ± 1/32 inch (1.59 ± 0.79 MM) from case for 10 seconds max. ..... +265°C

* Short circuit may be applied to ground or to either supply.

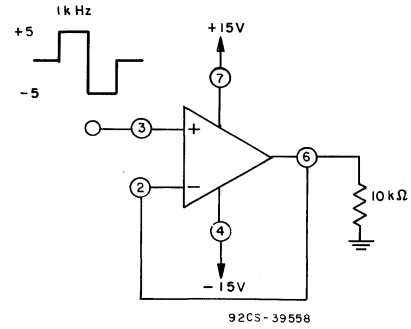
CA3160/..., CA3160A/...



Schematic diagram of the CA3160 Series.



Block diagram of the CA3160 Series.



Burn-in and life test circuit.

CA3160/..., CA3160A/...

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = +7.5 V, V^- = –7.5 V

CHARACTERISTIC		SYMBOL	LIMITS		UNITS
			MAX.	MAX.Δ	
Input Offset Voltage	CA3160	V_{IO}	15	±8	mV
	CA3160A		5	±3	
Input Offset Current	CA3160	I_{IO}	30	±15	pA
	CA3160A		20	±8	
Input Current	CA3160	I_I	50	±10	pA
	CA3160A		30	±10	

* Level /1 requires pre-burn-in electrical and post burn-in electrical tests, and delta limits. Level /3 requires final electrical test only after burn-in. The burn-in and operating life test circuit is shown on the previous page.

FINAL ELECTRICAL TESTS AND GROUP A SAMPLING INSPECTION

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+=+15 V, V^-= 0 V Unless Otherwise Specified	LIMITS						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
Input Offset Voltage:									
CA3160	V_{IO}	$V^{\pm}$ = ±7.5 V	–	–	–	40	25	40	mV
CA3160A			–	–	–	20	12	20	
Input Offset Current:									
CA3160	I_{IO}	$V^{\pm}$ = ±7.5 V	–	–	–	500	30	5000	pA
CA3160A			–	–	–	300	20	3000	
Input Current:									
CA3160	I_I	$V^{\pm}$ = ±7.5 V	–	–	–	50	0.05	50	nA
CA3160A			–	–	–	40	0.03	40	
Large Signal Voltage Gain:									
CA3160	A_{OL}	V_O = 10 V_{p-p}	86	94	86	–	–	–	dB
CA3160A			88	94	88	–	–	–	
Common-Mode Rejection Ratio:									
CA3160	CMRR		64	70	64	–	–	–	dB
CA3160A			74	80	74	–	–	–	
Common-Mode Input Voltage Range	V_{ICR}		0	0	0	10	10	10	V
Power Supply Rejection Ratio:									
CA3160	PSRR	$V^{\pm}$ = ± 7.5 V	–	–	–	400	320	400	μV/V
CA3160A			–	–	–	200	150	200	
Maximum Output Voltage	V_{OM}^+	R_L = 2 kΩ	10	12	12	–	–	–	V
	V_{OM}^-		–	–	–	0.05	0.01	0.05	
Maximum Output Voltage	V_{OM}^+	R_L = ∞	14.95	14.99	14.95	–	–	–	V
	V_{OM}^-		–	–	–	0.05	0.01	0.05	
Maximum Output Current	I_{OM}^+	V_O = 0 V	–	12	–	–	45	–	mA
	I_{OM}^-	V_O = 15 V	–	12	–	–	45	–	
Supply Current	I^+	V_O = 7.5V, R_L=∞	–	–	–	–	15	–	mA
		V_O = 0V, R_L=∞	–	–	–	–	3	–	

CA3160/..., CA3160A/...

Group C Electrical Characteristics Sampling Tests at $T_A = 25^oC$, $V^+ = +15\ V$, $V^- = -15\ V$

CHARACTERISTIC		SYMBOL	LIMITS		UNITS
			MIN.	MAX.	
Input Offset Voltage	CA3160	V_{IO}	–	25	mV
	CA3160A		–	12	
Input Offset Current	CA3160	I_{IO}	–	30	pA
	CA3160A		–	20	
Input Current	CA3160	I_I	–	50	pA
	CA3160A		–	30	
Large Signal Voltage Gain	CA3160	A_{OL}	91	–	dB
	CA3160A		91	–	

High-Reliability Slash (/) Series BiMOS Precision Operational Amplifiers

Features:
- *Low V_{IO}:*
  200 μV max. (CA3193A/...)
  500 μV max. (CA3193/...)
- *Low $\Delta V_{IO}/\Delta T$:*
  3 μV/°C max. (CA3193A/...)
  5 μV/°C max. (CA3193/...)
- *Low I_{IO} and I_I*
- *Low $\Delta I_{IO}/\Delta T$:*
  150 pA/°C max. (CA3193/...)
- *Low $\Delta I_I/\Delta T$: 3.7 nA/°C max. (CA3193/...)*
- *Extremely high gain:*
  110 dB min. (CA3193A/...)
  100 dB min. (CA3193/...)
- *Low V_{IO} vs. time*
- *High CMRR and PSRR*
- *Internally compensated:*
  1.2-MHz bandwidth product
- *Low input noise: 0.1 Hz to 10 Hz*
  Noise voltage: 0.36 μV_{p-p} typ.
  Noise current: 12 pA_{p-p} typ.

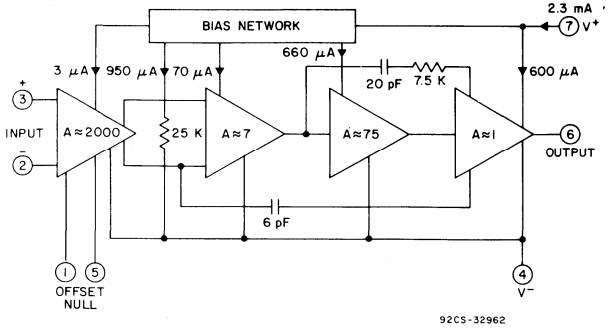
Applications:
- *Thermocouple preamplifiers*
- *Strain-gauge bridge amplifiers*
- *Summing amplifiers*
- *Differential amplifiers*
- *Bilateral current sources*
- *Log amplifiers*
- *Differential voltmeters*
- *Precision voltage references*
- *Active filters*
- *Buffers*
- *Integrators*
- *Sample-and-hold circuits*
- *Low frequency filters*

The CA3193/... and CA3193A/... series types are supplied in an 8-lead TO-5-style package with dual-in-line formed leads, DIL-CAN (S suffix) and in an 8-lead TO-5-style package (T suffix). These types are also available in chip form (H suffix).

ABSOLUTE-MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C*

DC SUPPLY VOLTAGE	±18 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±5 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ -4), V^- V
INPUT TERMINAL CURRENT	1 mA
DEVICE DISSIPATION WITHOUT HEAT SINK	
Up to 55°C	630 mW
Above 55°C	Derate Linearly 6.67 mW/°C
TEMPERATURE RANGE	-55°C to +125°C
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite
LEAD TEMPERATURE (DURING SOLDERING)	
At a distance of 1/16 in. ± 1/32 in. (1.59 mm ± 0.79 mm) from case for 10 s max.	±265°C

*Short circuit may be applied to ground or to either supply.



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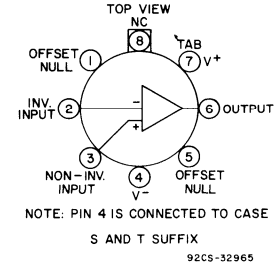
Block diagram of CA3193/... and CA3193A/...



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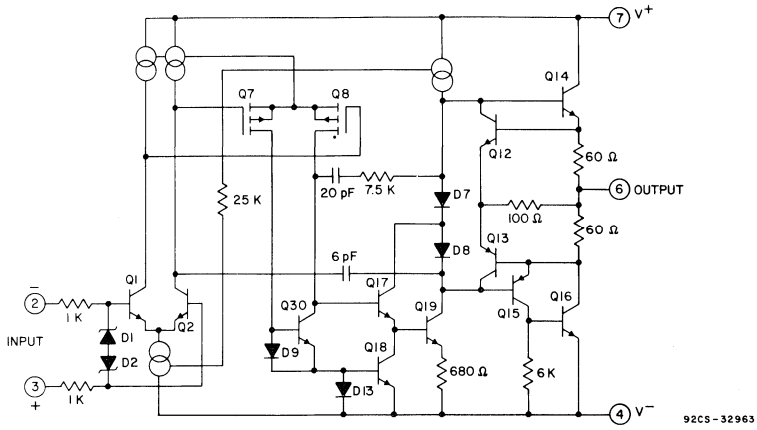
Functional diagram of CA3193/... and CA3193A/...

CA3193/..., CA3193A/...

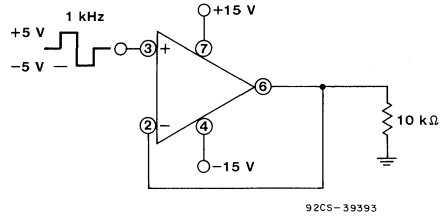


Simplified schematic diagram of CA3193/... and CA3193A/...

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*
ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = +15 V, V^- = −15 V

CHARACTERISTIC		SYMBOL	LIMITS		UNITS
			MAX.	MAX.Δ	
Input Offset Voltage	CA3193/...	V_{IO}	500	120	μV
	CA3193A/...		200	20	
Input Offset Current	CA3193/...	I_{IO}	10	2	nA
	CA3193A/...		5	2	
Input Current	CA3193/...	I_I	40	10	nA
	CA3193A/...		20	5	

*Level /1 requires pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires final electrical test only, after burn-in.
The burn-in and operating life test circuit is shown below.



Burn-in and life test circuit.

Electrical Test Requirements

Test Requirement	Group A Subgroups
Interim Electrical Parameters (pre burn-in)	1
Final Electrical Test Parameters (Method 5005, MIL-STD-883)	1*, 2, 3
Group C and D End-Point Parameters	1

*PDA applies to Subgroup 1.

CA3193/..., CA3193A/...

Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+=+15 V, V^-=-15 V Unless Otherwise Specified	LIMITS						UNITS
			MIMIMUM			MAXIMUM			
			-55° C	+25° C	+125° C	-55° C	+25° C	+125° C	
Input Offset Voltage:									
CA3193/...	V_{IO}		-725	-500	-725	+725	+500	+725	μV
CA3193A/...			-380	-200	-380	+380	+200	+380	
Input Offset Current:									
CA3193/...	I_{IO}		-20	-10	-20	+20	+10	+20	nA
CA3193A/...			-12	-5	-12	+12	+5	+12	
Input Bias Current:									
CA3193/...	I_I		-210	-40	-210	+210	+40	+210	nA
CA3193A/...			-85	-20	-85	+85	+20	+85	
Common-Mode Input Voltage Range:									
CA3193/...	V_{ICR}		-12	-12	-12	+10	+10	+10	V
CA3193A/...			-12	-12	-12	+10	+10	+10	
Common-Mode Rejection Ratio:									
CA3193/...	CMRR		-20	-10	-20	+20	+10	+20	μV/V
CA3193/...			94	100	94	—	—	—	dB
CA3193A/...			-6.36	-3.16	-6.36	+6.36	+3.16	+6.36	μV/V
CA3193A/...			104	110	104	—	—	—	dB
Common-Mode Input Voltage Range:									
CA3193/...	V_{ICR}	V^+=+18 V, V^-=-18 V	-13	-13	-13	+15	+15	+15	V
CA3193A/...			-13	-13	-13	+15	+15	+15	
Common-Mode Rejection Ratio:									
CA3193/...	CMRR	V^+=+18 V, V^-=-18 V	-20	-10	-20	+20	+10	+20	μV/V
CA3193/...			94	110	94	—	—	—	dB
CA3193A/...			-6.36	-3.16	-6.36	+6.36	+3.16	+6.36	μV/V
CA3193A/...			104	110	104	—	—	—	dB
Maximum Output Voltage Swing:									
CA3193/...	V_{OM}	R_L = 2 kΩ	-13	-13	-13	+13	+13	+13	V
CA3193A/...			-13	-13	-13	+13	+13	+13	
Large-Signal Voltage Gain:									
CA3193/...	A_{OL}	R_L = 2 kΩ	94	100	94	—	—	—	dB
CA3193A/...			104	110	104	—	—	—	
Short-Circuit Output Current to the Opposite Rail:									
CA3193/...	I_{OM}^+, I_{OM}^-		-45	-40	-45	+45	+40	+45	mA
CA3193A/...			-45	-40	-45	+45	+40	+45	
Supply Current:									
CA3193/...	I^+	V^+=+10 V, V^-=-10 V	—	—	—	5	3.5	5	mA
CA3193A/...			—	—	—	5	3.5	5	
Supply Current:									
CA3193/...	I^+		—	—	—	5	3.5	5	mA
CA3193A/...			—	—	—	5	3.5	5	
Supply Current:									
CA3193/...	I^+	V^+=+18 V, V^-=-18 V	—	—	—	6.1	6	6.1	mA
CA3193A/...			—	—	—	6.1	6	6.1	

CA3260/...

High-Reliability Slash (/) Series BiMOS Operational Amplifiers

With MOSFET Input, CMOS Output

Features:

- *Dual version of the CA3160/...*
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *CMOS output stage permits signal swing to either (or both) supply rails*

} *Ideal for single-supply applications*

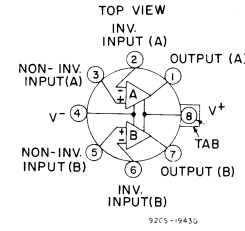
- *MOSFET input stage provides:*
  very high $Z_I = 1.5\ T\Omega$ ($1.5 \times 10^{12}\Omega$) typ.
  very low II = 5 pA typ. at 15-V operation
  = 2 pA typ. at 5-V operation
- *High A_{OL}: 320,000 (110 dB) typ.*
- *Internal phase compensation for unity gain.*
- *Same pin-out as CA1458, CA1558*

APPLICATIONS:

- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *Ideal interface with digital CMOS*
- *High-input-impedance wideband amplifiers*
- *Voltage followers*
  (e.g., follower for single supply D/A converter)
- *Voltage regulators*
  (permits control of output voltage down to zero volts)
- *Wein-Bridge oscillators*
- *Voltage-controlled oscillators*
- *Photo-diode sensor amplifiers*

The CA3260/... series is supplied in standard 8-lead TO-5-style packages (T suffix) and 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" packages (S suffix). The CA3260/... is available in chip form (H suffix).

TERMINAL ASSIGNMENT

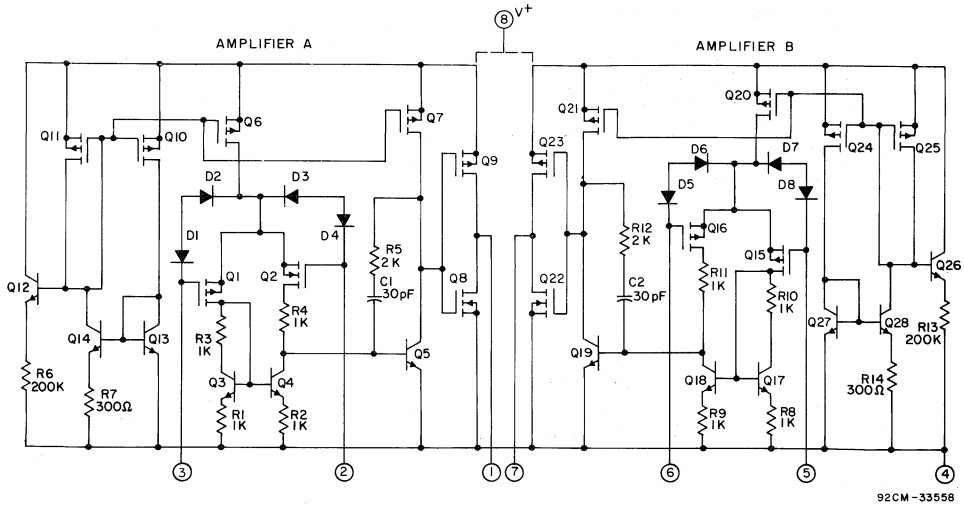


Functional diagram for the CA3260/... series.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8V) to (V^- -0.5 V)
INPUT TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK —
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate lineary 6.67 mW/°C
WITH HEAT SINK —
UP TO 90°C ..... 1 W
ABOVE 90°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE, ALL TYPES:
Operating ..... -55 to +125°C
Storage ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... 265°C

*Short circuit may be applied to ground or to either supply.

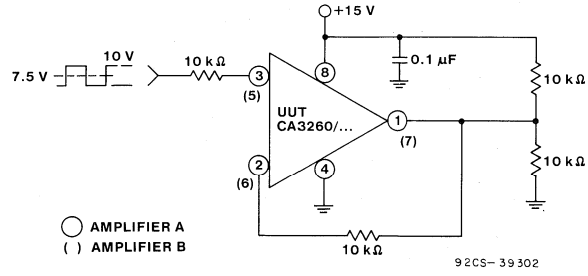


Schematic diagram of CA3260/... series.

Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*
ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = +7.5 V, V^- = -7.5 V

CHARACTERISTIC		SYMBOL	LIMITS		UNITS
			MAX.	MAX.△	
Input Offset Voltage	CA3260/...	V_{IO}	25	±10	mV
	CA3260A/...		12	±8	
Input Offset Current	CA3260/...	I_{IO}	30	±20	pA
	CA3260A/...		20	±10	
Input Current	CA3260/...	I_I	50	±10	pA
	CA3260A/...		30	±10	

*Level /1 require pre-burn-in electrical and post burn-in electrial tests, and delta limits.
Level /3 requires final electrical test only, after burn-in.
The burn-in and operating life test circuit is shown below.



Burn-in and life test circuit (T_A = 125°C).

CA3260/...

Electrical Test Requirements

TEST REQUIREMENT	GROUP A SUBGROUPS
Interim Electrical Parameters (Pre-burn-in)	1
Final Electrical Test Parameters (Method 5005, MIL-STD-883)	1*, 2, 3
Group C and D End Point Parameters	1

*PDA calculated based on Subgroup 1.

Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +15$ V, $V^- = 0$ V Unless Otherwise Specified	LIMITS						UNITS
			MINIMUM			MAXIMUM			
			-55°C	+25°C	+125°C	-55°C	+25°C	+125°C	
Input Offset Voltage: CA3260/...	V_{IO}	$V^{\pm} = \pm 7.5$ V	—	—	—	40	25	40	mv
CA3260A/...			—	—	—	20	12	20	
Input Offset Current: CA3260/...	I_{IO}	$V^{\pm} = \pm 7.5$ V	—	—	—	500	30	5000	pA
CA3260A/...			—	—	—	300	20	3000	
Input Current: CA3260/...	I_I	$V^{\pm} = \pm 7.5$ V	—	—	—	50	0.05	50	nA
CA3260A/...			—	—	—	40	0.03	40	
Large Signal Voltage Gain: CA3260/...	A_{OL}	$V_O = 10$ Vp-p, $R_L = 10K\ \Omega$	22K	50K	22K	—	—	—	V/V
			87	94	87	—	—	—	dB
CA3260A/...			28K	50K	28K	—	—	—	V/V
			89	94	89	—	—	—	dB
Common-Mode Rejection Ratio: CA3260/...	CMRR		64	70	64	—	—	—	dB
CA3260A/...			74	80	74	—	—	—	
Common-Mode Input Voltage Range	V_{ICR}		0	0	0	10	10	10	V
Power Supply Rejection Ratio: CA3260/...	PSRR	$V^{\pm} = \pm 7.5$ V	—	—	—	400	320	400	μV/V
CA3260A/...			—	—	—	200	150	200	
Maximum Output Voltage	V_{OM}^+	$R_L = 10k\ \Omega$	10	11.3	10	—	—	—	V
	V_{OM}^-		—	—	—	0.05	0.01	0.05	
	V_{OM}^+	$R_L = \infty$	14.95	14.99	14.95	—	—	—	
Maximum Output Current	I_{OM}^+	$V_O = 7.5$V	—	12	—	—	45	—	mA
	I_{OM}^-		—	12	—	—	45	—	
Total Supply Current	I^+	$V^{\pm} = \pm 7.5$ V, $R_L = \infty$, $V_{OA} = V_{OB} = 7.5$ V	—	—	—	—	15.5	—	mA
		$V^{\pm} = \pm 7.5$ V, $R_L = \infty$, $V_{OA} = V_{OB} = OV$	—	—	—	—	3	—	
		$V^{\pm} = \pm 7.5$ V, $R_L = \infty$, $V_{OA} = OV$, $V_{OB} = 7.5$V	—	—	—	—	8.5	—	

High-Reliability
BiMOS Dual Voltage Comparator

With MOSFET Input, Bipolar Output

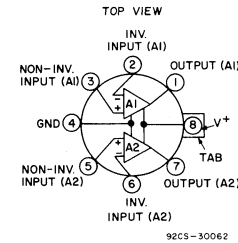
Features:

- *MOSFET input stage:*
  - (a) *Very high input impedance (Z_{IN}): 1.7 TΩ typ.*
  - (b) *Very low input current: 3.5 pA typ. at +5 V supply voltage*
  - (c) *Low input-offset voltage (V_{IO}): to 10 mV max.*
  - (d) *Wide common-mode input-voltage range (V_{ICR}): can be swung 1.5 V (typ.) below negative supply-voltage rail*
  - (e) *MOSFET input stage: zener diode protected*
  - (f) *Virtually eliminates errors due to flow of input currents*
- *Wide supply-voltage range:*
  Single supply: 4 to 36 V dc
  Dual supply: $^{+3.5}_{-0.5}$ to ± 18 V dc
- *Very low supply-current drain: 0.8 mA at +5 V*
- *Differential input-voltage range: up to ± 36 V*
- *Low output saturation voltage: 120 mV at 4 mA*
- *Output voltage compatible with TTL, DTL, ECL, MOS, and CMOS logic systems*
- *Stable V_{IO} vs. time due to source-follower inputs*

Applications:

- *High-source-impedance voltage comparators*
- *Long time delay circuits*
- *Square-wave generators*
- *A/D converters*
- *Window comparators*

TERMINAL ASSIGNMENT



This type is supplied in an 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN (S suffix), and in an 8-lead TO-5 style package (T suffix). The CA3290A/... is also available in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
- Single Supply ..... +36 V
- Dual Supply ..... ±18 V

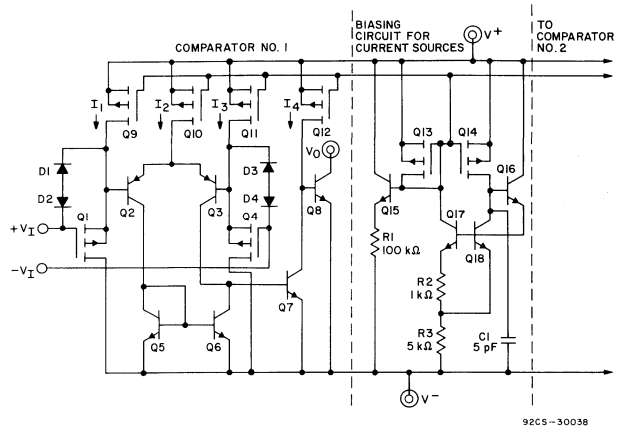
DIFFERENTIAL INPUT VOLTAGE ..... ±36 V or ± [(V^+-V^-)+5 V] (whichever is less)
COMMON-MODE INPUT VOLTAGE ..... V^++5 V to V^- -5 V
DEVICE DISSIPATION:
- Up to 55° C ..... 630 mW
- Above 55° C ..... Derate linearly at 6.67 mW/° C

OUTPUT-TO-V^- SHORT CIRCUIT DURATION* ..... CONTINUOUS
TEMPERATURE RANGE, ALL TYPES:
- Operating ..... -55 to +125° C
- Storage ..... -65 to +150° C

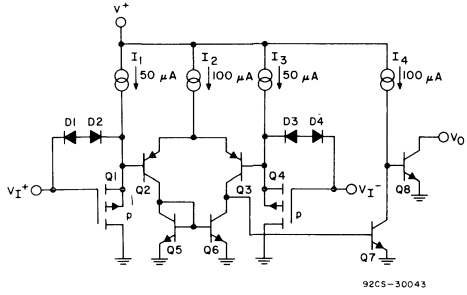
INPUT TERMINAL CURRENT ..... 1 mA
LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... 265° C

* Short circuits from the output to V^+ can cause excessive heating and eventual destruction of the device.

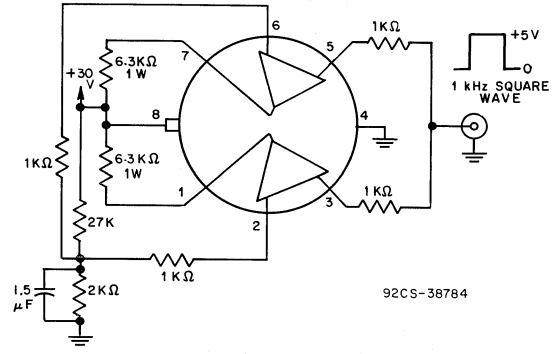
CA3290A/...



Schematic diagram of CA3290A/... (only one is shown).



Basic CA3290A/... comparator.



Burn-in and life test circuit.

Pre-Burn-In Electrical and Post-Burn-In Electrical Tests and Delta Limits at T_A = +25°C

CHARACTERISTIC		LIMITS		UNITS
		MIN.	MAX.Δ	
Input Offset Voltage (15 V)	V_{IO}	10	5	mV
Input Offset Current	I_{IO}	25	10	pA
Input Bias Current	I_I	40	15	pA

Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC		TEST CONDITIONS V^+ = 15V, V^- = -15 V Unless Otherwise Specified	LIMITS						UNITS
			MINIMUM			MAXIMUM			
			-55°C	+25°C	+125°C	-55°C	+25°C	+125°C	
Input Offset Voltage	V_{IO}	V_{CM} = 1.4 V, V^+ = 5 V	—	—	—	20	12	20	mV
		V_{CM} = 0, V^+ = 15 V	—	—	—	20	12	20	
Input Current	I_I	—	—	—	—	—	40	—	pA
						200	—	100	nA
Input Offset Current	I_{IO}	—	—	—	—	—	25	—	pA
						80	—	50	nA
Supply Current, R_L = ∞	I^+	5 V	—	—	—	1.5	1.4	1.4	mA
		30 V	—	—	—	3.3	3	3	
Voltage Gain R_L = 15 KΩ	A_{OL}	—	—	—	—	10	25	15.4	V/mV
						80	88	83.7	dB
Output Sink Current	I_{SINK}	V_O = 1.4 V, V^+ = 5 V	3	6	8	—	—	—	mA
Saturation Voltage	V_{SAT}	I_{SINK} = 4 mA; $-V_1$ = 1 V, V^+ = 5 V	—	—	—	0.5	0.4	0.35	V
Output Leakage Current	I_{OL}	—	—	—	—	—	1	—	nA
						1	—	1	μA
Common Mode Rejection Ratio	CMRR	V^+ = 5 V	—	—	—	—	562	—	μV/V
Power Supply Rejection Ratio	PSRR	—	—	—	—	—	316	—	μV/V

Group C and D Electrical Characteristic Sampling Tests at T_A = +25°C, V^+ = 15 V, V^- = -15 V

CHARACTERISTIC		LIMITS		UNITS
		MIN.	MAX.	
Input Offset Voltage	V_{IO}	—	15	mV
Input Current	I_I	—	50	pA
Input Offset Current	I_{IO}	—	35	pA
Voltage Gain R_L = 15 KΩ	A_{OL}	20	—	V/mV
Output Sink Current	I_{SINK}	5	—	mA
Saturation Voltage	V_{SAT}	—	48	V
Output Leakage Current	I_{OL}	—	2	nA
Common Mode Rejection Ratio	CMRR	—	780	μV/V

CA3300/...

High-Reliability CMOS Video Speed 6-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

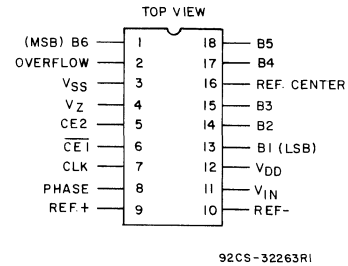
Features:

- *CMOS low power with speed*
- *Parallel conversion technique*
- *15-MHz sampling rate (66-ns conversion time)*
- *6-bit latched 3-state output with overflow bit*
- *±½ LSB accuracy*
- *Single supply voltage (3 to 10 V)*
- *2 units in series allow 7-bit output*
- *2 units in parallel allow 30-MHz sampling rate*
- *Internal V_{REF} with ext V_{REF} option*

The CA3300 is supplied in an 18-lead dual-in-line ceramic package (D suffix) or in chip form (H suffix).

Applications:

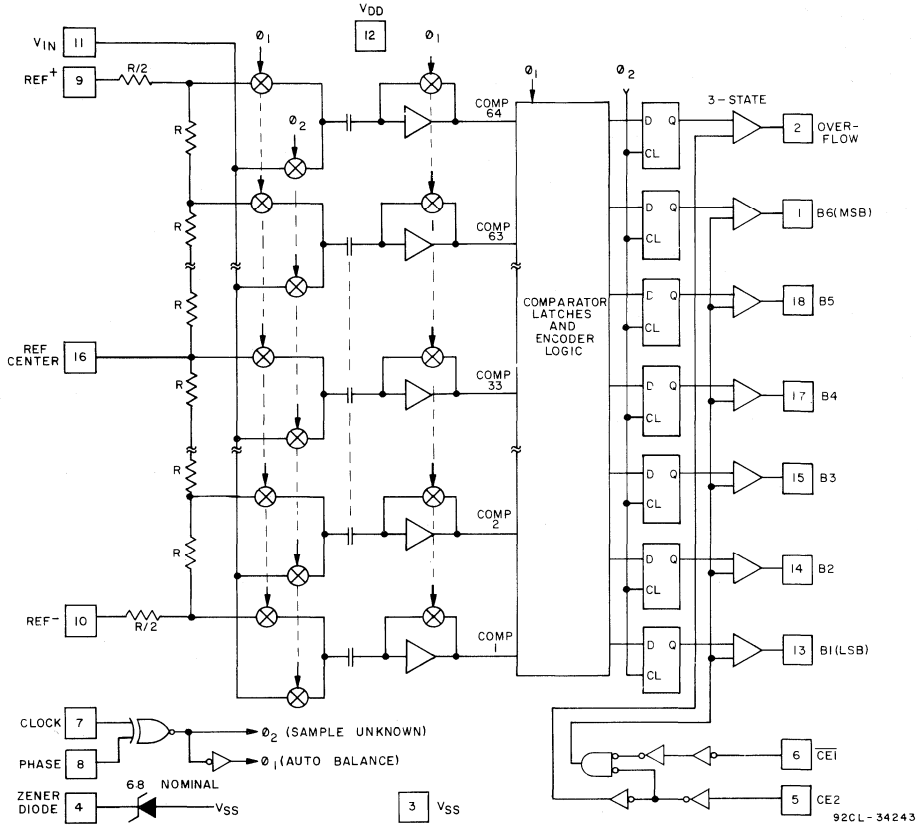
- *The CA3300 is especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security)*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADC's*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*



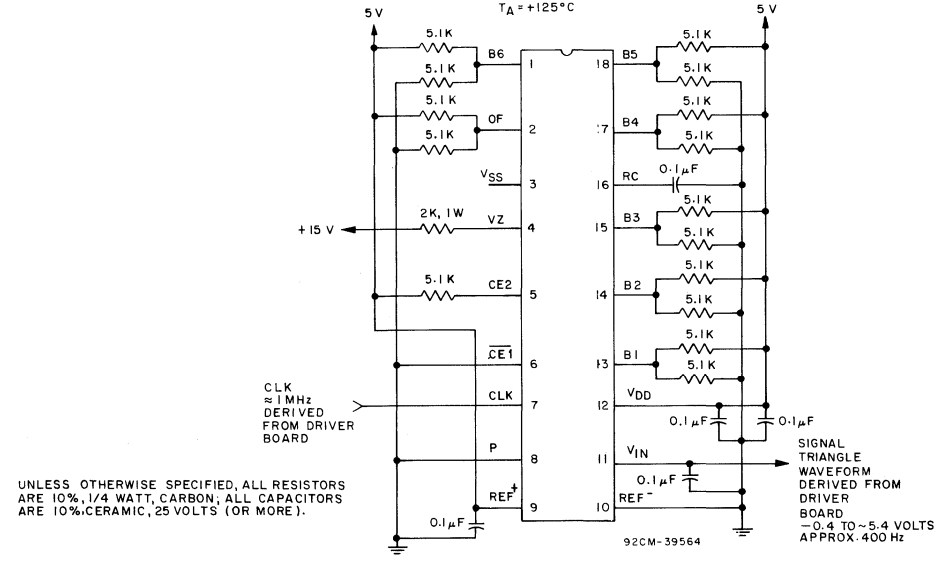
TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE (V_{DD})
(VOLTAGE REFERENCED TO V_{SS} TERMINAL) ..... -0.5 to 10 V
INPUT VOLTAGE RANGE
ALL INPUTS EXCEPT ZENER (PIN 4) ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT
CLK, PH, $\overline{CE1}$, CE2, V_{IN} ..... ± 10 mA
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = -55 to +55°C ..... 315 mW
FOR T_A = +55°C to +125°C ..... Derate linearly at 3.3 mW/°C
TEMPERATURE RANGE
OPERATING ..... -55 to +125°C
STORAGE ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C



Block diagram for the CA3300.



Burn-in and operating life-test circuit.

CA3300/...

ELECTRICAL CHARACTERISTICS

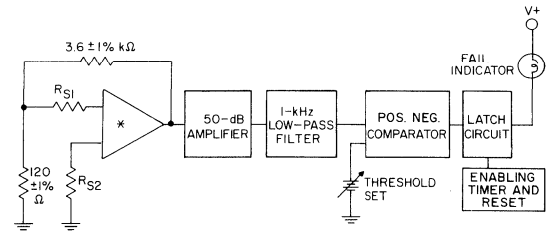
CHARACTERISTIC	TEST CONDITIONS @ 25°C	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	6	Bits
Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=15 MHz, gain adjusted	—	±0.5	±0.8	LSB
Differential Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=15 MHz	—	±0.5	±0.8	
Quantizing Error		-½	—	½	
Analog Input:	V_{DD}=8 V				
Full Scale Range	CLK=15 MHz	2.4	—	V_{DD}+0.5	V
Input Capacitance		—	50	—	pF
Input Current		—	600	1000	μA
Gain Temperature Coefficient	V_{DD}=8 V, CLK=15 MHz	—	0.016	—	LSB/°C
Maximum Conversion Speed	V_{DD}=5 V	—	12M	—	SPS
	V_{DD}=8 V	15M	19M	—	
Device Current	V_{DD}=5 V (CLK=11 MHz)	—	7	—	mA
(Excludes I_{REF}, I_Z)	V_{DD}=8 V (CLK=15 MHz)	—	22	—	
	V_{DD}=5 V (Auto Balance State)	—	6.4	16	
	V_{DD}=8 V (Auto Balance State)	—	24	40	
Ladder Impedance		1000	1400	1800	Ω
Digital Inputs:					
Low Voltage	V_{DD}=5 V	—	—	1.5	V
	V_{DD}=8 V	—	—	2.5	
High Voltage	V_{DD}=5 V	3.5	—	—	V
	V_{DD}=8 V	5.5	—	—	
Input Current	V_{DD}=8 V	—	±1	—	μA
Digital Outputs:					
Output Low	V_{DD}=5 V, V_O=0.4 V	1.6	10	—	mA
(Sink) Current	V_{DD}=8 V, V_O=0.5 V	3.2	15	—	
Output High	V_{DD}=5 V, V_O=4.6 V	-0.8	6	—	
(Source) Current	V_{DD}=8 V, V_O=7.5 V	-1.6	9	—	
Zener Voltage	I_Z=10 mA	6.2	6.8	7.4	V
Zener Dynamic Impedance	I_Z=10 mA	—	10	30	Ω
Zener Temperature Coefficient		—	0.5	—	mV/°C
Digital Output Delay, t_d	V_{DD}=8 V	—	20	—	ns
Aperture Time	V_{DD}=8 V	—	25	—	
	T_A=-55°C or T_A=+125°C				
Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=10 MHz			+1 -0.8	LSB

High-Reliability Operational Amplifier

See the CA741 types with the additional Subgroup A Test ("Popcorn") below.

ELECTRICAL CHARACTERISTICS - CA6741T

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts; $V^+ = 15$, $V^- = -15$ $T_A = 25^oC$	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz $R_{S1} = R_{S2} = 100\ k\Omega$			Device is rejected if the total noise voltage (burst + $1/f$), referred to input, exceeds 20 μV peak, during a 30-sec. test period.	



R_{S1} & R_{S2} = 100 kΩ FOR CA6741T AND 200 kΩ FOR CA6078AT
* CA6741T OR CA6078AT

92CS-19423

Block diagram of burst-noise "popcorn" test equipment.

HR3N187

High-Reliability Silicon Dual Insulated-Gate Field-Effect Transistor

With Integrated Gate-Protection Circuits
For Applications in Aerospace, Military, and Critical Industrial Equipment up to 300 MHz

Device Features:

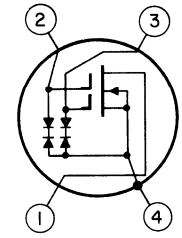
- **Back-to-back diodes to protect each gate against handling and in-circuit transients**
- **High forward transconductance – g_{FS} = 12,000 μmho (typ.)**
- **High unneutralized RF power gain – G_{ps} = 18 dB(typ.) at 200 MHz**
- **Low VHF noise figure – 3.5 dB(typ.) at 200 MHz**

Applications

- **RF amplifier amplifier, mixer, and IF amplifier in military, and industrial communications equipment**
- **Aircraft and marine vehicular receivers**
- **CATV and MATV equipment**
- **Telemetry and multiplex equipment**

Performance Features

- **Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's**
- **Wide dynamic range permits large-signal handling before overload**
- **Virtually no agc power required**
- **Greatly reduces spurious responses in FM receivers**



LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

Terminal diagram.

The HR3N187 is hermetically sealed in the metal JEDEC TO-72 package.

MAXIMUM RATINGS, *Absolute-Maximum Values, at T_A = 25° C*

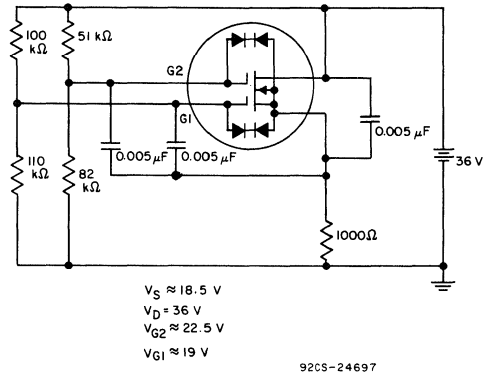
DRAIN-TO-SOURCE VOLTAGE, V_{DS} ..... -0.2 to +20 V
GATE No. 1-TO-SOURCE VOLTAGE, V_{G1S}:
  Continuous (dc) ..... -6 to +3 V
  Peak ac ..... -6 to +6 V
GATE No. 2-TO-SOURCE VOLTAGE, V_{G2S}:
  Continuous (dc) ..... -6 to 30% of V_{DS} V
  Peak ac ..... -6 to +6 V
*DRAIN-TO-GATE VOLTAGE,
  V_{DG1} OR V_{DG2} ..... +20 V
*DRAIN CURRENT, I_D ..... 50 mA
*TRANSISTOR DISSIPATION P_T:
  At ambient temperatures } up to 25° C ..... 330 mW
  At ambient temperatures } above 25° C ..... derate linearly at 2.2 mW/° C
*AMBIENT TEMPERATURE RANGE:
  Storage and Operating ..... -65 to +175° C
*LEAD TEMPERATURE (During Soldering):
  At distances ≥ 1/32 inch from seating surface for 10 seconds max. ..... 265° C

*In accordance with JEDEC Registration Data Format JS-9 RDF-19A

HR3N187

Final Electrical Tests, *at* $T_A = 25°C$

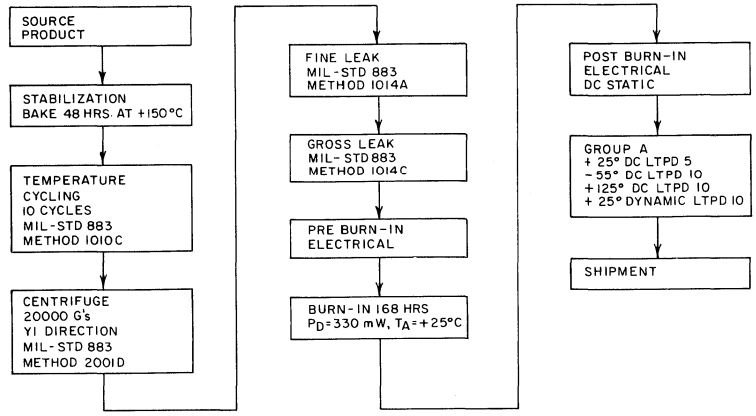
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			Min.	Max.	
Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V	-0.5	-4	V
Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0	-0.5	-4	V
Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +6 V, V_{G2S} = V_{DS} = 0	–	50	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V, V_{G2S} = V_{DS} = 0	–	50	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V, V_{G1S} = V_{DS} = 0	–	50	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V, V_{G1S} = V_{DS} = 0	–	50	nA
Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V, V_{G2S} = +4 V V_{G1S} = 0	5	30	mA
Gate-to-Source Forward Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	6.5	–	V
Gate No. 2	$V_{(BR)G2SSF}$				
Gate-to-Source Reverse Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	-6.5	–	V
Gate No. 2	$V_{(BR)G2SSR}$				



Burn-In and operating life-test circuit.

HR3N187

High-Reliability Processing Flow Chart



High-Reliability Silicon Dual Insulated-Gate Field-Effect Transistor

With Integrated Gate-Protection Circuits
For Applications in Aerospace, Military, and Critical Industrial Equipment Up to 500 MHz.

Performance Features:

- **Superior cross-modulation performance and greater dynamic range than bipolar and single-gate FET's**
- **Wide dynamic range permits large-signal handling before overload**
- **Dual gate permits simplified agc circuitry**
- **Virtually no agc power required**
- **Greatly reduces spurious responses in FM receivers**

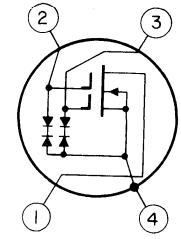
Device Features:

- **Back-to-back diodes protect each gate against handling and in-circuit transients**
- **High forward transconductance – g_{fs} = 15,000 μmho (typ.)**
- **High unneutralized RF power gain – G_{ps} = 12.5 dB (typ.) at 400 MHz = 19 dB (typ.) at 200 MHz**
- **Low VHF noise figure – 4.5 dB (typ.) at 400 MHz 3.0 dB (typ.) at 200 MHz**

The HR3N200 is hermetically sealed in the metal JEDEC TO-72 package.

Applications:

- **RF amplifier, mixer, and IF amplifier in military and industrial communications equipment**
- **Aircraft and marine vehicular receivers**
- **CATV and MATV equipment**
- **Telemetry and multiplex equipment**



LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

Terminal diagram.

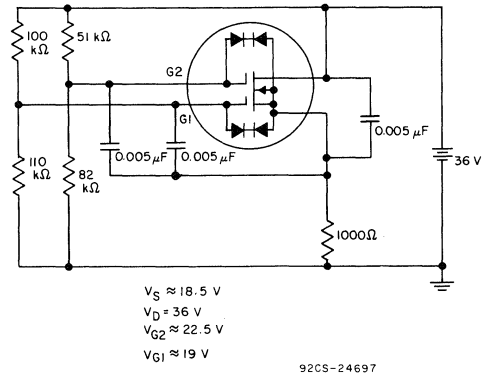
Maximum Ratings, *Absolute-Maximum Values, at T_A = 25° C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No. 1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +3	V
Peak ac	-6 to +6	V
GATE No. 2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
DRAIN CURRENT, I_D	50	mA
TRANSISTOR DISSIPATION P_T:		
At ambient temperatures: up to 25°C	330	mW
At ambient temperatures: above 25°C	derate linearly at 2.2 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32 inch from seating surface for 10 seconds max.	265	°C

HR3N200

Pre Burn-In and Post Burn-In Electrical Go/No-Go Tests

ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$ unless otherwise specified*	SYMBOL	TEST CONDITIONS		LIMITS Min.	LIMITS Max.	UNITS
Gate No. 1-Terminal Forward Current	I_{G1SSF}	$V_{G1S} = +6$ V $V_{G2S} = V_{DS} = 0$		–	50	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	$V_{G1S} = -6$V $V_{G2S} = V_{DS} = 0$		–	50	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	$V_{G2S} = +6$ V $V_{G1S} = V_{DS} = 0$		–	50	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	$V_{G2S} = -6$ V $V_{G1S} = V_{DS} = 0$		–	50	nA
Zero-Bias Drain Current	I_{DS}	$V_{DS} = +15$ V, $V_{G1S} = 0$ $V_{G2S} = +4$ V		0.5	12	mA
Gate-to-Source Forward Breakdown Voltage Gate No. 1	$V_{(BR)G1SSF}$	$I_{G1SSF} =$ $I_{G2SSF} =$ 100 μA	$V_{G2S} = V_{DS} = 0$	6.5	13	V
Gate No. 2	$V_{(BR)G2SSF}$		$V_{G1S} = V_{DS} = 0$			
Gate-to-Source Reverse Breakdown Voltage Gate No. 1	$V_{(BR)G1SSR}$	$I_{G1SSR} =$ $I_{G2SSR} =$ 100 μA	$V_{G2S} = V_{DS} = 0$	-6.5	-13	V
Gate No. 2	$V_{(BR)G2SSR}$		$V_{G1S} = V_{DS} = 0$			



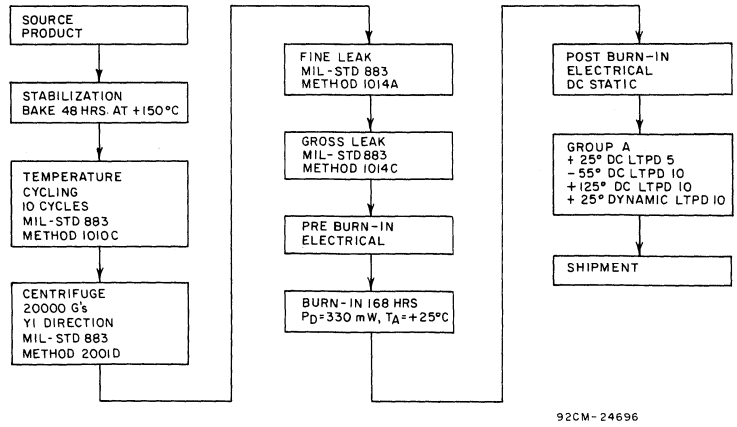
Burn-In and operating life-test circuit.

HR3N200

Final Electrical Tests

ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$ unless otherwise specified*	SYMBOL	TEST CONDITIONS		LIMITS Min.	LIMITS Max.	UNITS
Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V		-0.1	-3	V
Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0		-0.1	-3	V
Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +1 V $V_{G2S} = V_{DS}$ = 0		–	50	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V $V_{G2S} = V_{DS}$ = 0		–	50	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V $V_{G1S} = V_{DS}$ = 0		–	50	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V $V_{G1S} = V_{DS}$ = 0		–	50	nA
Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V, V_{G1S} = 0 V_{G2S} = +4 V		0.5	12	mA
Gate-to-Source Forward Breakdown Voltage Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	$V_{G2S} = V_{DS}$ = 0	6.5	13	V
Gate No. 2	$V_{(BR)G2SSF}$		$V_{G1S} = V_{DS}$ = 0			
Gate-to-Source Reverse Breakdown Voltage Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	$V_{G2S} = V_{DS}$ = 0	-6.5	-13	V
Gate No. 2	$V_{(BR)G2SSR}$		$V_{G1S} = V_{DS}$ = 0			

High-Reliability Processing Flow Chart



92CM-24696

High-Reliability Slash-Series LSI Products

High-Reliability Slash-Series LSI Products

8-Bit CMOS Microprocessor Family

The RCA high-reliability slash-series of CMOS LSI microprocessors, memories, and peripherals are ideally suited for military applications such as mobile ground equipment that must be battery operated and exposed to harsh environments. Use of a highly-reliable, all CMOS LSI technology provides low power operation throughout the military temperature range.

The 'Slash 3' suffix following the type designation indicates that the devices are screened to military specifications as described in the screening sequence.

Features:

- Low power consumption
- Fully static
- Single power supply
- Full temperature range
- High noise immunity
- Complete family which includes RAMs, ROMs, and I/Os
- Leadless-chip-carrier packaging option for selected types
- Full CMOS CDP1802A microprocessor

Index to the RCA High-Reliability 8-Bit CMOS Microprocessor Family

Available to /3 Screening (RCA's Class B Equivalent for LSI Devices)

Type No.	Description
CDP1802A	CMOS 8-Bit Microprocessor
CDP1821*	1024-Word x 1-Bit Static RAM
CDP1822*	256-Word x 4-Bit Static RAM
CDP1823*	128-Word x 8-Bit Static RAM
CDP1824	32-Word x 8-Bit Static RAM
CDM5114*	1024-Word x 4-Bit Static RAM
CDM6116A	2048-Word x 8-Bit Static RAM
CDM6264	8192-Word x 8-Bit Static RAM
CDP1831	512-Word x 8-Bit Static ROM
CDP1832	512-Word x 8-Bit Static ROM
CDP1833	1024-Word x 8-Bit Static ROM
CDP1834	1024-Word x 8-Bit Static ROM
CDP1837C+	4096-Word x 8-Bit Static ROM
CDP1852	8-Bit Input/Output Port
CDP1853	N-Bit 1 of 8 Decoder
CDP1854A	UART
CDP1856	4-Bit Bus Buffer/Separator
CDP1857	4-Bit Bus Buffer/Separator
CDP1858	4-Bit Latch and Memory Interface
CDP1859	4-Bit Latch and Decoder Memory Interface

*CMOS/SOS Technology — Transient-Radiation Resistant

+Available on special order; preliminary data not included in this book.

Note:
Dual-in-line ceramic packages are standard for /3 product.
Other package styles may be available on a special-order basis.

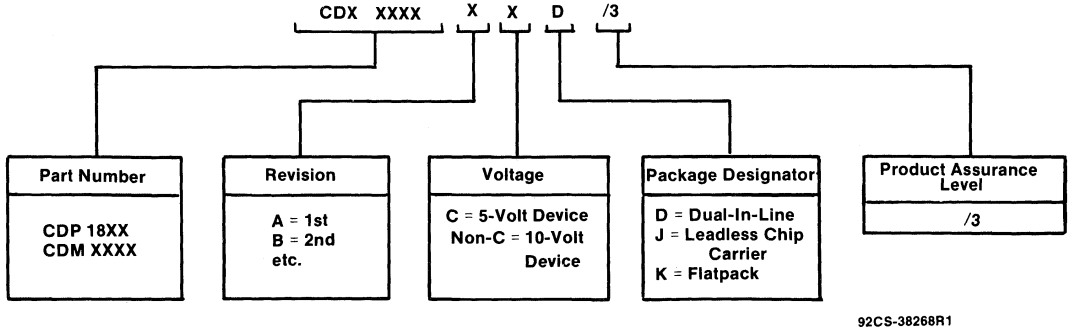
Transient Radiation-Resistant RAMs for Tactical Military Systems

The RCA CDP1821, CDP1822, CDP1823, and CDM5114 RAMs utilize a latch-up free, dielectrically isolated silicon-on-sapphire (SOS) technology that provides inherent resistance to transient-radiation pulses. These devices are ideally suited for systems that must operate during exposure to a high transient-radiation source.

Transient Capability of CMOS/SOS Memories

Temporary Upset	3×10^{10} rads (Si)/Second
Permanent Upset	$\geq 1 \times 10^{11}$ rads (Si)/Second
Latch-Up	Not Possible
Survival	$\geq 1 \times 10^{12}$ rads (Si)/Second

Guide to the Part Number, Package Designator, and Product Assurance Level of RCA High-Reliability CDP18XX Series.



92CS-38268R1

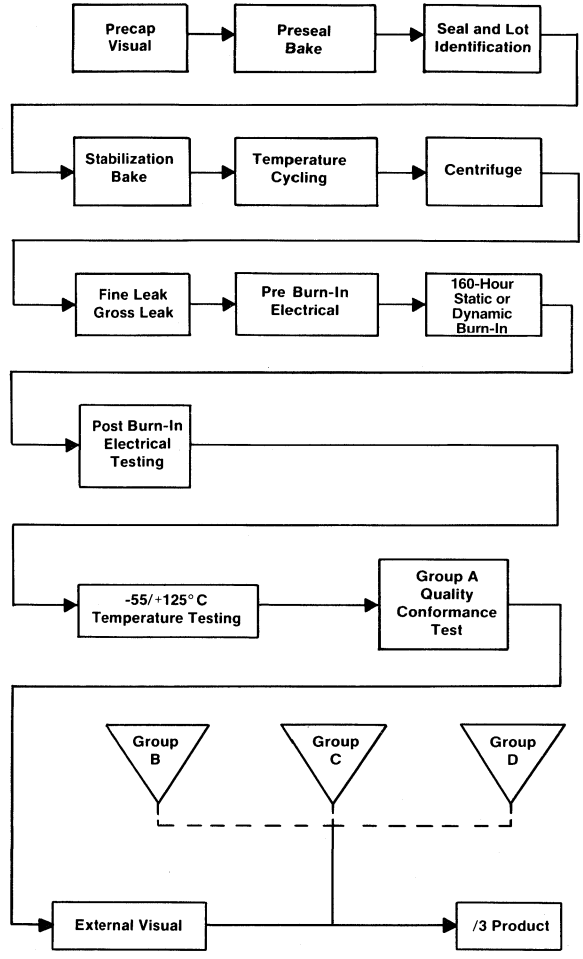
/3 Screening

Screen	Method (MIL-STD-883)	Reqmt.	Notes
Internal Visual	Cond. B Modified for LSI Visual	100%	1 or 3
Pre-Seal Bake	—	100%	
Stabilization Bake	1008 Cond. C 24 Hours	100%	
Temperature Cycling	1010 Cond. C	100%	
Constant Acceleration (Centrifuge)	2001 Cond. D or E Y1 Dir.	100%	
Seal A) Fine B) Gross Initial (Pre Burn-In) Electrical Parameters at 25°C	1014 A or B C Per Applicable Device Spec.	 100% 100% 100%	
Burn-In	1015, 160 Hrs @ 125°C	100%	2
Interim (Post Burn-In) Electrical Parameters at 25°C	Per Applicable Device Spec.	100%	
Final Electrical Test @ -55/125°C	Per Applicable Device Spec.	100%	
Group A Quality Conformance Test	5005	Sample	
External Visual	2009	100%	

Notes:

1. Visual Inspection for RCA High-Rel /3 LSI Product.
   The RCA Internal Visual Inspection Procedure for LSI devices is Military, Visual Condition B, except as follows:
   A. High Magnification Inspection is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 80X to 120X where high magnification is required and at 30X to 60X for low magnification.
   B. Criteria 3.2.1.1 and 3.2.1.2, metallization scratches and voids, are not applied to metallization over the step surrounding the contact cut and in the contact itself.
   C. Criteria 3.2.6.1C has the following notes added: glassivated areas of the die are excluded from the criteria of 3.1.6.1C when the particle or material is attached only at the top surface of the passivation.
   D. 3.2.1.7 is applied to areas of sufficient complexity on each chip to assure general alignment and contact coverage. These areas are inspected at 200X to 300X and consist only of the area exposed to the immediate field of view.
   E. 3.2.2 Diffusion and passivation faults are inspected only in two opposing corners of the chip.
   F. During CSI screening, if individual devices are observed to have defects that clearly violate 3.2.1.1 or 3.2.1.2 at the contact cut or 3.2.2 they are rejected and removed from the lot, but are not counted against any lot acceptance criteria.
2. Refer to the High-Reliability Integrated Circuits DATABOOK or data sheets for burn-in circuit information.
3. Visual Inspection for the CDP1821, CDP1822, CDP1823 and CDM5114 only.
   RCA performs Visual Inspection on /3 SOS LSI devices to MIL-STD-883, Method 2010, Condition 'B' for Bond Inspection (3.2.4), internal leads (3.2.5) and package condition (3.2.6). All other Visual Inspection is to Method 2010, Condition 'B' except as follows:
   A. High magnification inspection is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 80X to 120X where high magnification is required and at 30X to 60X for low magnification.
   B. Criteria 3.2.1.1 and 3.2.1.2, metallization scratches and voids, are not applied to metallization over the step surrounding the contact cut and in the contact itself.
   C. Criteria 3.2.6.1C has the following notes added: Glassivated areas of the die are excluded from the criteria of 3.1.6.1C when the particle or material is attached only at the top surface of the passivation.
   D. 3.2.1.7 is applied to areas of sufficient complexity on each chip to assure general alignment and contact coverage. These areas are inspected at 200X to 300X and consist only of the area exposed to the immediate field of view.
   E. 3.2.2 Diffusion and passivation faults are inspected only in two opposing corners of the chip.
   F. During CSI screening, if individual devices are observed to have defects that clearly violate 3.2.1.1 or 3.2.1.2 at the contact cut or 3.2.2 they are rejected and removed from the lot, but are not counted against any lot acceptance criteria.
   G. 3.2.3C. Cracks greater than 5 mils are rejected only if they point to or cross the grid line.

/3 Screening Tests



Groups B, C and D Conformance Testing are Performed if Specifically Ordered.

/3 Product Information:

Die Attach ..... Eutectic or Epoxy
Manufacturing Location ..... USA, Off-Shore

Data Supplied With Order for /3 Packaged Devices

A) Certificate of Conformance
B) Group A Acceptance Test Results

CDP1800-Series Ratings and Reliability

Maximum Ratings, Absolute Maximum Values

DC SUPPLY-VOLTAGE RANGE, (V_{CC}, V_{DD})
(All voltage values referenced to V_{SS} terminal)

$V_{CC} \leq V_{DD}$:

CDP1800 Series ..... -0.5 to +11 V
CDP1800C Series ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to VDD + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ± 10 mA
POWER DISSIPATION PER PACKAGE (PD):
For T_A = -55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Lineraly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package Temperature Range.
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	/3		C/3		
	MIN.	MAX.	MIN.	MAX.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

Life-Test History of Ceramic /3 Devices

Type	Total Quantity	Unit Hours	Rejects
1802A (1978-1984)	949	780,088	0
1822 (1983)	102	102,408	0
1824 (1979-1983)	374	183,842	0
1834 (1982-1983)	207	208,694	0
1852 (1982-1984)	94	75,226	0
1853 (1982-1984)	373	345,381	0
1856 (1983)	160	167,920	0
1857 (1982-1983)	169	183,753	0
1859 (1982-1983)	264	273,954	1
Total	2,692	2,321,266	1

Failure rate of 0.089% per 1000 hours at 125°C.

60% Confidence Level.

Extrapolated to 55°C with a 1.0-eV activation energy, the failure rate is 1.8 per 10^9 device hours.

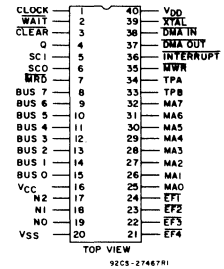
CDP1802A/3, CDP1802AC/3

High-Reliability CMOS 8-Bit Microprocessor

For Use in Aerospace, Military, and Critical Industrial Equipment

Features

- *Minimum instruction fetch-execute time of 2.2 μs (maximum clock frequency of 7.4 MHz) at V_{DD} = 10 V, T_A = 25° C*
- *Operation over the full military temperature range -55° C to +125° C*
- *Any combination of standard RAM and ROM up to 65,536 bytes*
- *8-bit parallel organization with bidirectional data bus and multiplexed address bus*
- *16 x 16 matrix of registers for use as multiple program counters, data pointers, or data registers*
- *On-chip DMA, interrupt, and flag inputs*
- *High noise immunity - 30% of V_{DD}*



TERMINAL ASSIGNMENT

The RCA-CDP1802A/3 high-reliability LSI CMOS 8-bit register-oriented central-processing unit (CPU) is designed for use as a general-purpose computing or control element in a wide range of stored-program systems or products.

The CDP1802A/3 includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

The 1800 series architecture is designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The 1800 series CPU also provides a synchronous interface to memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Further, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct memory-access modes.

The CDP1802A/3 and CDP1802AC/3 are functionally identical. They differ in that the CDP1802A/3 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1802AC/3 a recommended operating voltage range of 4 to 6.5 volts.

The CDP1802A/3 is functionally identical to its predecessor, the CDP1802. The "A" version includes some performance enhancements and can be used as a direct replacement in systems using the CDP1802.

These types are supplied in 40-lead dual-in-line side-brazed ceramic packages (D suffix), that conforms to MIL-M-38510 Case Outline D-5. Other package styles may be available on a special order basis.

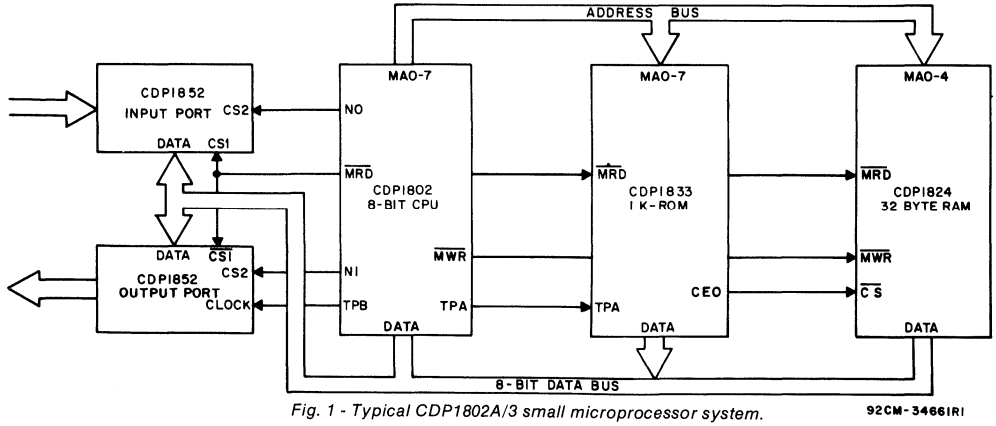


Fig. 1 - Typical CDP1802A/3 small microprocessor system. 92CM-34661R1

CDP1802A/3, CDP1802AC/3

RECOMMENDED OPERATING CONDITIONS at T_A = FULL-PACKAGE TEMPERATURE RANGE.
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	LIMITS				UNITS
	CDP1802A/3		CDP1802AC/3		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	
Maximum Clock Input Rise or Fall Time tr, tf	—	1	—	1	μs

PERFORMANCE CHARACTERISTICS

CHARACTERISTIC	V_{DD} V	LIMITS				UNITS
		CDP1802A/3		CDP1802AC/3		
		-55°C to +25°C	+125°C	-55°C to +25°C	+125°C	
Minimum Instruction Time Δ	5	4.5	5.9	4.5	5.9	μs
	10	2.2	2.8	—	—	
Maximum DMA Transfer Rate	5	450	340	450	340	KBytes per
	10	925	700	—	—	second
Maximum Clock Input Frequency, Load Capacitance(C_L) = 50 pF f_{CL}	5	DC-3.6	DC-2.7	DC-3.6	DC-2.7	MHz
	10	DC-7.4	DC-5.6	—	—	

Δ Equals 2 machine cycles — one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles — one Fetch and two Execute operations.

CDP1802A/3, CDP1802AC/3

STATIC ELECTRICAL CHARACTERISTICS * All Limits are 100% Tested

CHARACTERISTIC		CONDITIONS			LIMITS				UNITS
		VOUT (V)	VIN (V)	VCC, VDD (V)	-55° C, +25° C		+125° C		
					Min.	Max.	Min.	Max.	
Quiescent Device Current	IDD	—	—	5	—	100	—	250	μA
		—	—	10	—	120	—	300	
Output Low Drive (Sink) Current	IOL	0.4	0, 5	5	1.20	—	0.90	—	mA
(Except $\overline{XTAL}$)		0.5	0, 10	10	2.50	—	1.85	—	
$\overline{XTAL}$	IOL	0.4	5	5	185	—	140	—	μA
Output High Drive (Source) Current	IOH	4.6	0, 5	5	—	-0.30	—	-0.20	mA
(Except $\overline{XTAL}$)		9.5	0, 10	10	—	-0.60	—	-0.40	
$\overline{XTAL}$	IOH	4.6	0	5	—	-135	—	-100	μA
Output Voltage Low-Level	VOL	—	0, 5	5	—	0.1	—	0.2	V
		—	0, 10	10	—	0.1	—	0.2	
Output Voltage High Level	VOH	—	0, 5	5	4.9	—	4.8	—	
		—	0, 10	10	9.9	—	9.8	—	
Input Low Voltage	VIL	0, 5	—	5	—	1.5	—	1.5	
		0, 10	—	10	—	3	—	3	
Input High Voltage	VIH	0.5, 4.5	—	5	3.5	—	3.5	—	
		0, 10	—	10	7	—	7	—	
Input Leakage Current	IIN	Any Input	0, 5	5	—	±1	—	±5	μA
			0, 10	10	—	±1	—	±5	
3-State Output Leakage Current	IOUT	0, 5	0, 5	5	—	±1	—	±5	
		0, 10	0, 10	10	—	±1	—	±5	

* 5-V level characteristics apply to part CDP1802AC/3
5-V and 10-V level characteristics apply to part CDP1802A/3

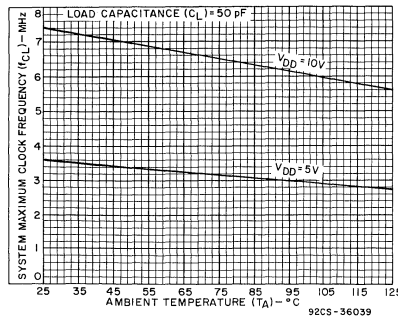


Fig. 2 - Typical maximum clock frequency as a function of temperature.

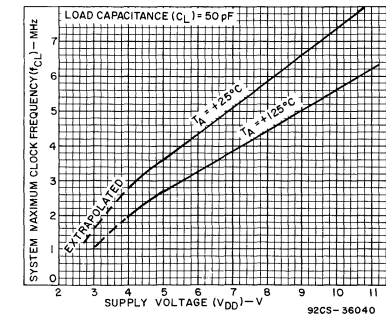


Fig. 3 - Typical maximum clock frequency as a function of supply voltage.

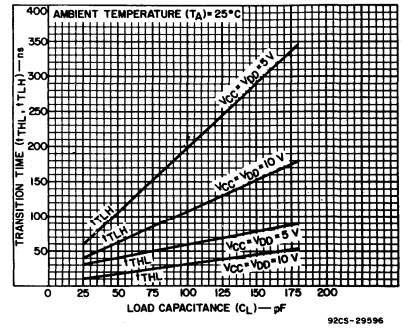


Fig. 4 – Typical transition time vs. load capacitance.

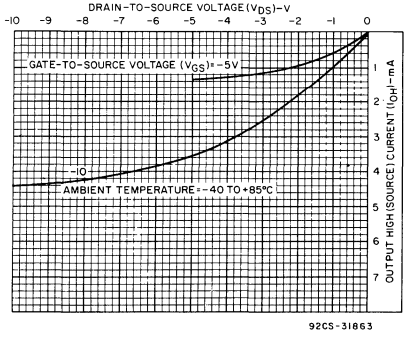


Fig. 5 – Minimum output high (source) current characteristics.

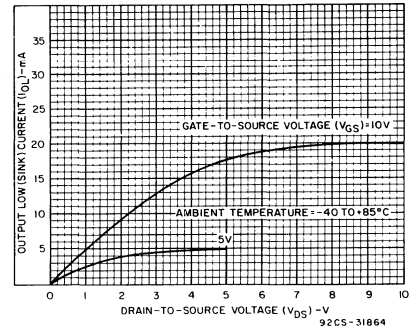


Fig. 6 – Minimum output low (sink) current characteristics.

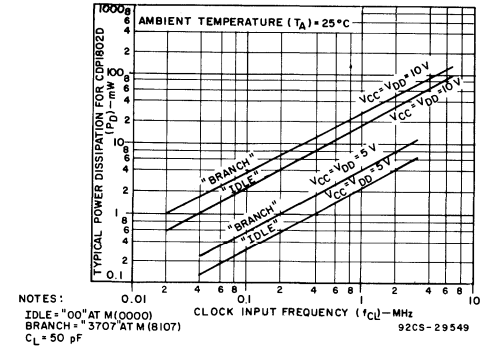


Fig. 7 – Typical power dissipation as a function of clock frequency for BRANCH instruction and IDLE instruction.

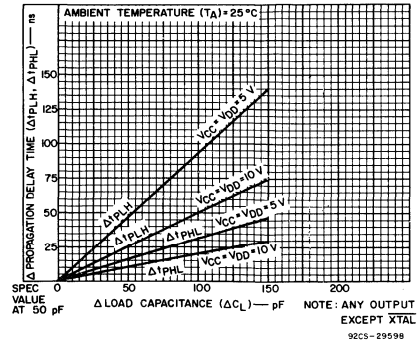


Fig. 8 – Typical change in propagation delay as a function of a change in load capacitance.

CDP1802A/3, CDP1802AC/3

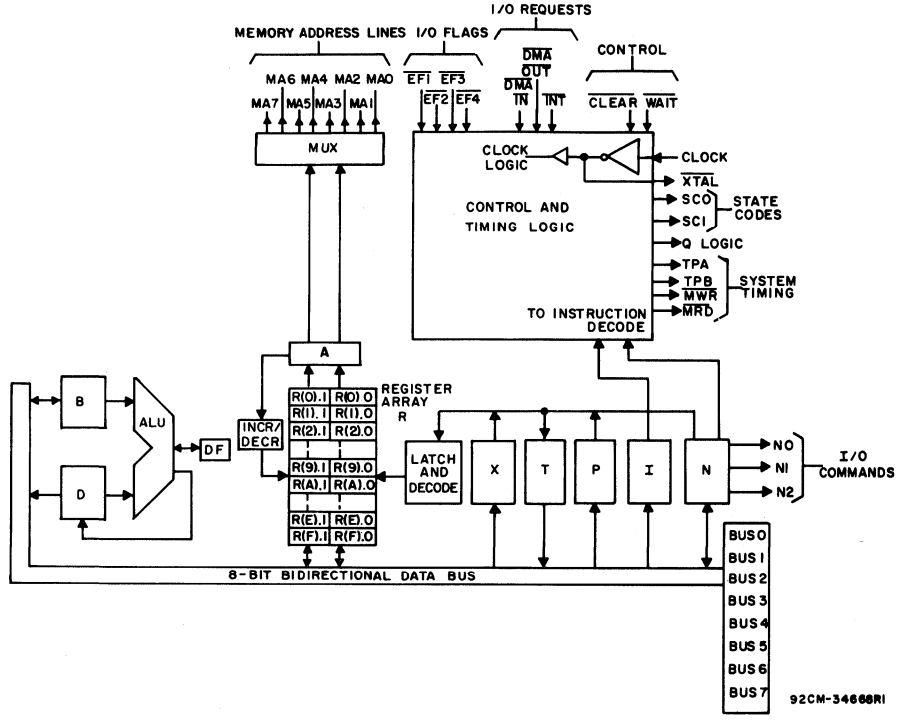


Fig. 9 - CDP1802A/3 block diagram.

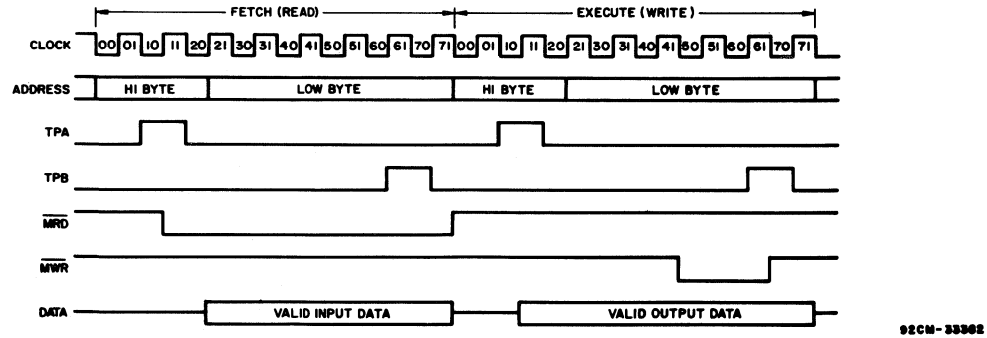


Fig. 10 - Basic dc timing waveforms, one instruction cycle.

SIGNAL DESCRIPTIONS

Bus 0 to BUS 7 (Data Bus):

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O) Lines):

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal.
$\overline{MRD}$ = Vcc: Data from I/O to CPU and Memory
$\overline{MRD}$ = Vss: Data from Memory to I/O

$\overline{EF1}$ to $\overline{EF4}$ (4 Flags):

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

$\overline{INTERRUPT}$, $\overline{DMA\text{-}IN}$, $\overline{DMA\text{-}OUT}$ (3 I/O Requests)

These inputs are sampled by the CDP1802A/3 during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and Interrupt requests, DMA-IN has priority followed by DMA-OUT and then Interrupt.

SC0, SC1, (2 State Code Lines):

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA. H= Vcc, L= Vss.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB (2 Timing Pulses):

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

MA0 to MA7 (8 Memory Address Lines):

In each cycle, the higher-order byte of a 16-bit CPU memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64K bytes.

$\overline{MWR}$ (Write Pulse):

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{MRD}$ (Read Level):

A low level on $\overline{MRD}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, $\overline{MRD}$ is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction. For additional information see Table I.

Q:

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK:

Input for externally generated single-phase clock. The clock is counted down internally to 8 clock pulses per machine cycle.

$\overline{XTAL}$:

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{XTAL}$) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be required at terminals 1 and 39. For additional information, see ICAN-6565.

$\overline{WAIT}$, $\overline{CLEAR}$ (2 Control Lines):

Provide four control modes as listed in the following truth table:

$\overline{CLEAR}$	$\overline{WAIT}$	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

CDP1802A/3, CDP1802AC/3

ARCHITECTURE

The CPU block diagram is shown in Fig. 9. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. the D register (either of the two bytes can be gated to D);
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

With two exceptions, CPU instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and third if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. indicate to the I/O devices a command code or device-selection code for peripherals;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions (70-73 and 78-7B);
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations F1-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions — 70-73, 78, 60, F0.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the 1800-series architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, four instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

The Q Flip Flop

An internal flip flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a microprocessor output.

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request occurs and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Interrupt Enable is automatically de-activated to inhibit further interruptions. The user's interrupt routine is now in control; the contents of T may be saved by means of a single instruction (78) in the memory location pointed to by R(X). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with a single instruction (70 or 71). The Interrupt-Enable flip flop can be activated to permit further interrupts or can be disabled to prevent them.

CPU Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer

N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nibble)
IE	1 Bit	Interrupt Enable
Q	1 Bit	Output Flip Flop

CDP1802A/3 Control Modes

The $\overline{WAIT}$ and $\overline{CLEAR}$ lines provide four control modes as listed in the following truth table:

$\overline{CLEAR}$	$\overline{WAIT}$	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

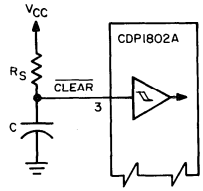
The function of the modes are defined as follows:

Load

Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

Reset

Registers I, N, Q are reset, IE is set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Powerup reset can be realized by connecting an RC network directly to the CLEAR pin, since it has a Schmitt-triggered input, see Fig. 11.



92CS-33873

Fig. 11 - Reset diagram.

The RC time constant should be greater than the oscillator start-up time (typically 20 ms).

Pause

Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RUN-MODE STATE TRANSITIONS

The CDP1802A/3 CPU state transitions when in the RUN and RESET modes are shown in Fig. 12. Each machine cycle requires the same period of time, 8 clock pulses, except the initialization cycle, which requires 9 clock pulses. The execution of an instruction requires either two or three machine cycles, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response. Table II shows the conditions on Data Bus and Memory-Address lines during all machine states.

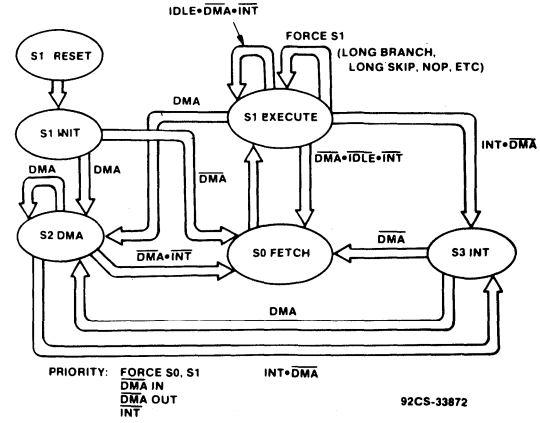


Fig. 12 - State transition diagram.

CDP1802A/3, CDP1802AC/3

INSTRUCTION SET

The CPU instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where
W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)

Operation Notation
M(R(N)) → D; R(N) + 1 → R(N)

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I — INSTRUCTION SUMMARY (See Notes following table, pp. 12 and 13)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N))→D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N))→D; (RN)+1→R(N)
LOAD VIA X	LDX	F0	M(R(X))→D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X))→D; R(X)+1→R(X)
LOAD IMMEDIATE	LDI	F8	M(R(P))→D; R(P)+1→R(P)
STORE VIA N	STR	5N	D→M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D→M(R(X)); R(X)−1→R(X)
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N)+1→R(N)
DECREMENT REG N	DEC	2N	R(N)−1→R(N)
INCREMENT REG X	IRX	60	R(X)+1→R(X)
GET LOW REG N	GLO	8N	R(N).0→D
PUT LOW REG N	PLO	AN	D→R(N).0
GET HIGH REG N	GHI	9N	R(N).1→D
PUT HIGH REG N	PHI	BN	D→R(N).1
LOGIC OPERATIONS ϕ			
OR	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D→D; R(P)+1→R(P)
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D→D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D→D; R(P)+1→R(P)
AND	AND	F2	M(R(X)) AND D→D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D→D; R(P)+1→R(P)
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)→DF, O→MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76§	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
RING SHIFT RIGHT	RSHR		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E§	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	RSHL		

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS ϕ			
ADD	ADD	F4	M(R(X))+D→DF, D
ADD IMMEDIATE	ADI	FC	M(R(P))+D→DF,D; R(P)+1→R(P)
ADD WITH CARRY	ADC	74	M(R(X))+D+DF→DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P))+D+DF→DF, D R(P)+1→R(P)
SUBTRACT D	SD	F5	M(R(X))−D→DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P))−D→DF, D; R(P)+1→R(P)
SUBTRACT D WITH BORROW	SDB	75	M(R(X))−D−(NOT DF)→DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P))−D−(NOT DF)→DF, D; R(P)+1→R(P)
SUBTRACT MEMORY	SM	F7	D−M(R(X))→DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D−M(R(P))→DF, D; R(P)+1→R(P)
SUBTRACT MEMORY WITH BORROW	SMB	77	D−M(R(X))−(NOT DF)→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D−M(R(P))−(NOT DF)→DF, D R(P)+1→R(P)
BRANCH INSTRUCTIONS—SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38§	R(P)+1→R(P)
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF DF=1	BDF	33§	IF DF=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B§	IF DF=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=F	BQ	31	IF Q=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF1=1 ($\overline{EF1}$=V_{SS})	B1	34	IF EF1=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF1=0 ($\overline{EF1}$=V_{CC})	BN1	3C	IF EF1=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF2=1 ($\overline{EF2}$=V_{SS})	B2	35	IF EF2=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF2=0 ($\overline{EF2}$=V_{CC})	BN2	3D	IF EF2=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF3=1 ($\overline{EF3}$=V_{SS})	B3	36	IF EF3=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF3=0 ($\overline{EF3}$=V_{CC})	BN3	3E	IF EF3=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS—SHORT BRANCH			
SHORT BRANCH IF EF4=1 (EF4=V_{SS})	B4	37	IF EF4=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF4=0 (EF4=V_{CC})	BN4	3F	IF EF4=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
BRANCH INSTRUCTIONS—LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P)+1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8§	R(P)+2→R(P)
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF DF=0	LBNF	CB	IF DF=0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38§	R(P)+1→R(P)
LONG SKIP (SEE NLBR)	LSKP	C8§	R(P)+2→R(P)
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P)+2→R(P) ELSE CONTINUE

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)−1→R(2)
RETURN	RET	70	M(R(X))→(X,P); R(X)+1→R(X) 1→IE
DISABLE	DIS	71	M(R(X))→(X,P); R(X)+1→R(X) 0→IE
INPUT-OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS;R(X)+1→R(X); N LINES=1
OUTPUT 2	OUT 2	62	M(R(X))→BUS;R(X)+1→R(X); N LINES=2
OUTPUT 3	OUT 3	63	M(R(X))→BUS;R(X)+1→R(X); N LINES=3
OUTPUT 4	OUT 4	64	M(R(X))→BUS;R(X)+1→R(X); N LINES=4
OUTPUT 5	OUT 5	65	M(R(X))→BUS;R(X)+1→R(X); N LINES=5
OUTPUT 6	OUT 6	66	M(R(X))→BUS;R(X)+1→R(X); N LINES=6
OUTPUT 7	OUT 7	67	M(R(X))→BUS;R(X)+1→R(X); N LINES=7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES=1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES=2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES=3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES=4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES=5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES=6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES=7

Notes:

ʃThe arithmetic operations and the shift instructions are the only instructions that can alter the DF.
After an add instruction:
DF=1 Denotes a carry has occurred
DF=0 Denotes a carry has not occurred
After a subtract instruction:
DF=1 Denotes no borrow. D is a true positive number
DF=0 Denotes a borrow. D is two's complement
The syntax "—(Not DF)" denotes the subtraction of the borrow

§This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

#An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request ($\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, or $\overline{\text{DMA-OUT}}$) is activated. When the request is acknowledged, the idle cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

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Additional Notes for TABLE I

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch +2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high- and low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

   The short-branch instruction can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test the status (1 or 0) of the four EF flags
   f) Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

   The Long-Skip instructions take three cycles to complete (1 fetch +2 execute).

   They can:
   a) Skip unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test for IE=1

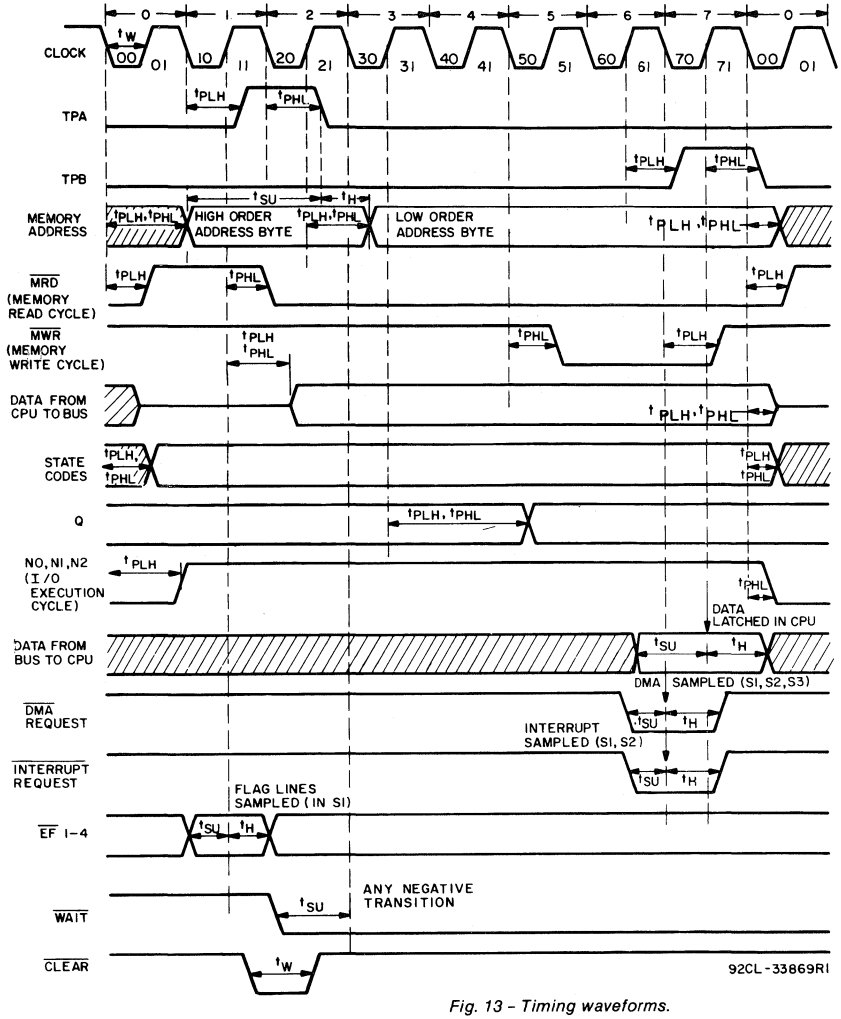
   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken.

   Execution is continued by fetching the next instruction in sequence.

TIMING SPECIFICATIONS as a function of T ($T = 1/f_{CLOCK}$), C_L = 50 pF

CHARACTERISTIC		V_{DD} (V)	LIMITS* -55°C +25°C	LIMITS* +125°C	UNITS
High-Order Memory-Address Byte Set Up to TPA Time	t_{SU}	5	2T-450	2T-580	ns
		10	2T-210	2T-275	
High-Order Memory-Address Byte Hold after TPA Time	t_H	5	T/2+0	T/2+0	
		10	T/2+0	T/2+0	
Low-Order Memory-Address Byte Hold after WR Time	t_H	5	T-30	T-40	
		10	T-10	T-20	
CPU Data to Bus Hold after WR Time	t_H	5	T-170	T-250	
		10	T-80	T-110	
Required Memory Access Time Address to Data	t_{ACC}	5	5T-300	5T-400	
		10	5T-150	5T-200	

* These limits are not directly tested.



NOTES:
1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE
2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS
3. SHADED AREAS INDICATE "DON'T CARE" OR UNDEFINED STATE; MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD

Fig. 13 - Timing waveforms.

IMPLICIT CHARACTERISTICS * T_A = -55°C to +25°C

CHARACTERISTIC			V_{DD} (V)	TYPICAL VALUES	UNITS
Typical Total Power Dissipation	f = 2 MHz		5	4	mW
Idle "00" at M(0000), C_L = 50 pF	f = 4 MHz		10	30	
Effective Input Capacitance Any Input		C_{IN}	—	5	pF
Effective 3-State Terminal Capaciatance DATA BUS			—	7.5	
Minimum Data Retention Voltage		V_{DR}	—	2.4	V
Data Retention Current		I_{DR}	2.4	10	μA

* These characteristics are not tested. Typical values are provided for guidance only.

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DYNAMIC ELECTRICAL CHARACTERISTICS C_L = 50 pF, Timing Measurement at 0.5 V_{DD} Point

CHARACTERISTIC		VDD (V)	LIMITS				UNITS
			-55° C to +25° C		+125° C		
			Min.	Max.	Min.	Max.	
Propagation Delay Times:		5	—	275	—	370	ns
Clock to TPA, TPB	t_{PLH}, t_{PHL}	10	—	125	—	170	
Clock-to-Memory High-Address		5	—	725	—	950	
Byte	t_{PLH}, t_{PHL}	10	—	340	—	450	
Clock-to-Memory Low-Address		5	—	340	—	425	
Byte Valid	t_{PLH}, t_{PHL}	10	—	150	—	200	
Clock to $\overline{MRD}$	t_{PLH},t_{PHL}	5	—	340	—	425	
		10	—	150	—	200	
Clock to $\overline{MWR}$	t_{PLH}, t_{PHL}	5	—	275	—	370	
		10	—	125	—	170	
Clock to (CPU DATA to BUS)		5	—	430	—	550	
Valid	t_{PLH}, t_{PHL}	10	—	200	—	260	
Clock to State Code	t_{PLH}, t_{PHL}	5	—	440	—	550	
		10	—	200	—	260	
Clock to Q	t_{PLH}, t_{PHL}	5	—	375	—	475	
		10	—	175	—	230	
Clock to N (0-2)	t_{PLH}, t_{PHL}	5	—	400	—	525	
		10	—	200	—	260	
Interface Timing Requirements:		5	10	—	10	—	
Data Bus Input Setup	t_{SU}	10	20	—	20	—	
Data Bus Input Hold	t_{H}■	5	175	—	230	—	
		10	80	—	110	—	
$\overline{DMA}$ Setup	t_{SU}	5	10	—	10	—	
		10	20	—	20	—	
$\overline{DMA}$ Hold	t_{H}■	5	200	—	270	—	
		10	100	—	135	—	
Interrupt Setup	t_{SU}	5	10	—	10	—	
		10	20	—	20	—	
Interrupt Hold	t_{H}■	5	175	—	230	—	
		10	80	—	110	—	
$\overline{WAIT}$ Setup	t_{SU}	5	30	—	30	—	
		10	20	—	20	—	
$\overline{EF1\text{-}4}$ Setup	t_{SU}	5	20	—	20	—	
		10	50	—	50	—	
$\overline{EF1\text{-}4}$ Hold	t_{H}■	5	100	—	135	—	
		10	50	—	65	—	
Required Pulse Width Times:		5	150	—	200	—	
$\overline{CLEAR}$ Pulse Width	t_{WL}■	10	75	—	100	—	
$\overline{CLOCK}$ Pulse Width	t_{WL}	5	140	—	185	—	
		10	68	—	90	—	

5-V level characteristics apply to part CDP1802AC/3.

5-V level and 10-V level characteristics apply to part CDP1802A/3.

■ Minimum input Setup and Hold Times required by part CDP1802A/3.

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	OPCODE REG. I	OPCODE REG. N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES[G]
S1	RESET			0→I,N,Q,X,P; 1→IE	00	XXXX	1	1	0	A
S1	INITIALIZE NOT PROGRAMMER ACCESSIBLE			0000→R	00	XXXX	1	1	0	B
S0	FETCH			MRP→I, N; RP+1→RP	MRP	RP	0	1	0	C
S1	0	0	IDL	IDLE	MR0	R0	0	1	0	D,3
	0	1-F	LDN	MRN→D	MRN	RN	0	1	0	3
	1	0-F	INC	RN+1→RN	FLOAT	RN	1	1	0	1
	2	0-F	DEC	RN−1→RN	FLOAT	RN	1	1	0	1
	3	0-F	SHORT BRANCH	TAKEN; MRP→RP.0 NOT TAKEN; RP+1→RP	MRP	RP	0	1	0	3
	4	0-F	LDA	MRN→D; RN+1→RN	MRN	RN	0	1	0	3
	5	0-F	STR	D→MRN	D	RN	1	0	0	2
	6	0	IRX	RX+1→RX	MRX	RX	0	1	0	2
	6	1	OUT 1	MRX→BUS; RX+1→RX	MRX	RX	0	1	1	6
		2	OUT 2						2	
		3	OUT 3						3	
		4	OUT 4						4	
		5	OUT 5						5	
		6	OUT 6						6	
		7	OUT 7						7	
	6	9	INP 1	BUS→MRX,D	DATA FROM I/O DEVICE	RX	1	0	1	5
		A	INP 2						2	
		B	INP 3						3	
		C	INP 4						4	
		D	INP 5						5	
		E	INP 6						6	
		F	INP 7						7	
	7	0	RET	MRX→(X,P); RX+1→RX; 1→IE	MRX	RX	0	1	0	3
		1	DIS	MRX→(X,P); RX+1→RX; 0→IE	MRX	RX	0	1	0	3
		2	LDXA	MRX→D; RX+1→RX	MRX	RX	0	1	0	3
		3	STXD	D→MRX; RX−1→RX	D	RX	1	0	0	2
		4	ADC	MRX+D+ DF→DF,D	MRX	RX	0	1	0	3

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TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (CONT'D)

STATE	OPCODE REG. I	OPCODE REG. N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES[G]
S1	7	5	SDB	MRX−D−DFN→DF,D	MRX	RX	0	1	0	3
		6	SHRC	LSB(D)→DF; DF→MSB(D)	FLOAT	RX	1	1	0	1
		7	SMB	D−MRX−DFN→DF,D	MRX	RX	0	1	0	3
		8	SAV	T→MRX	T	RX	1	0	0	2
		9	MARK	(X,P)→T, MR2; P→X; R2−1→R2	T	R2	1	0	0	2
		A	REQ	0→Q	FLOAT	RP	1	1	0	1
		B	SEQ	1→Q	FLOAT	RP	1	1	0	1
		C	ADCI	MRP+D+DF→DF,D; RP+1	MRP	RP	0	1	0	3
		D	SDBI	MRP−D−DFN→DF,D; RP+1	MRP	RP	0	1	0	3
		E	SHLC	MSB(D)→DF; DF→LSB(D)	FLOAT	RP	1	1	0	1
		F	SMBI	D−MRP−DFN→DF,D; RP+1	MRP	RP	0	1	0	3
	8	0-F	GLO	RN.0→D	RN.0	RN	1	1	0	1
	9	0-F	GHI	RN.1→D	RN.1	RN	1	1	0	1
	A	0-F	PLO	D→RN.0	D	RN	1	1	0	1
	B	0-F	PHI	D→RN.1	D	RN	1	1	0	1
S1#1	C	0-3, 8-B	LONG BRANCH	TAKEN: MRP→B; RP+1→RP	MRP	RP	0	1	0	4
#2				TAKEN: B→RP.1; MRP→RP.0	M(RP+1)	RP+1	0	1	0	4
S1#1				NOT TAKEN: RP+1→RP	MRP	RP	0	1	0	4
#2				NOT TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0	4
S1#1		5	LONG SKIP	TAKEN: RP+1→RP	MRP	RP	0	1	0	4
#2		6 7 C D E		TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0	4
S1#1				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0	4
#2		F		NOT TAKEN: NO OPERATION	MRP	RP	0	1	0	4
S1#1		4	NOP	NO OPERATION	MRP	RP	0	1	0	4
#2				NO OPERATION	MRP	RP	0	1	0	4

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (CONT'D)

STATE	OPCODE REG. I	OPCODE REG. N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES[G]
S1	D	0-F	SEP	N→P	NN	RN	1	1	0	1
	E	0-F	SEX	N→X	NN	RN	1	1	0	1
	F	0	LDX	MRX→D	MRX	RX	0	1	0	3
		1	OR	MRX OR D→D						
		2	AND	MRX AND D→D						
		3	XOR	MRX XOR D→D	MRX	RX	0	1	0	3
		4	ADD	MRX+D→DF,D						
		5	SD	MRX−D→DF,D						
		7	SM	D−MRX→DF,D						
		6	SHR	LSB(D)→DF; 0→MSB(D)	FLOAT	RX	1	1	0	1
		8	LDI	MRP→D; RP+1→RP						
		9	ORI	MRP OR D→D; RP+1→RP						
		A	ANI	MRP AND D→D; RP+1→RP						
		B	XRI	MRP XOR D→D; RP+1→RP	MRP	RP	0	1	0	3
		C	ADI	MRP+D→DF,D; RP+1→RP						
		D	SDI	MRP−D→DF,D; RP+1→RP						
		F	SMI	D−MRP→DF,D; RP+1→RP						
		E	SHL	MSB(D)→DF; 0→LSB(D)	FLOAT	RP	1	1	0	1
S2	DMA IN			BUS→MR0; R0+1→R0	DATA FROM I/O DEVICE	R0	1	0	0	F, 7
	DMA OUT			MR0→BUS; R0+1→R0	MR0	R0	0	1	0	F, 8
S3	INTERRUPT			X,P→T; 0→IE 1→P; 2→X	FLOAT	RN	1	1	0	9
S1	LOAD			IDLE ($\overline{CLEAR}$, $\overline{WAIT}$=0)	M(R0−1)	R0−1	0	1	0	E,3

NOTES:

A. IE=1, TPA, TPB suppressed, state=S1.
B. BUS=0 for entire cycle.
C. Next state always S1.
D. Wait for DMA or INTERRUPT.
E. Suppress TPA, wait for DMA.
F. IN REQUEST has priority over OUT REQUEST.
G. Number refers to machine cycle. See Fig. 14 timing waveforms for machine cycles 1 through 9.

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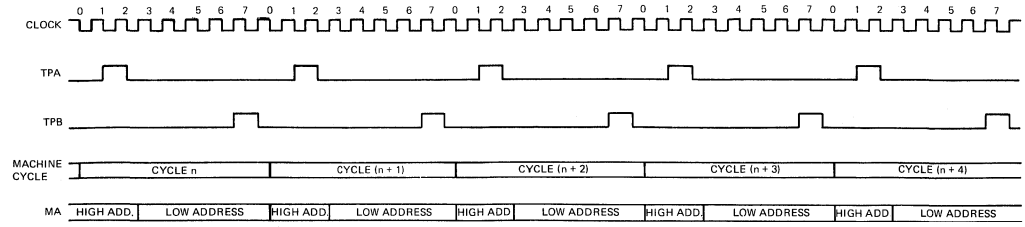
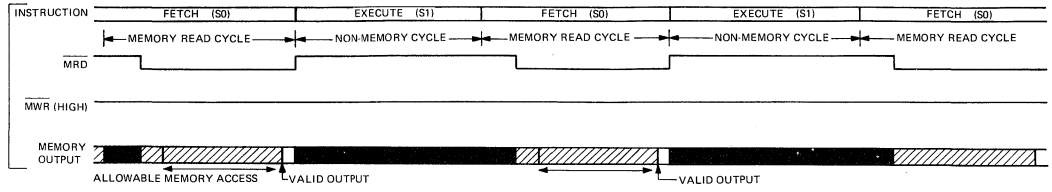
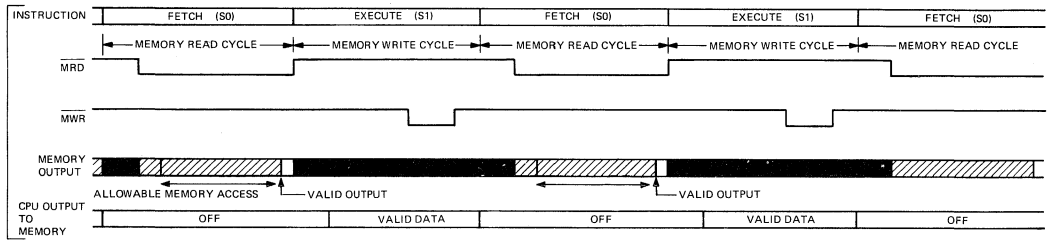


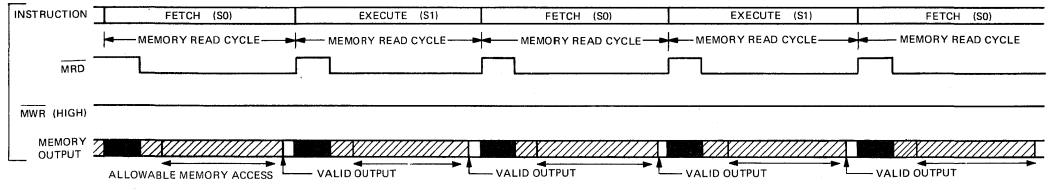
General timing waveforms.



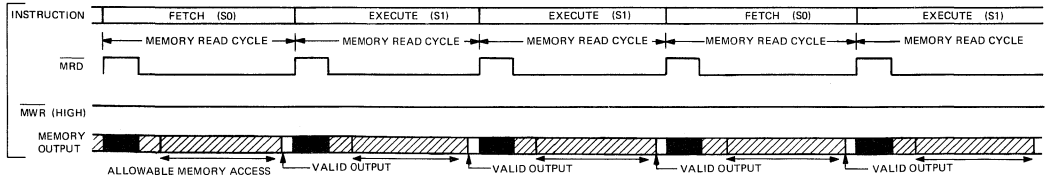
No. 1 Non-memory-cycle timing waveforms.



No. 2 Memory write-cycle timing waveforms.



No. 3 Memory read-cycle timing waveforms.

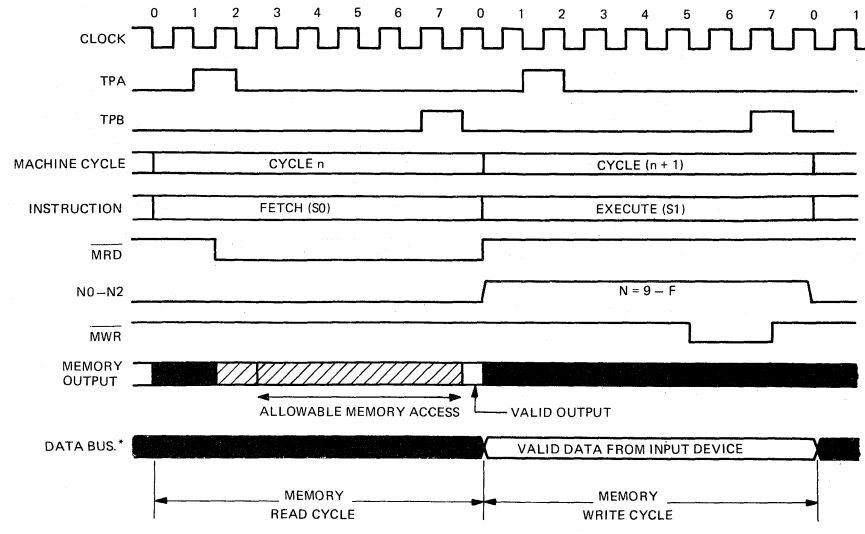


No. 4 Long-branch or long-skip-cycle timing waveforms.

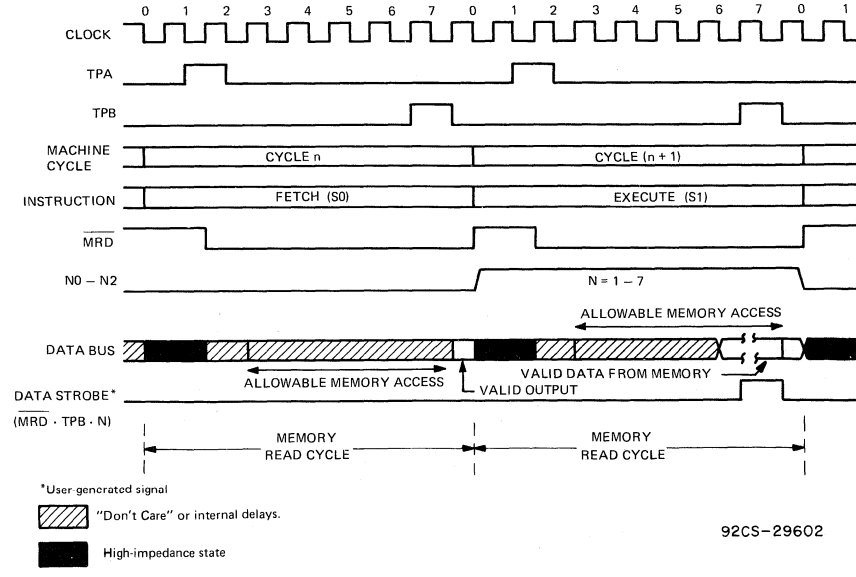
"Don't Care" or internal delays. High-impedance state

92CL-29600

Fig. 14 - Machine-cycle timing waveforms (propagation delays not shown).

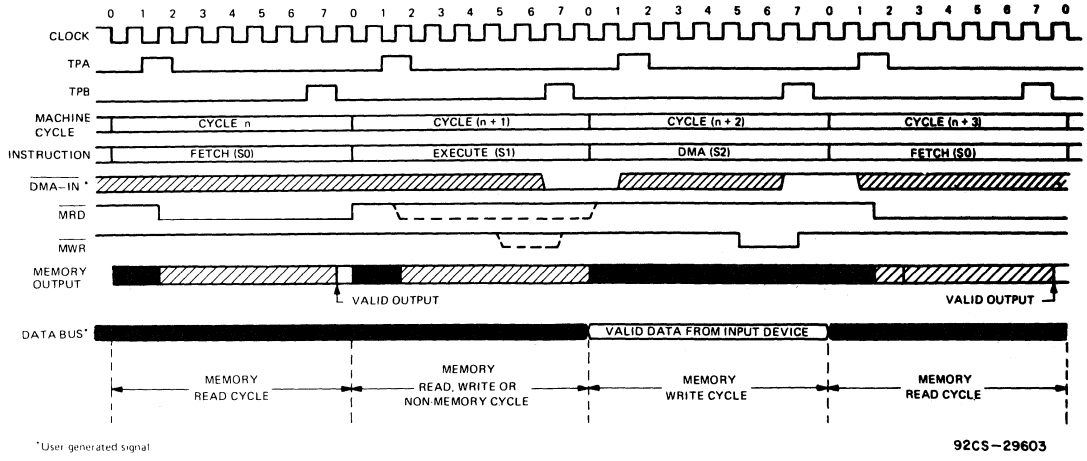


No. 5 Input-cycle timing waveforms.

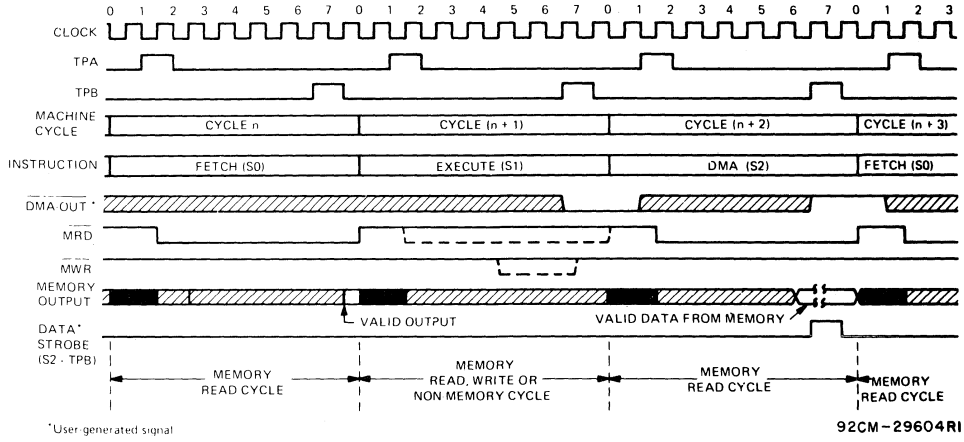


No. 6 Output-cycle timing waveforms.

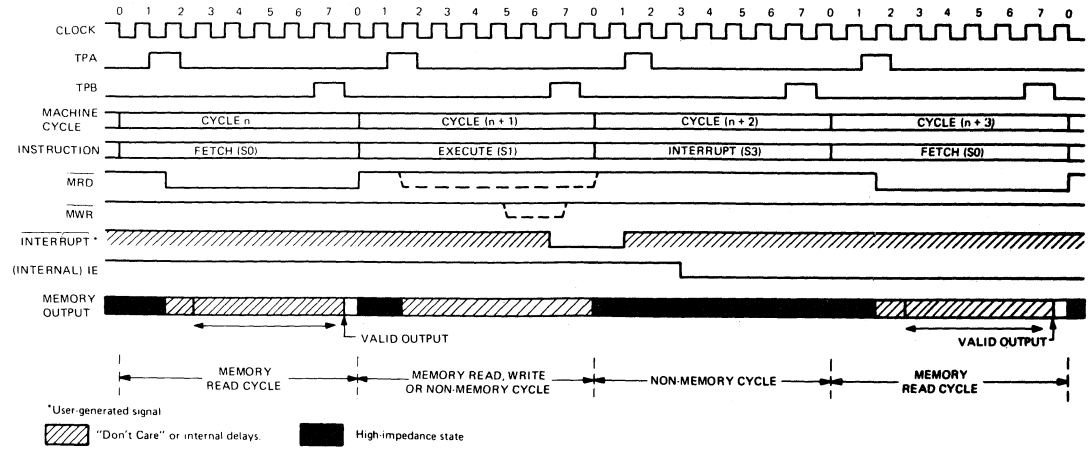
Fig. 14 - Machine-cycle timing waveforms (propagation delays not shown). Continued.



No. 7 DMA-IN-cycle timing waveforms.



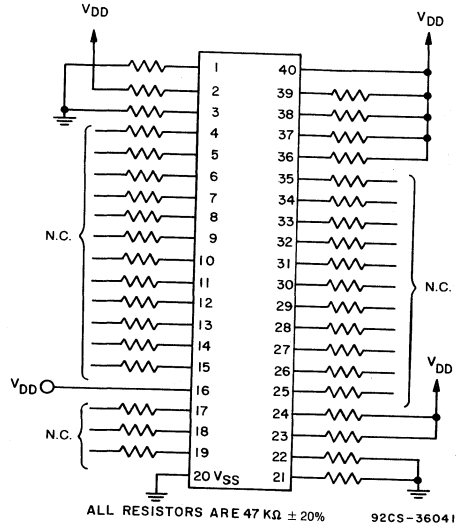
No. 8 DMA-OUT-cycle timing waveforms.



No. 9 INTERRUPT-cycle timing waveforms.

Fig. 14 - Machine-cycle timing waveforms (propagation delays not shown). Continued.

CDP1802A/3, CDP1802AC/3



TYPE	V_{DD}	TEMP	TIME
CDP1802A	11 ± 0.5 V	+ 125°C	160 hrs.
CDP1802AC	7 ± 0.5 V	+ 125°C	160 hrs.

Fig. 15 - Bias/static burn-in circuit.

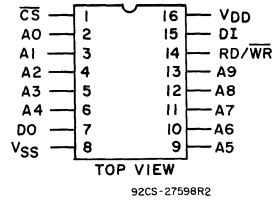
CDP1821C/3

High-Reliability CMOS 1024-Word x 1-Bit Static Random-Access Memory

For Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- *Static CMOS Silicon-On-Sapphire circuitry-CD4000-series compatible*
- *Compatible with CDP1800-series microprocessors at maximum speed*
- *Fast access time: 100 ns typ. at V_{DD}=5 V*
- *Single voltage supply*
- *No precharge or external clocks required*
- *Low quiescent and operating power*
- *Separate data inputs and outputs*
- *High noise immunity-30% of V_{DD}*
- *Memory retention for standby battery voltage down to 2 V at 25°C*
- *Latch-up-free transient-radiation tolerance*



TERMINAL ASSIGNMENT

The RCA-CDP1821C slash(/) series types are 1024-word x 1-bit CMOS silicon-on-sapphire (SOS), fully static, random-access memories designed for use in CDP1800 microprocessor systems. These devices have a recommended operating voltage range of 4 to 6.5 volts. 10-volt versions are available as custom units.

The output state of the CDP1821C slash(/) series types is a function of the input address and chip-select states only. Valid data will appear at the output in one access time following the latest address change to a selected chip. After valid data appears, the address may be changed immediately. It is not necessary to clock the chip-select input or any other input terminal for fully static operation; therefore the chip-select input may be used as an additional address input. When the device is in an unselected state (CS = 1), the internal write circuitry and output sense amplifier are disabled. This feature allows the three-state data outputs from many arrays to be OR-tied to a common bus for easy memory expansion.

The CDP1821C slash(/) series types are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established in MIL-STD-883. The packaged devices are provided to screening level /3 which corresponds to MIL-STD-883 Class B.

The CDP1821C slash(/) series types are supplied in the 16-lead hermetic dual-in-line side-brazed ceramic package (D suffix) that conforms to MIL-M-38510 Case Outline D-2.

CDP1821C/3

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
		+25°C -55°C		+125°C		
		Min.	Max.	Min.	Max.	
Quiescent Device Current, I_{DD}	V_{IN} = 0 V or V_{DD}	—	260•	—	1000•	μA
Output Low Drive (Sink) Current, I_{OL}	V_{OUT} = 0.4 V	2.7•	—	1.6•	—	mA
Output High Drive (Source) Current, I_{OH}	V_{OUT} = V_{DD} -0.4 V	-1.3•	—	-0.8•	—	mA
Output Voltage Low-Level, V_{OL}	—	—	0.1	—	0.5	V
Output Voltage High-Level, V_{OH}	—	V_{DD}-0.1	—	V_{DD}-0.5	—	
Input Low Voltage, V_{IL}	—	—	0.3V_{DD}	—	0.3V_{DD}	V
Input High Voltage, V_{IH}	—	0.7V_{DD}	—	0.7V_{DD}	—	
Input Current, I_{IN}	V_{IN} = 0 V or V_{DD}	—	±2.6•	—	±10•	μA
3-State Output Leakage Current, I_{OUT}	V_{IN} = 0 V or V_{DD}	—	±2.6•	—	±10•	μA
Operating Current, I_{DD1}#	—	—	5	—	10	μA
Input Capacitance, C_{IN}	—	—	7.5	—	7.5	pF
Output Capacitance, C_{OUT}	—	—	15	—	15	

Limits with black dot (•) designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testings.

#Measured with 1-μs read-cycle time and outputs floating.

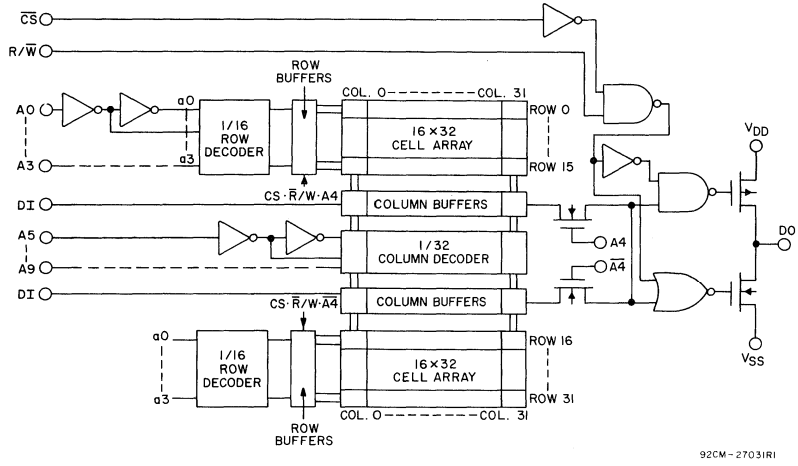


Fig. 1 - Functional block diagram.

OPERATIONAL MODES

MODE	INPUTS		OUTPUT
	READ/ WRITE R/$\overline{W}$	CHIP-SELECT $\overline{CS}$	DATA OUTPUT DO
Standby	X	1	High Impedance
Write	0	0	High Impedance
Read	1	0	Contents of Addressed Call

X=Don't Care Logic 1=High
Logic 0=Low

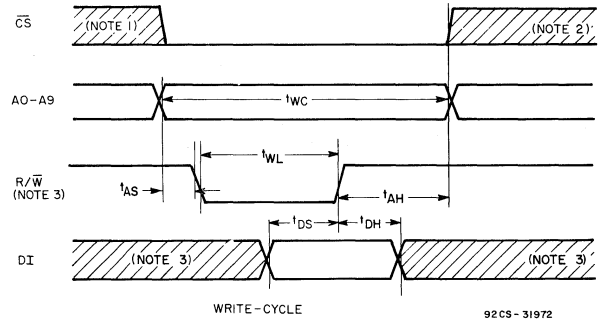
CDP1821C/3

WRITE-CYCLE DYNAMIC ELECTRICAL CHARACTERISTICS

t_r, t_f=10 ns, C_L=50 pF

CHARACTERISTIC	V_{DD} (V)	LIMITS +25°C -55°C Min.	LIMITS +25°C -55°C Max.	LIMITS +125°C Min.	LIMITS +125°C Max.	UNITS
Write-Cycle Time, t_{WC}	5	300	—	420	—	ns
Address Setup Time, t_{AS}	5	60•	—	84•	—	
Address Hold Time, t_{AH}	5	130•	—	180•	—	
Input Data Setup Time, t_{DS}	5	90•	—	125•	—	
Input Data Hold Time, t_{DH}	5	60•	—	84•	—	
Read/$\overline{\text{Write}}$ Pulse Width Low, t_{WL}	5	110•	—	155•	—	

Dot (•) indicates 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.



Note 1: Chip-Select ($\overline{CS}$) permitted to change from high to low level or remain low on a selected device.
Note 2: Chip-Select ($\overline{CS}$) permitted to change from low to high level or remain low.
Note 3: Don't care.

Fig. 2 - Write-cycle timing diagram.

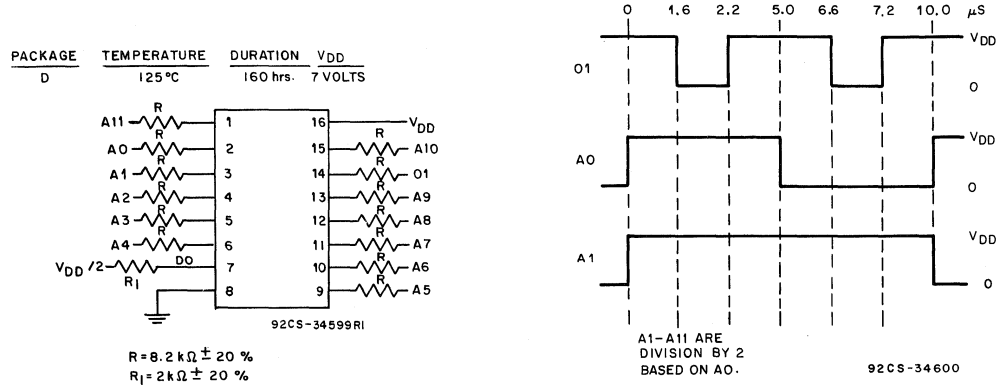


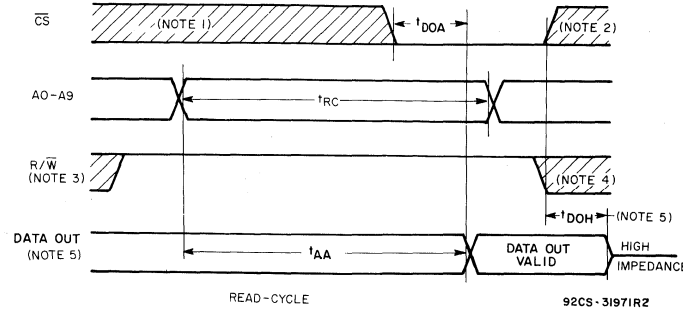
Fig. 3 - Dynamic/operating burn-in circuit and timing diagram.

READ-CYCLE DYNAMIC ELECTRICAL CHARACTERISTICS

t_r,t_f=10 ns, C_L=50 pF

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		+25°C -55°C		+125°C		
		Min.	Max.	Min.	Max.	
Data Access Time, t_{DA}	5	—	190•	—	255•	ns
Read-Cycle Time, t_{RC}	5	190	—	255	—	
Output Enable Time, t_{EN}	5	65	—	90	—	
Output Disable Time, t_{DIS}	5	—	65	—	90	

Dot (•) indicates 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.



Note 1: Chip-Select ($\overline{CS}$) permitted to change from high to low level or remain low on a selected device.
Note 2: Chip-Select ($\overline{CS}$) permitted to change from low to high level or remain low.
Note 3: Read/Write ($R/\overline{W}$) must be at a high level during all address transitions.
Note 4: Don't care.
Note 5: Data-Out (DO) is a high impedance within t_{DIS} ns after the falling edge of R/W or the rising edge of $\overline{CS}$.

Fig. 4 - Read-cycle timing diagram.

DATA RETENTION CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS		-55°C, +25°C		+125°		UNITS
	V_{DR} (V)	V_{DD} (V)	Min.	Max.	Min.	Max.	
Minimum Data Retention Voltage, V_{DR}	—	—	—	2•	—	2.5•	V
Data Retention Quiescent Current, I_{DD}	2	—	—	50•	—	200•	μA
Chip Deselect to Data Retention Time, t_{CDR}	—	5	450	—	650	—	ns
Recovery to Normal Operation Time, t_{RC}	—	5	450	—	650	—	

Dot (•) indicates 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

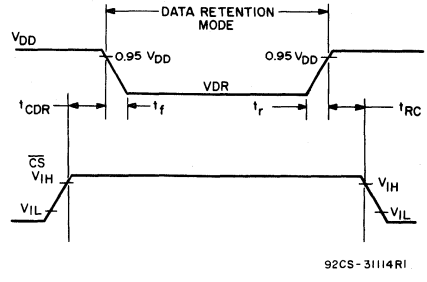


Fig. 5 - Low V_{DD} data retention waveforms and timing diagram.

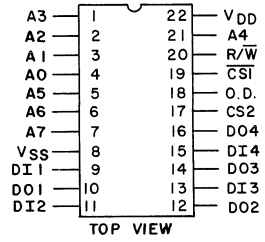
CDP1822C/3

High-Reliability CMOS 256-Word by 4-Bit LSI Static Random-Access Memory

For Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- *Interfaces directly with CDP1802 microprocessor*
- *Very low operating current — 4 mA typ. at V_{DD} = 5 V and cycle time = 1 μs*
- *Static CMOS Silicon-On-Sapphire circuitry — CD4000-series compatible.*
- *Industry standard pinout*
- *Two Chip-Select inputs — simple memory expansion*
- *Memory retention for standby battery voltage of 2 V min.*
- *Single-power-supply operation — 4 to 6.5 V*
- *High noise immunity — 30% of V_{DD} over the range 4 to 6.5 V*
- *Output-Disable for common I/O systems*
- *3-State data output for bus-oriented systems*
- *Separate data inputs and outputs*
- *Latch-up-free transient-radiation tolerance*



TERMINAL ASSIGNMENTS

The RCA-CDP1822C Slash(/) Series types are 256-word by 4-bit random-access memories designed for use in memory systems where high speed, low operating current, and simplicity in use are desirable. The CDP1822 features high speed and excellent noise immunity. These types have separate data inputs and outputs and utilizes a single power supply of 4 to 6.5 volts. 10 volt versions are available as custom parts.

Two Chip-Select inputs simplify system expansion. An Output Disable control provides Wire-OR- capability and is also useful in common Input/Output systems. The Output Disable input allows this RAM to be used in common data Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input condition. The output assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or CS2.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5-V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

These devices are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established in MIL-STD-883. The packaged types can be provided to screening level /3, which corresponds to MIL-STD-883 Class B.

The CDP1822C Slash(/) Series types are supplied in the 22-lead hermetic dual-in-line side-brazed ceramic package (D Suffix) that meets the specifications of MIL-M-38510 Case outline D-7.

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	$\overline{\text{Chip Select 1}}$ $\overline{CS_1}$	Chip Select 2 CS_2	Output Disable OD	Read/$\overline{\text{Write}}$ R/$\overline{W}$	
READ	0	1	0	1	Read
WRITE	0	1	0	0	Data in
WRITE	0	1	1	0	High Impedance
STANDBY	1	X	X	X	High Impedance
STANDBY	X	0	X	X	High Impedance
OUTPUT DISABLE	X	X	1	X	High Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

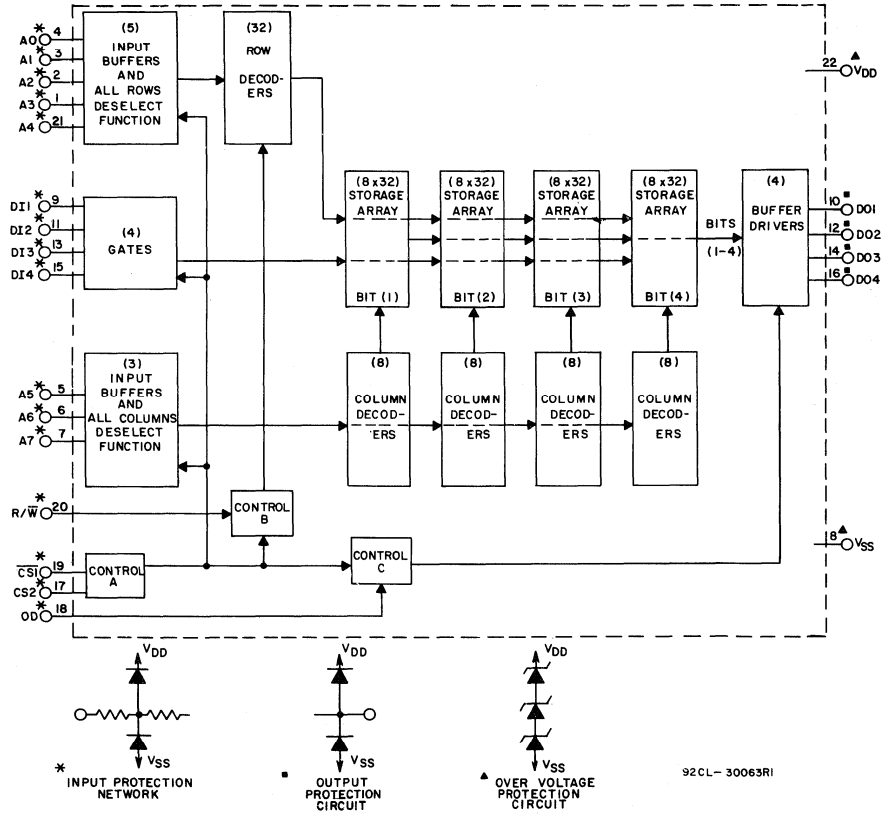


Fig. 1 — Functional block diagram for CDP1822CD/...

CDP1822C/3

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS				UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Temp. -55°C, +25°C		Temp. +125°C		
				Min.	Max.	Min.	Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	—	390•	—	1000•	μA
Output Low Drive (Sink) Current, I_{OL} Min.	0.4	0,5	5	2.6•	—	1.6•	—	mA
Output High Drive (Source) Current, I_{OH} Min.	4.6	0,5	5	—	−1.2•	—	−0.8•	mA
Output Voltage Low-Level V_{OL} Max.	—	0.5	5	—	0.1	—	0.5	V
Output Voltage High Level, V_{OH} Min.	—	0.5	5	V_{DD} -0.1	—	V_{DD} -0.5	—	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	—	5	—	0.3 V_{DD}	—	0.3 V_{DD}	V
Input High Voltage, V_{IH} Min.	0.5, 4.5	—	5	0.7 V_{DD}	—	0.7 V_{DD}	—	
Input Current, I_{IN} Max.	—	0,5	5	—	±3.2•	—	±10•	μA
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	—	±3.2•	—	±19•	μA
Operating Current, I_{DD1}	—	0,5	5	—	6.5	—	10	mA
Input Capacitance, C_{IN}	—	—	—	—	7.5	—	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	7.5	—	7.5	

Limits with black dot (•) designate 100% testing, all other limits are designer's parameters under given test conditions and do not represent 100% testing.

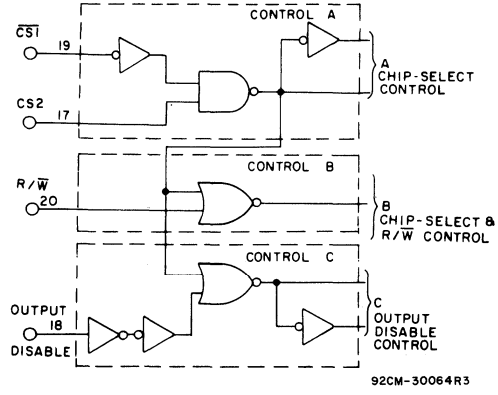


Fig. 2 — Logic diagram of controls for CDP1822CD.

READ CYCLE DYNAMIC ELECTRICAL CHARACTERISTICS

t_r, t_f = 10 ns, C_L = 50 pF

CHARACTERISTIC	V_{DD} (V)	LIMITS +25°C -55°C Min.	LIMITS +25°C -55°C Max.	LIMITS +125°C Min.	LIMITS +125°C Max.	UNITS
Read Cycle ..... t_{RC}	5	370•	—	500•		ns
Access from Address ..... t_{ADA}	5	—	370•	—	500•	ns
Output Valid from $\overline{\text{Chip-Select 1}}$ ..... t_{DOA1}	5	—	370•	—	500•	ns
Output Valid from Chip-Select 2 ..... t_{DOA2}	5	—	370•	—	500•	ns
Output Active from Output Disable..... t_{DOA3}	5	—	170•	—	225•	ns
Output Hold from $\overline{\text{Chip-Select 1}}$ ..... t_{DOH1}	5	10	—	20	—	ns
Output Hold from Chip-Select 2 ..... t_{DOH2}	5	10	—	20	—	ns
Output Hold from Output Disable..... t_{DOH3}	5	10	—	20	—	ns

Limits with black dot (•) designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

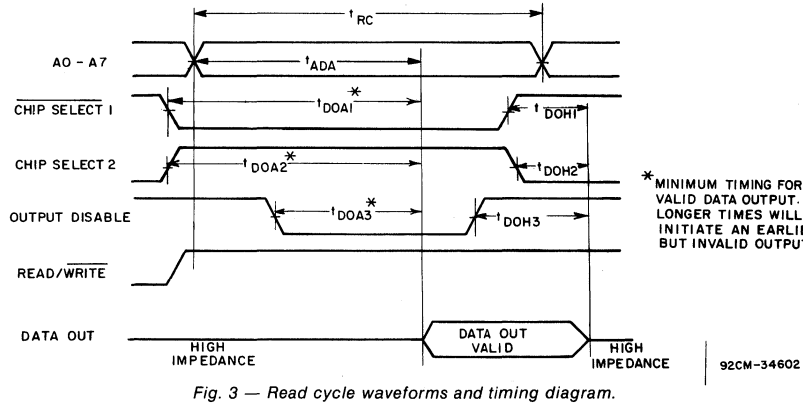


Fig. 3 — Read cycle waveforms and timing diagram.

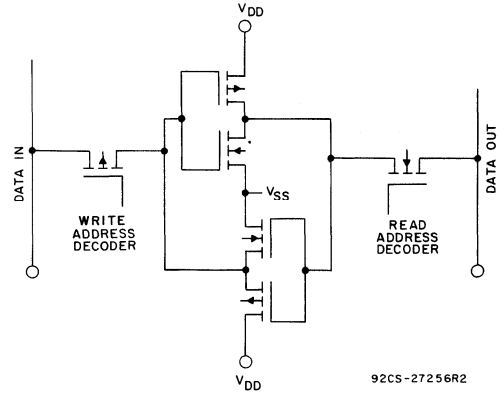


Fig. 4 — Memory cell configuration.

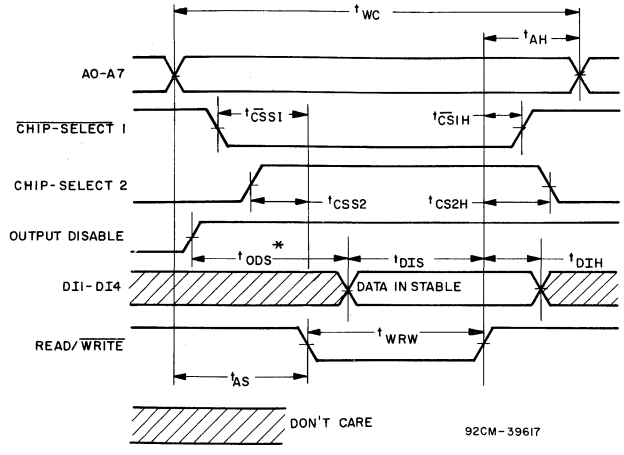
CDP1822C/3

WRITE CYCLE DYNAMIC ELECTRICAL CHARACTERISTICS

t_r, t_f = 10 ns C_L = 50 pF

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			+25°C, -55°C		+125°C		
			Min.	Max.	Min.	Max.	
Write Cycle	t_{WC}	5	400•	—	560•	—	ns
Address Setup	t_{AS}	5	160•	—	225•	—	ns
Address Hold	t_{AH}	5	40•	—	55•	—	ns
Write Pulse Width	t_{WRW}	5	200•	—	280•	—	ns
Data in Setup	t_{DIS}	5	200•	—	280•	—	ns
Data in Hold	t_{DIH}	5	40•	—	55•	—	ns
$\overline{\text{Chip-Select}}$ 1 Setup	$t_{\overline{CS}S1}$	5	200	—	280	—	ns
Chip-Select 2 Setup	t_{CSS2}	5	200	—	280	—	ns
Output Disable Setup	t_{ODS}	5	140	—	225	—	ns

Limits with black dot (•) designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.



* t_{ODS} IS REQUIRED FOR COMMON I/O OPERATION ONLY; FOR SEPARATE I/O OPERATIONS, OUTPUT DISABLE IS DON'T CARE

Fig. 5 — Write cycle timing waveforms.

DATA RETENTION CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS		LIMITS				UNITS
			+25°C -55°C		+125°C		
	V_{DR} (V)	V_{DD} (V)	Min.	Max.	Min.	Max.	
Min. Data Retention Voltage, V_{DR}	—	—	—	2•	—	2.5•	V
Data Retention Quiescent Current, I_{DD}	2	—	—	70•	—	380•	μA
Chip Deselect to Data Retention Time, t_{CDR}	—	5	450	—	650	—	ns
	—	10					
Recovery to Normal Operation Time, t_{RC}	—	5	450	—	650	—	

Limits with black dot (•) designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

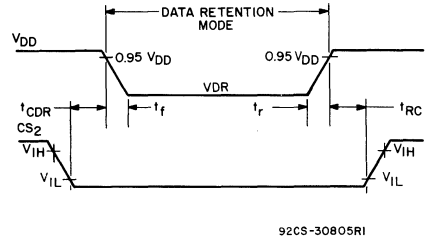


Fig. 6 — Low V_{DD} data retention timing waveforms.

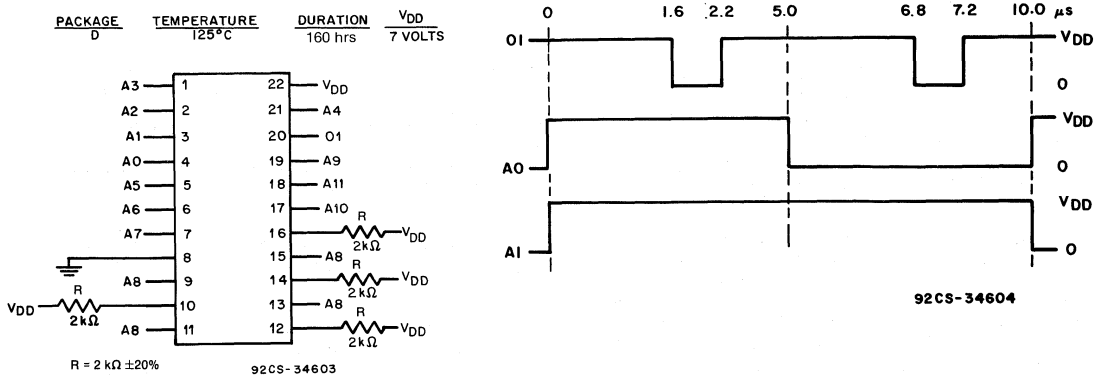


Fig. 7 — Dynamic/operating burn-in circuit and timing diagram.

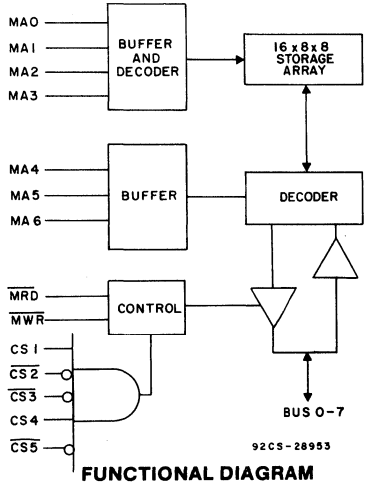
CDP1823C/3

High-Reliability CMOS 128-Word x 8-Bit Static Random-Access Memory

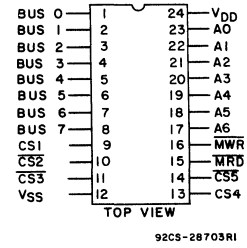
For Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- *Compatible with CDP1800-series microprocessors at maximum speed*
- *Interfaces with CDP1800-series microprocessors without additional components*
- *Fast access time: 275 ns typ. at V_{DD} = 5 V, 25° C*
- *Single voltage supply*
- *Common data inputs and outputs*
- *Multiple-chip select inputs to simplify memory system expansion*
- *High noise immunity -30% of V_{DD}*
- *Memory retention for standby battery voltage down to 2 V at 25° C*
- *Latch-up-free transient-radiation tolerance*



FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENT

The RCA-CDP1823C Slash(/) Series types are 128-word x 8-bit CMOS/SOS static random-access memories. These memories are compatible with the CDP1802, CDP1804, CDP1805, and CDP1806 microprocessors, and will interface directly without additional components. The CDP1823C has a recommended operating voltage range of 4 to 6.5 volts. A 10-volt version is available as a custom device.

The CDP1823C memory has 8 common data input and data output terminals for direct connection to a bidirectional data bus and is operated from a single voltage supply. Five chip-select inputs are provided to simplify memory-system expansion. In order to enable the CDP1823C, the chip-select inputs $\overline{CS2}$, $\overline{CS3}$, and $\overline{CS5}$ require a low input signal, and the chip-select inputs CS1 and CS4 require a high input signal.

The $\overline{MRD}$ signal enables all 8 output drivers when in the low state and should be in a high state during a write cycle.

After valid data appear at the output, the address inputs may be changed immediately. Output data will be valid until either the $\overline{MRD}$ signal goes high, the device is deselected, or t_{AA} (access time) after address changes.

The CDP1823C Slash(/) Series types are supplied in hermetic 24-lead dual-in-line side-brazed ceramic packages (D suffix) that meet the specifications of Mil-M-38510 Case Outline D3.

These devices are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established in MIL-STD-883. The packaged types can be supplied to screening level /3, which corresponds to MIL-STD-883 Class B.

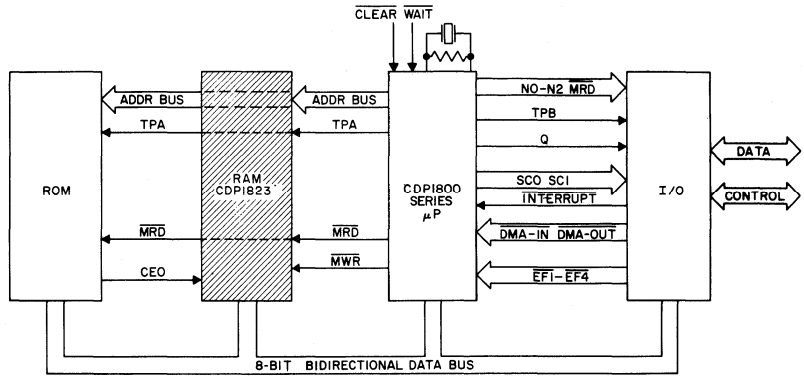


Fig. 1 - Typical CDP1802 microprocessor system. 92CM-28954RI

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%

CHARACTERISTIC		CONDITIONS			LIMITS				UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	+25°C -55°C MIN.	+25°C -55°C MAX.	+125°C MIN.	+125°C MAX.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	270•	—	1000•	μA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	2.7•	—	1.5•	—	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	—	-1.3•	—	-0.7•	mA
Output Voltage Low-Level	V_{OL}	—	0, 5	5	—	0.1	—	0.1	V
Output Voltage High-Level	V_{OH}	—	0,5	5	V_{DD} -0.1	—	V_{DD}-0.1	—	V
Input Low Voltage	V_{IL}	0.5, 4.5	—	5		0.3 V_{DD}•	—	0.3 V_{DD}•	V
Input High Voltage	V_{IH}	0.5, 4.5	—	5	0.7V_{DD}•	—	0.7V_{DD}•	—	V
Input Current	I_{IN}	—	0, 5	5	—	±2.6•	—	±10•	μA
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	—	±2.6•	—	±10•	μA
Operating Current	I_{DD1}	0, 5	0, 5	5	—	5	—	10	mA
Input Capacitance	C_{IN}	—	—	—	—	7.5	—	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	15	—	15	pF

Limits with black dot (•) designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

CDP1823C/3

READ-CYCLE DYNAMIC ELECTRICAL CHARACTERISTICS

t_r, t_f = 10 ns, C_L = 50 pF

CHARACTERISTIC		VDD (V)	LIMITS				UNITS
			+25°C -55°C		+125°C		
			MIN.	MAX.	MIN.	MAX.	
Access Time From Address Change	t_{AA}	5	—	360•	—	505•	ns
Read Cycle Time	t_{RC}	5	360	—	505	—	
Access Time From Chip Select	t_{AC}	5	—	360	—	505	
Access Time From $\overline{MRD}$	t_{AM}	5	—	310•	—	435•	ns
Data Hold Time After Read	t_{DH}	5	50	—	70	—	

Limits with black dot (•) designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

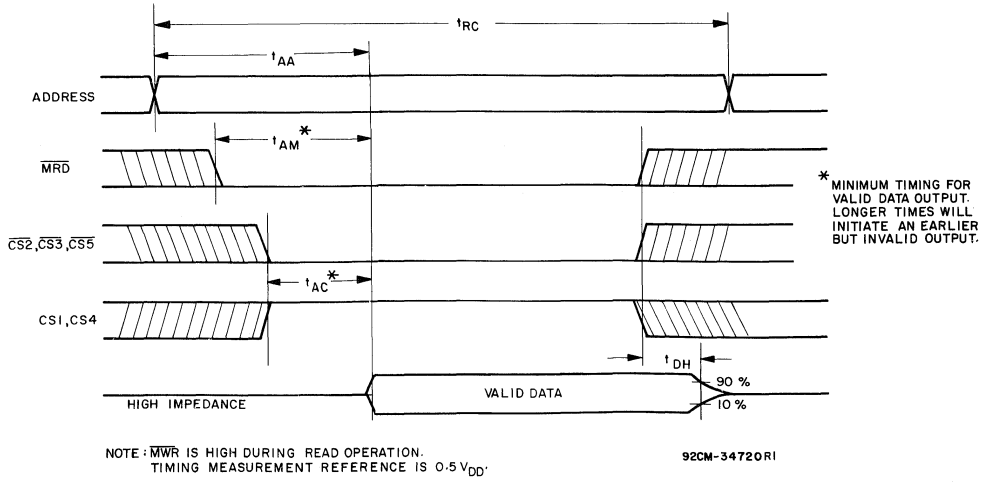


Fig. 2 - Read cycle timing diagram.

WRITE-CYCLE DYNAMIC ELECTRICAL CHARACTERISTICS
t_r, t_f = 10 ns, C_L = 50 pF

CHARACTERISTIC		VDD (V)	LIMITS +25°C -55°C MIN. †	+25°C -55°C MAX.	+125°C MIN. †	+125°C MAX.	UNITS
Write Cycle	t_{WC}	5	280	—	400	—	ns
Write Pulse Width	t_{WW}	5	140•	—	200•	—	
Chip Select Setup Time	$t_{\overline{CS}}$	5	210	—	300	—	
Address Setup Time	t_{AS}	5	70•	—	100•	—	
Address Hold Time	t_{AH}	5	70	—	100	—	
Data to $\overline{MWR}$ Setup Time	t_{DS}	5	70•	—	100•	—	
Data Hold Time From $\overline{MWR}$	t_{DH}	5	50•	—	70•	—	

† Minimum timing to allow the indicated function to occur.

Limits with black dot (•) designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

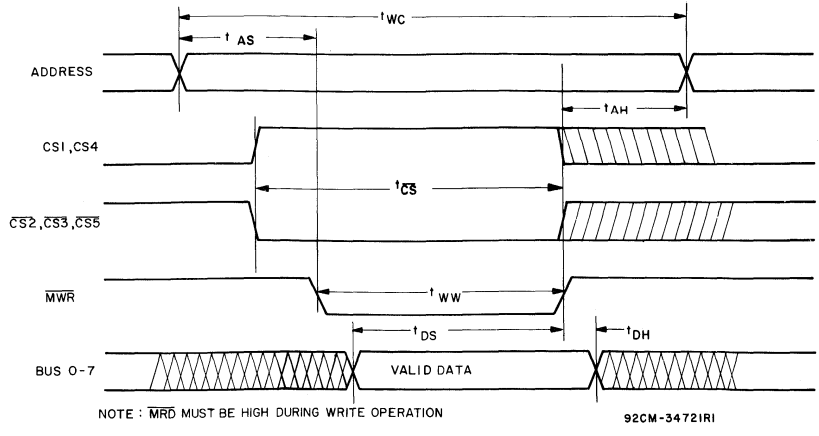


Fig. 3 - Write cycle timing diagram.

CDP1823C/3

OPERATIONAL MODES

Function	$\overline{MRD}$	$\overline{MWR}$	CS1	$\overline{CS2}$	$\overline{CS3}$	CS4	$\overline{CS5}$	Bus Terminal State
READ	0	X	1	0	0	1	0	Storage State of Addressed Word
WRITE	1	0	1	0	0	1	0	Input High-Impedance
STAND-BY	1	1	1	0	0	1	0	High-Impedance
NOT SELECTED	X	X	0	X	X	X	X	High-Impedance
	X	X	X	1	X	X	X	
	X	X	X	X	1	X	X	
	X	X	X	X	X	0	X	
	X	X	X	X	X	X	1	

Logic 1 = High Logic 0 = Low X = Don't Care

DATA RETENTION CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS V_{DR} (V)	TEST CONDITIONS V_{DD} (V)	-55°C, +25°C MIN.	-55°C, +25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS
Min. Data Retention Voltage	V_{DR}	—	—	—	2•	—	2.5•	V
Data Retention Quiescent Current	I_{DD}	2	—	—	100	—	400	μA
Chip Deselect to Data Retention Time	t_{CDR}	—	5	450	—	650	—	ns
Recovery to Normal Operation Time	t_{RC}	—	5	450	—	650	—	ns

Limits with black dot (•) designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

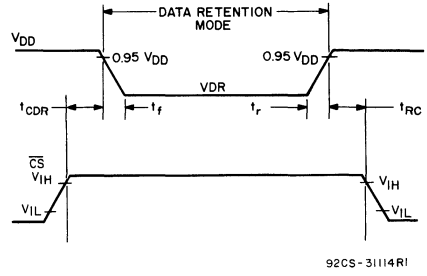


Fig. 4 - Low V_{DD} data retention waveforms.

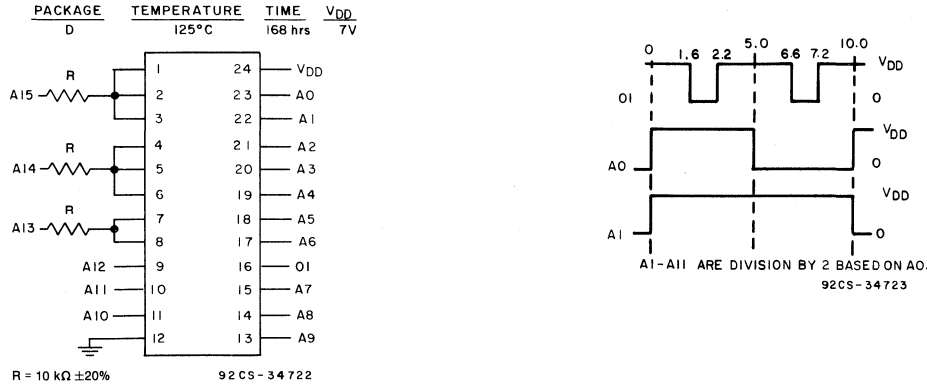


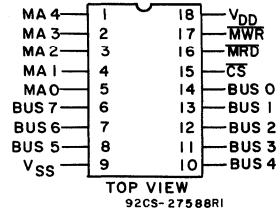
Fig. 5 - Dynamic/operating burn-in circuit and timing diagram.

CDP1824/3, CDP1824C/3

High-Reliability CMOS 32-Word x 8-Bit Static Random-Access Memory

Features:

- *Access time:*
  610 ns at V_{DD} = 5 V;
  320 ns at V_{DD} = 10 V
- *No precharge or clock required*



TERMINAL ASSIGNMENT

The RCA-CDP1824/3 and CDP1824C/3 types are high-reliability CMOS 32-word x 8 bit fully static random-access memories for use in CDP1800 series microprocessor systems. These parts are compatible with the CDP1802 microprocessor and will interface directly without additional components.

The CDP1824/3 is fully decoded and does not require a precharge or clocking signal for proper operation. It has common input and output and is operated from a single voltage supply. The $\overline{MRD}$ signal (output disable control) enables the three-state output drivers, and overrides the $\overline{MWR}$ signal. A $\overline{CS}$ input is provided for memory expansion.

The CDP1824C/3 is functionally identical to the CDP1824/3. The CDP1824/3 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1824C/3 has an operating voltage range of 4 to 6.5 volts.

The CDP1824/3 and CDP1824C/3 are supplied in 18-lead, dual-in-line side-brazed ceramic packages (D suffix) that conform to the requirements and dimensions specified in MIL-M-38510 Case Outline D-6. Other package styles may be available on a special order basis.

OPERATIONAL MODES

FUNCTION	$\overline{CS}$	$\overline{MRD}$	$\overline{MWR}$	DATA PINS STATUS
READ	0	0	X	Output: High/Low Dependent on Data
WRITE	0	1	0	Input: Output Disabled
Not Selected	1	X	X	Output Disabled: High-Impedance State
Standby	0	1	1	

Logic 1 = High Logic 0 = Low X = Don't Care

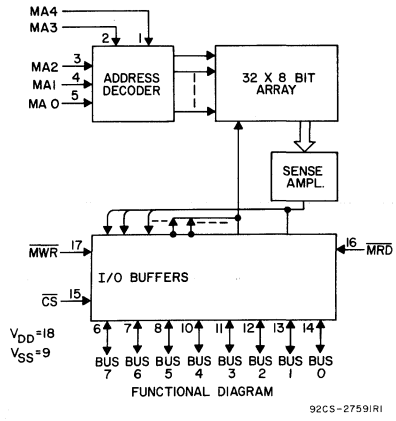
CDP1824/3, CDP1824C/3

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS			LIMITS				UNITS
					+25/-55°C		+125°C		
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current,		—	0, 5	5	—	50	—	500	μA
Note 1	I_{DD}	—	0, 10	10	—	500	—	1000	
Output Voltage: Note 2		—	0, 5	5	—	0.1	—	0.2	V
Low Level	V_{OL}	—	0, 10	10	—	0.1	—	0.2	
High Level	V_{OH}	—	0, 5	5	4.9	—	4.8	—	
		—	0, 10	10	9.9	—	4.8	—	
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	1.5	—	1.5	
		1, 9	—	10	—	3	—	—	
Input High Voltage	V_{IH}	0.5, 4.5	—	5	3.5	—	3.5	—	
		1,9	—	10	7	—	7	—	
Output Low (Sink) Current	I_{OL}	0.4	0, 5	5	2	—	1.5	—	mA
		0.5	0, 10	10	4	—	2.9	—	
Output High (Source) Current	I_{OH}	4.6	0, 5	5	—	-1	—	-0.75	
		9.5	0, 10	10	—	-2	—	-1.5	
Input Current	I_{IN}	Any	0, 5	5	—	±1	—	±5	μA
		Input	0, 10	10	—	±1	—	±5	
3-State Output Leakage	I_{OUT}	0, 5	0, 5	5	—	±2	—	±5	
Current		0, 10	0, 10	10	—	±2	—	±5	
Input Capacitance	C_{IN}	Note 2			—	10	—	10	pF
Output Capacitance	C_{OUT}	Note 2			—	15	—	15	

Note 1: The CDP1824C/3 meets all 5-volt Static Electrical Characteristics of the CDP1824/3 except Quiescent Device Current for which the limits are I_{DD} = 200 μA at +25/-55°C; I_{DD} = 1000 μA at +125°C.

Note 2: Guaranteed, but not tested.

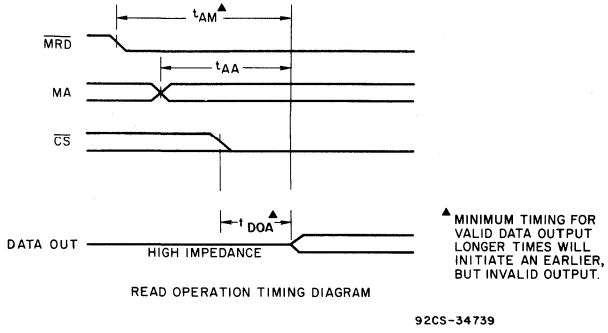


Functional diagram.

CDP1824/3, CDP1824C/3

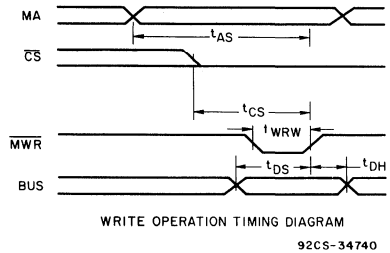
DYNAMIC ELECTRICAL CHARACTERISTICS, Input t_r, $t_f \leq 15$ ns, $C_L = 50$ pF

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25°C/-55°C		+125°C		
Read Operation		V_{DD} (V)	MIN.	MAX.	MIN.	MAX.	
Access Time From Address Change	t_{AA}	5	—	610	—	825	ns
		10	—	320	—	375	
Access Time From Chip Select	t_{DOA}	5	—	610	—	825	
		10	—	320	—	375	
Output Active From $\overline{MRD}$	t_{AM}	5	—	610	—	825	
		10	—	320	—	375	



▲MINIMUM TIMING FOR VALID DATA OUTPUT LONGER TIMES WILL INITIATE AN EARLIER, BUT INVALID OUTPUT.

Read cycle timing diagram.



Write cycle timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS, Input t_r, $t_f \leq 15$ ns, $C_L = 50$ pF

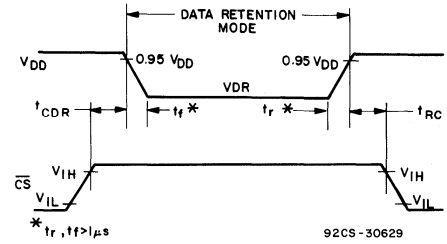
CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25°C/-55°C		+125°C		
Write Operation		V_{DD} (V)	MIN.†	MAX.	MIN.†	MAX.	
Write Pulse Width	t_{WRW}	5	350	—	475	—	ns
		10	180	—	220	—	
Data Setup Time	t_{DS}	5	400	—	560	—	
		10	190	—	260	—	
Data Hold Time	t_{DH}	5	70	—	90	—	
		10	35	—	45	—	
Chip Select Setup Time	t_{CS}	5	550	—	775	—	
		10	340	—	475	—	
Address Setup Time	t_{AS}	5	550	—	775	—	
		10	340	—	475	—	

† Time required by a device to allow for the indicated function.

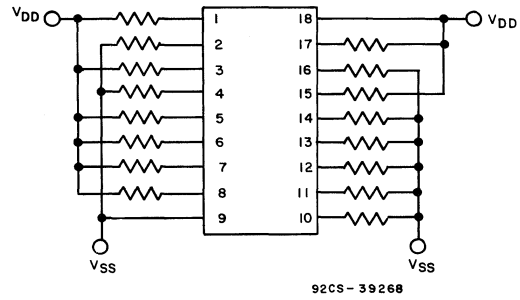
CDP1824/3, CDP1824C/3

DATA RETENTION CHARACTERISTICS at T_A = +25° C

CHARACTERISTIC		TEST CONDITIONS		CDP1824/3		CDP1824C/3		UNITS
			V_{DD} (V)	MIN.	MAX.	MIN.	MAX.	
Data Retention Voltage	V_{DR}	—	—	2.5	—	2.5	—	V
Data Retention Quiescent Current	I_{DD}	V_{DR} = 2.5 V	—	—	10	—	40	μA
Chip Deselect to Data Retention Time	t_{CDR}	V_{DR} = 2.5 V	5	600	—	600	—	ns
			10	300	—	—	—	
Recovery to Normal Operation Time	t_{RC}	V_{DR} = 2.5 V	5	600	—	600	—	
			10	300	—	—	—	



Low V_{DD} data retention waveforms and timing diagram.



ALL RESISTORS 47 kΩ (±20%)

TYPE	V_{DD}	TEMP.	TIME
CDP1824	11 V ± 0.5 V	+125° C	160 Hrs, Min.
CDP1824C	7 V ± 0.5 V	+125° C	160 Hrs, Min.

Static burn-in circuit.

CDM5114CD/3

Advance Information/ Preliminary Data

High-Reliability, CMOS 1024-Word By 4-Bit Static RAM

Features:
- *Single power supply: 4.5 V to 6.5 V*
- *Low standby and operating power*
- *All inputs and outputs TTL compatible*
- *Common data inputs and outputs*
- *Fully static operation*
- *3-state output*
- *Industry-standard 18-pin DIL weld seal*
- *Also available in 24-contact LCC*
- *Latch-up free*
- *Operation in radiation environment*

The RCA-CDM5114CD/3 is a high-reliability 1024-word by 4-bit static random-access memory using CMOS/SOS technology. It is designed for use in memory systems where low power and simplicity in use are desirable. TTL compatibility on all I/O terminals permits easy system integration.

CMOS/SOS technology permits operation in transient radiation environments. It is insensitive to neutrons, cannot latch up at any dose rate and is resistant to single-event upset caused by cosmic rays or heavy ions.

The CDM5114CD/3 is available in an industry-standard pinout configuration, 18-lead ceramic dual-in-line side-brazed package weld seal (D suffix), that conforms to the requirements and dimensions specified in MIL-38510 Case Outline D-6. The part is also available in a 24-contact leadless chip carrier (J suffix).

OPERATIONAL MODES			
FUNCTION	$\overline{CS}$	$\overline{WE}$	**DATA PINS**
Read	0	1	Output: Dependent on Data
Write	0	0	Input
Not Selected	1	X	High-Impedance

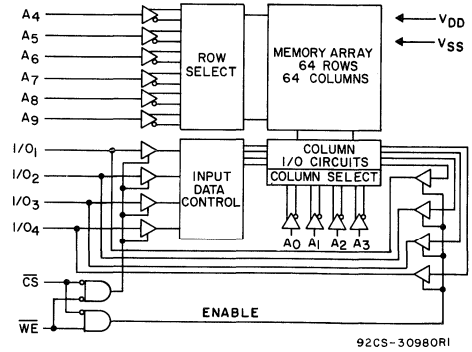


Fig. 1 - Functional block diagram for CDM5114CD/3.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR DIC PACKAGES:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%

CHARACTERISTIC		CONDITIONS	LIMITS				UNITS
			-55° C, +25° C		+125° C		
			Min.	Max.	Min.	Max.	
Quiescent Device Current	I_{DD}	V_{IN}=0 V or V_{DD}, $V_{\overline{CS}} = V_{DD}$	—	0.1•	—	1•	mA
Operating Device Current	I_{DD1}*	Outputs open circuited: cycle time = 1 μs	—	5•	—	6•	
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	2.6•	—	1.7•	—	
Output (Source) Current	I_{OH}	$V_{OUT} = V_{DD}$ -0.4 V	—	-1.8•	—	1.1•	
Output Voltage Low Level	V_{OL}	—	—	0.1	—	0.2	V
Output Voltage High Level	V_{OH}	—	V_{DD} -0.1 V	—	V_{DD} -0.2 V	—	
Input Low Voltage	V_{IL}	—	—	0.8•	—	0.8•	
Input High Voltage	V_{IH}	—	$V_{DD}/2$•	—	$V_{DD}/2$•	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{DD}	—	±2•	—	±10•	μA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0 V or V_{DD}	—	±5•	—	±50•	
Input Capacitance	C_{IN}	—	—	5	—	5	pF
Output Capacitance	C_{OUT}	—	—	7	—	7	

•Limit with black dot (•) designates actual measurement, all other limits are designer's parameters under given test conditions.
*Operating current measured using 1-MHz cycle and C_L = 50 pF.

DYNAMIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%, C_L = 50 pF, $V_{OL} = V_{DD}/2$, $V_{OH} = V_{DD}/2$

CHARACTERISTIC		LIMITS				UNITS
		-55° C, +25° C		+125° C		
		Min.	Max.	Min.	Max.	
Read-Cycle Times (Fig. 2)						
Read Cycle	t_{AVAV}	200	—	250	—	ns
Access	t_{AVQV}	—	200•	—	250•	
Chip Selection to Output Valid	t_{SLQV}	—	160•	—	200•	
Chip Selection to Output Active	t_{SLQA}	20	—	20	—	
Output 3-State from Deselection	t_{SHQZ}	—	100	—	140	
Output Hold from Address Change	t_{AVQZ}	30	—	60	—	
Write-Cycle Times (Fig. 3)						
Write Cycle	t_{AVAV}	200•	—	250•	—	ns
Write Pulse Width	t_{WLWH}*	125•	—	150•	—	
Address Hold Time from Write Enable	t_{WHAV}	50•	—	50•	—	
Address to Write Set-up Time	t_{AVWL}	25•	—	50•	—	
Chip Select Pulse Width	t_{SLSH}*	150•	—	200•	—	
Chip Select to Write Set-up Time	t_{SLWH}	150•	—	200•	—	
Data to Write Set-up Time	t_{DVWH}	75•	—	85•	—	
Data Hold from Write	t_{WHDX}	30•	—	30•	—	

•Limit with black dot (•) designates actual measurement, all other limits are designer's parameters under given test conditions.
*$\overline{CS}$ and $\overline{WE}$ must overlap for at least t_{WLWH} min. t_{DVWH} min. must occur during this overlap.

CDM5114CD/3

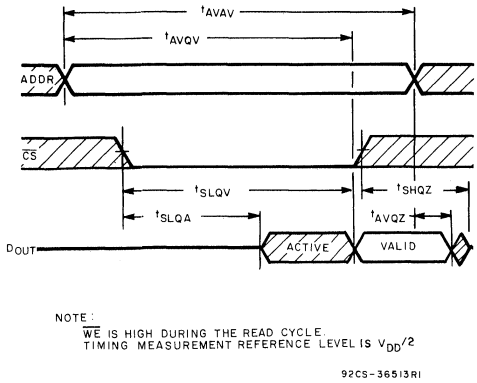


Fig. 2 - Read-cycle timing waveforms.

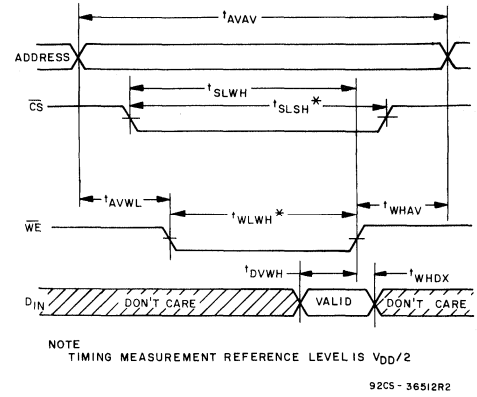


Fig. 3 - Write-cycle timing waveforms.

DATA RETENTION CHARACTERISTICS; See Fig. 4

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			-55°C, +25°C		+125°C		
		V_{DD} (V)	Min.	Max.	Min.	Max.	
Minimum Data Retention Voltage	V_{DR}	—	—	2•	—	2.5•	V
Data Retention Quiescent Current	$I_{DD}DR$	2	—	50•	—	500•	μA
V_{DD} to V_{DR} Rise and Fall Time	t_r, t_f	5	1	—	1	—	μs

•Limit with black dot (•) designates actual measurement, all other limits are designer's parameters under given test conditions.

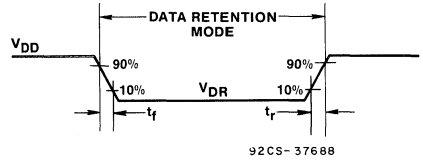
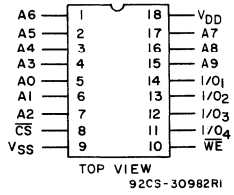


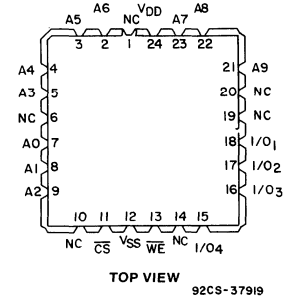
Fig. 4 - Low V_{DD} data retention timing waveforms.

TERMINAL ASSIGNMENTS

D-Suffix Package
(18-Lead, Ceramic Dual-In-Line Side-Brazed)

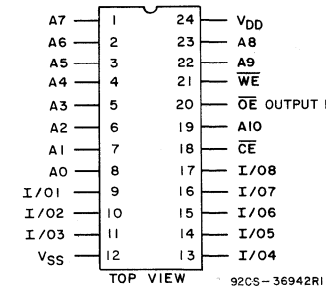


J-Suffix Package
(24-Contact Leadless Chip Carrier)



High-Reliability CMOS 2048-Word by 8-Bit Static RAM

Features:
- *Fully static operation*
- *Single power supply: 4.5 to 5.5 V*
- *All inputs and outputs directly TTL compatible*
- *3-state outputs*
- *Industry standard 24-pin configuration*
- *Chip-enable gates address buffers for minimum standby current*
- *Tested to meet the electrical, mechanical and environmental /3 screening*



TERMINAL ASSIGNMENT

The RCA-CDM6116ACD/3 is a CMOS 2048-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This device has common data inputs and data outputs and utilizes a single power supply of 4.5 to 5.5 V. A chip-enable input and an output-enable input are provided for memory expansion and output buffer control.

The chip enable (CE) gates the address and output buffers and powers down the chip to the low power standby mode.

The output enable ($\overline{OE}$) controls the output buffers to eliminate bus contention.

The CDM6116ACD/3 has an operating temperature range of -55° to +125° C.

The CDM6116ACD/3 is supplied in a 24-lead dual-in-line side-brazed ceramic package (D suffix), that conforms to the requirements and dimensions specified in MIL-STD-38510 Case Outline D-3. This type is also available in a 28-contact LCC (J suffix).

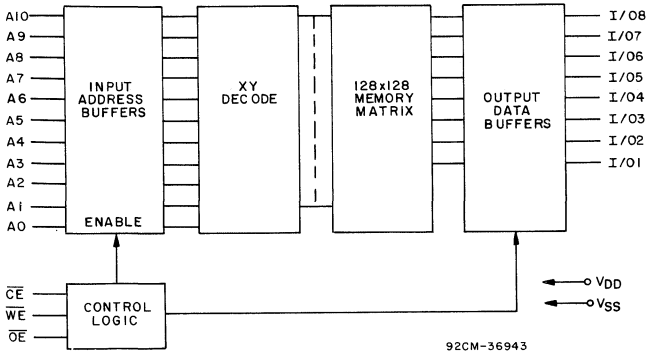


Fig. 1 - Functional block diagram.

	25/-55°C	+125°C
Access Time (max.)	150 ns	185 ns
Output Enable Time (max.)	60 ns	80 ns
Operating Temperature	-55° to +125°C	
Operating Current (max.)	45 mA	45 mA
Standby Current: TTL Level	1.7 mA	2 mA
Standby Current: CMOS Level	0.1 mA	2 mA

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0 TO A10	MODE	I/01 TO I/08	DEVICE CURRENT
H	X	X	X	NOT SELECTED	HIGH Z	STANDBY
L	L	H	STABLE	READ	DATA OUT	ACTIVE
L	H	L	STABLE	WRITE	DATA IN	ACTIVE
L	L	L	STABLE	WRITE	DATA IN	ACTIVE

L = LOW H = HIGH X = H or L

CDM6116ACD/3

MAXIMUM RATINGS, *Absolute-Maximum Ratings*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(Voltage referenced to V_{SS} terminal) ..... -0.3 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.3 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C ..... 500 mW
For T_A = +100°C to +125°C ..... Derate linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS ALL TYPES		UNITS
		MIN.	MAX.	
DC Operating Voltage Range		4.5	5.5	V
Input Voltage Range	V_{IH}	2.2	V_{DD} + 0.3	
	V_{IL}	-0.3	0.8	

STATIC ELECTRICAL CHARACTERISTICS at T_A=-55°C to +125°C, V_{DD}=5 V ± 10%, except where noted

CHARACTERISTIC		TEST CONDITIONS	LIMITS +25/-55°C Min.	LIMITS +25/-55°C Max.	LIMITS +125°C Min.	LIMITS +125°C Max.	UNITS
Standby Device Current	I_{DDS}	$\overline{CE}$ = V_{IH}, V_{IH} = 2.2 V, V_{IL} = 0.8 V	—	1.7	—	2	mA
	I_{DDS1}	$\overline{CE}$ = 5.5 V, V_{IH} = 5.5 V, V_{IL} = 0 V	—	0.1	—	2	mA
Output Voltage Low Level	V_{OL} Max.	I_{OL} = 2.1 mA	—	0.4	—	0.4	V
Output Voltage High Level	V_{OH} Min.	I_{OH} = -1 mA	2.4	—	2.4	—	V
Input Leakage Current	I_{IN} Max.	V_{DD} = 5 V, V_{IN} = 0 V to V_{DD}	—	±1	—	±2	μA
3-State Output Leakage Current	I_{OUT}	$\overline{CE}$ or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{DD}	—	±1	—	±2	μA
Operating Device Current	I_{OPER}#	V_{IN} = V_{IL}, V_{IH}, f = 1 MHz, (Where V_{IL} = 0.8 V, V_{IH} = 2.2 V)	—	45	—	45	mA

#Outputs open circuited.

SIGNAL DESCRIPTIONS

A0-A10 (Address Inputs): These inputs must be stable prior to a write operation, but may change asynchronously during read operations.
I/01-I/08: 8-bit tri-state data bus.
$\overline{CE}$ (Chip Enable): Powers down chip, disables Read and Write functions, and gates off address inputs.
$\overline{OE}$ (Output Enable): Enables tri-state outputs if $\overline{CE}$ is low and $\overline{WE}$ is high.
$\overline{WE}$ (Write Enable): Enables Write function, if $\overline{CE}$ is low. $\overline{WE}$ will dominate if both $\overline{WE}$ and $\overline{OE}$ are low (i.e., the bus will be tri-stated and a Write will occur).
V_{DD}, V_{SS}: Power supply connections.

CDM6116ACD/3

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -55°C to +125°C, V_{DD} = 5 V ± 10%, Input $t_r, t_f \leq$ 10 ns; C_L = 50 pF

CHARACTERISTIC		LIMITS				UNITS
		+25°C/-55°C		+125°C		
Read Cycle Times, See Fig. 2		**Min.†**	**Max.**	**Min.†**	**Max.**	
Read Cycle Time	t_{RC}	150	—	185	—	ns
Address Access Time	t_{AA}	—	150*	—	185*	
Chip Enable Access Time	t_{ACE}	—	150*	—	185*	
Chip Enable to Output Active	t_{CX}	15	—	15	—	
Output Enable to Output Valid	t_{OEV}	—	60*	—	80*	
Output Enable to Output Active	t_{OEX}	15	—	15	—	
Chip Disable to Output "High Z"	t_{CHZ}	—	60	—	80	
Output Disable to Output "High Z"	t_{OHZ}	—	60	—	80	
Output Hold from Address Change	t_{OH}	15	—	15	—	

†Time required by a limit device to allow for the indicated function.
*Indicates 100% testing. Other parameters do not represent 100% testing.

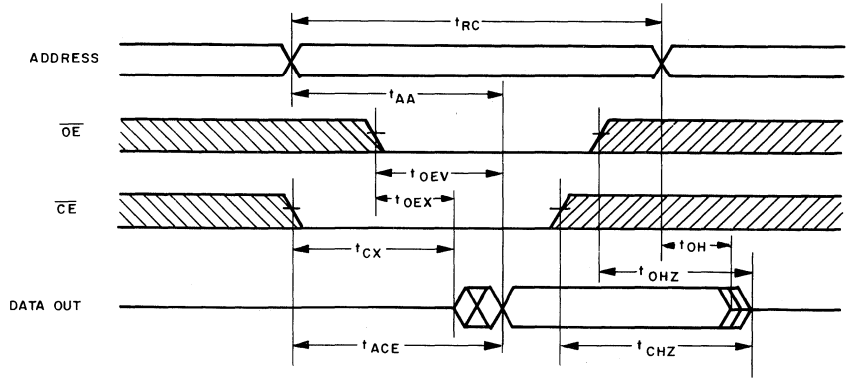


Fig. 2 - Read-cycle timing waveforms.

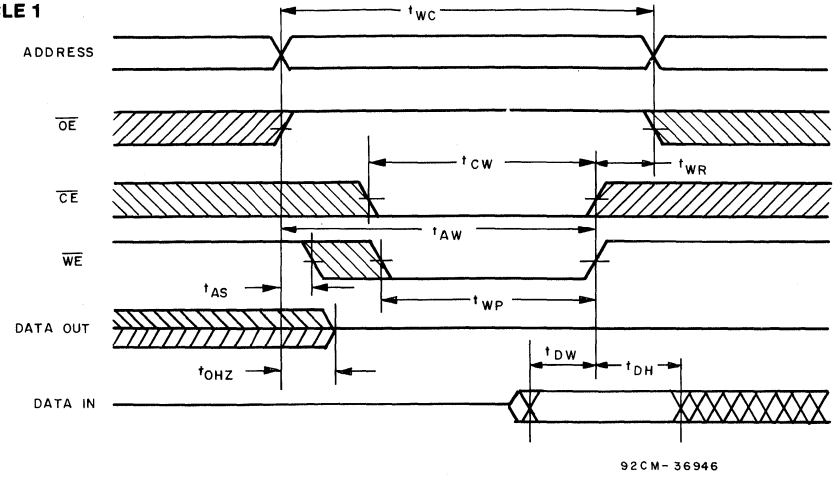
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -55°C to +125°C, V_{DD} = 5 V ± 10%, Input $t_r, t_f \leq$ 10 ns; C_L = 50 pF

CHARACTERISTIC		LIMITS				UNITS
		+25°C/-55°C		+125°C		
Write Cycle Times, See Fig. 3		**Min.†**	**Max.**	**Min.†**	**Max.**	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable to End of WRITE	t_{CW}	90*	—	120*	—	
Address Valid to End of WRITE	t_{AW}	90*	—	120*	—	
Address Setup Time	t_{AS}	0*	—	0*	—	
Write Pulse Width	t_{WP}	90*	—	120*	—	
Write Recovery Time	t_{WR}	10	—	10	—	
Output Disable to Output "High Z"	t_{OHZ}	—	60	—	80	
Write to Output "High Z"	t_{WHZ}	—	60	—	80	
Input Data Setup Time	t_{DW}	50*	—	80*	—	
Input Data Hold Time	t_{DH}	5*	—	10*	—	
Output Active from End of Write	t_{OW}	10	—	10	—	

†Time required by a limit device to allow for the indicated function.
*Indicates 100% testing. Other parameters do not represent 100% testing.

CDM6116ACD/3

WRITE CYCLE 1



WRITE CYCLE 2 - $\overline{OE}$ = LOW

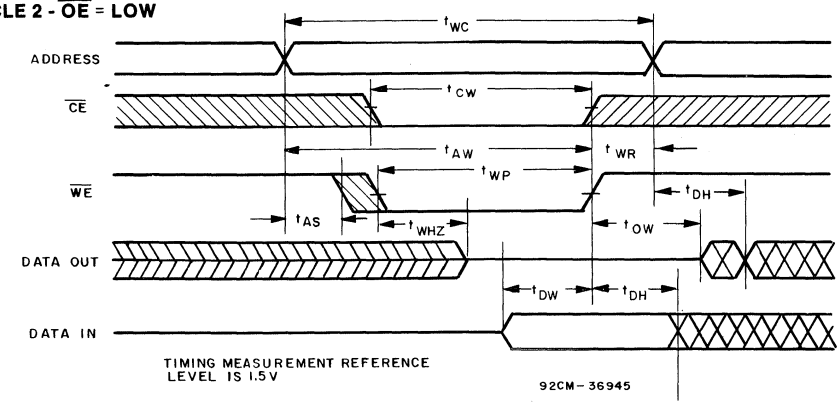


Fig. 3 - Write-cycle timing waveforms.

DATA RETENTION CHARACTERISTICS at T_A = -55° C to +125° C

CHARACTERISTIC See Fig. 4		TEST CONDITIONS	LIMITS +25° C Min.	LIMITS +25° C Max.	LIMITS +125° C Min.	LIMITS +125° C Max.	UNITS
Minimum Data Retention Voltage	V_{DR}	$\overline{CE} \geq V_{DD}$ - 0.2 V	2	—	2	—	V
Data Retention Quiescent Current	$I_{DD}DR$	V_{DD} = 3 V, $\overline{CE} \geq$ 2.8 V	—	50	—	700	μA
Chip Disable to Data Retention Time	t_{CDR}	See Fig. 4	10	—	10	—	ns
Recovery to Normal Operation Time	t_R	See Fig. 4	*t_{RC}	—	*t_{RC}	—	ns

*t_{RC} = Read Cycle Time.

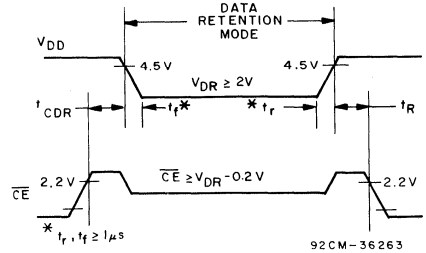


Fig. 4 - Low V_{DD} data retention timing waveforms.

Advance Information/
Preliminary Data

CDM6264CD/3

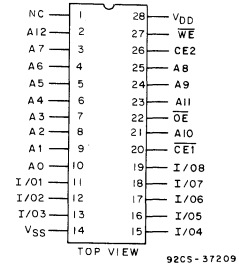
High-Reliability CMOS 8192-Word By 8-Bit LSI Static RAM

Features:
- *Fully static operation*
- *Single power supply: 4.5 V to 5.5 V*
- *All inputs and outputs directly TTL compatible*
- *3-state outputs*
- *Industry-standard 28-pin configuration*
- *Input address buffers gated off with chip disable*
- *Fast access time: t_{AA}=200 ns at +125° C*
- *Low operating power: I_{OPER2}=40 mA maximum*
- *Data retention voltage: 2 V min. 0° to +125° C*
- *Operating-temperature range (max. rating): −55° C to +125° C*

The RCA-CDM6264CD/3 is a high-reliability 8192-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This device has common data input and data output and utilizes a single power supply of 4.5 V to 5.5 V.

Either chip enable ($\overline{CE1}$ or CE2), when not valid, will gate off the address and output buffers and power down the chip to minimum standby power with inputs toggling. The output enable ($\overline{OE}$) controls the output buffers to eliminate bus contention.

The CDM6264CD/3 is supplied in 28-lead hermetic, dual-in-line side-brazed ceramic package (D suffix) that conforms to the requirements and dimensions specified in MIL-38510 Case Outline D-3. This type will also be available in a LCC package (J suffix).



TERMINAL ASSIGNMENT

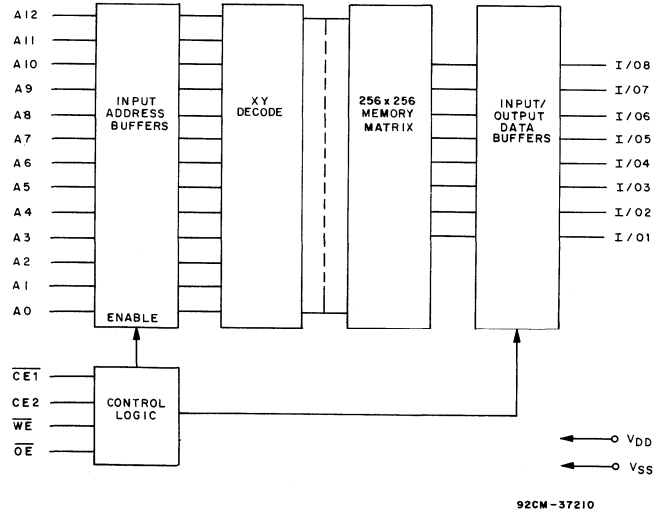


Fig. 1 - Functional block diagram.

CDM6264CD/3

TRUTH TABLE

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	A0 to A12	MODE	DATA I/O	DEVICE CURRENT
H	X	X	X	X	NOT SELECTED	HIGH Z	STANDBY
X	L	X	X	X	NOT SELECTED	HIGH Z	STANDBY
L	H	L	H	STABLE	READ	DATA OUT	ACTIVE
L	H	X	L	STABLE	WRITE	DATA IN	ACTIVE
L	H	H	H	STABLE	OUTPUT DISABLE	HIGH Z	ACTIVE

L = Low H = High X = H or L

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(Voltage reference to V_{SS} terminal) ..... -0.3 to +7 V
INPUT VOLTAGE RANGE, ALL INPUT ..... -0.3 to +7 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55° to 100°C (PACKAGE TYPE D) ..... 500 mW
For T_A = 100° to 125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55 to +125°C
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS		UNITS
		ALL TYPES		
		MIN.	MAX.	
DC Operating Voltage Range		4.5	5.5	V
Input Voltage Range	V_{IH}	2.2	V_{DD} + 0.3	
	V_{IL}	-0.3	0.8	
Input Signal Rise or Fall Time Δ	t_r, t_f	—	5	μs

Δ Input signal rise and fall times with a duration greater than the maximum value can cause loss of stored data in the selected mode.

CDM6264CD/3

STATIC ELECTRICAL CHARACTERISTICS at T_A = -55 to +125° C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS	LIMITS				UNITS
			+25/-55° C		+125° C		
			MIN.	MAX.	MIN.	MAX.	
Standby Device Current	I_{DDS}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}	—	3	—	4	mA
	I_{DDS1}	$\overline{CE1}$ = CE2 ≥ V_{DD} -0.2 V or CE2 ≤ 0.2 V	—	100	—	2	mA
Output Voltage Low Level	V_{OL} Max.	I_{OL} = 2.1 mA	—	0.4	—	0.4	V
Output Voltage High Level	V_{OH} Min.	I_{OH} = -1 mA	2.4	—	2.4	—	V
Input Leakage Current	I_{IN} Max.	V_{IN} = 0 V to V_{DD}	—	±2	—	±2	μA
3-State Output Leakage	I_{OUT}	$V_{I/O}$ = 0 V to V_{DD}	—	±2	—	±2	
Operating Device Current	I_{OPER1} #	V_{IN} = V_{IL}, V_{IH} t_{cyc} = 1 μs	—	15	—	15	mA
	I_{OPER2} #	V_{IN} = 0.2 V, V_{DD} -0.2 V t_{cyc} = 1 μs	—	10	—	10	
Input Capacitance	C_{IN}	V_{IN} = 0 V, f = 1 MHZ, T_A = 25° C	—	6	—	6	pF
Output Capacitance	C_{IO}	$V_{I/O}$ = 0 V, f = 1 MHz, T_A = 25° C	—	8	—	8	

Output open circuited.

SIGNAL DESCRIPTIONS

A0-A10 (Address Inputs):

These inputs must be stable prior to a write operation, but may change asynchronously during read functions.

I/01-I/08:

8-bit tristate data bus.

$\overline{CE1}$, CE2 (Chip Enable):

Either chip enable, when not true, powers down the chip, disables Read and Write functions, and gates off address and output buffers.

$\overline{OE}$ (Output Enable):

Enables tristate outputs if $\overline{CE1}$ and CE2 are valid and $\overline{WE}$ is high.

$\overline{WE}$ (Write Enable):

Enables Write function, if $\overline{CE1}$ and CE2 are valid. $\overline{WE}$ will dominate if both $\overline{WE}$ and $\overline{OE}$ are low (i.e., the bus will be tristated and a Write will occur).

V_{DD}, V_{SS}:

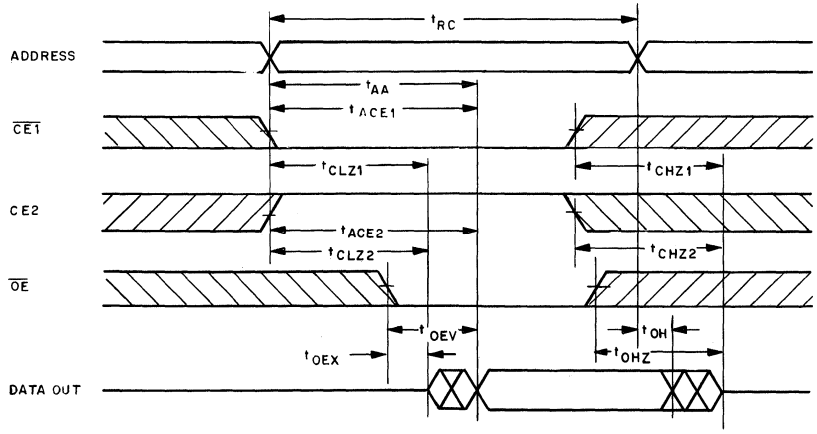
Power supply connections.

CDM6264CD/3

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -55 to +125° C, V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns

CHARACTERISTIC		LIMITS				UNITS
		+25/-55° C		+125° C		
Read Cycle Times, See Fig. 2		**MIN.**	**MAX.**	**MIN.**	**MAX.**	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	
Chip Enable Access Time	t_{ACE1}, t_{ACE2}	—	150	—	200	
Chip Enable to Output Active	t_{CLZ1}, t_{CLZ2} *	10	—	10	—	
Output Enable to Output Valid	t_{OEV}	—	70	—	70	
Output Enable to Output Active	t_{OEX} *	5	—	5	—	
Chip Disable to Output "High"	t_{CHZ1}, t_{CHZ2} *	0	70	0	70	
Output Disable to Output "High" Z	t_{OHZ} *	0	60	0	60	
Output Hold from Address Change	t_{OH} *	30	—	30	—	

* Indicates 100% testing.



WE IS HIGH DURING READ CYCLE. TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V. 92CM-37205

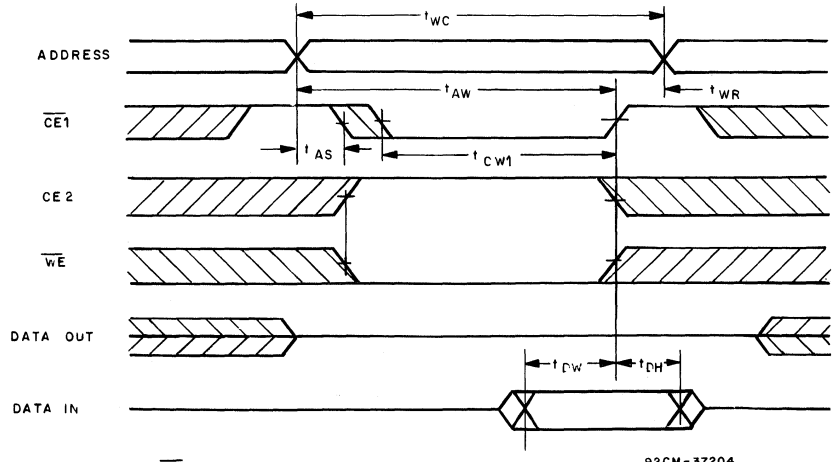
Fig. 2 - Read-cycle timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -55 to +125° C, V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns

CHARACTERISTIC		LIMITS				UNITS
		+25/-55° C		+125° C		
Write Cycle Times, See Fig. 3		**MIN.**	**MAX.**	**MIN.**	**MAX.**	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable to End of WRITE	t_{CW1}, t_{CW2}	120	—	170	—	
Address Valid to End of WRITE	t_{AW}	120	—	170	—	
Address Setup Time	t_{AS}	0	—	0	—	
Write Enable Width	t_{WW}	100	—	120	—	
Write Recovery Time	t_{WR}	0	—	0	—	
Write to Output "High Z"	t_{WHZ} *	—	70	—	70	
Input Data Setup Time	t_{DW}	60	—	80	—	
Input Data Hold Time	t_{DH}	0	—	0	—	
Output Active from End of Write	t_{OW} *	10	—	10	—	

* Indicates 100% testing.

WRITE CYCLE 1 ($\overline{CE1}$ CONTROL)

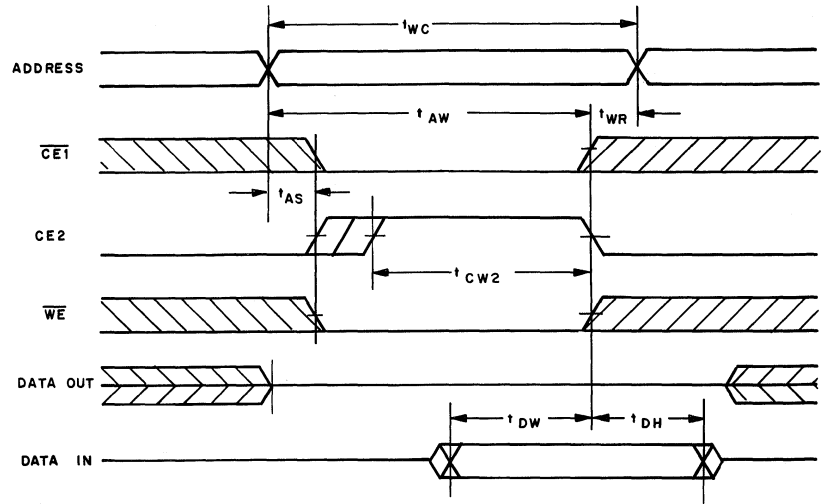


IN A $\overline{CE1}$ OR CE2 CONTROLLED WRITE CYCLE, THE OUTPUT BUFFERS REMAIN IN A HIGH IMPEDANCE STATE, WHETHER $\overline{OE}$ IS HIGH OR LOW. TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

Fig. 3 - Write-cycle timing waveforms.

CDM6264CD/3

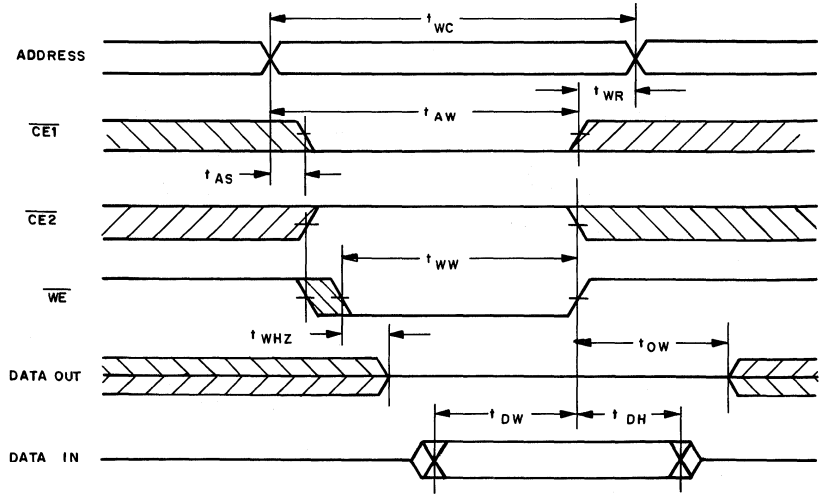
WRITE CYCLE 2 (CE2 CONTROL)



IN A $\overline{CE1}$ OR CE2 CONTROLLED WRITE CYCLE, THE OUTPUT BUFFERS REMAIN IN A HIGH IMPEDANCE STATE, WHETHER $\overline{OE}$ IS HIGH OR LOW.
TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

92CM-37206

WRITE CYCLE 3 ($\overline{WE}$ CONTROL)



IF $\overline{OE}$ IS HIGH DURING A $\overline{WE}$ CONTROLLED WRITE CYCLE,
THE OUTPUT BUFFERS REMAIN IN A HIGH IMPEDANCE STATE IN THIS PERIOD.
TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

92CS-37207

Fig. 3 - Write-cycle timing waveforms (cont'd).

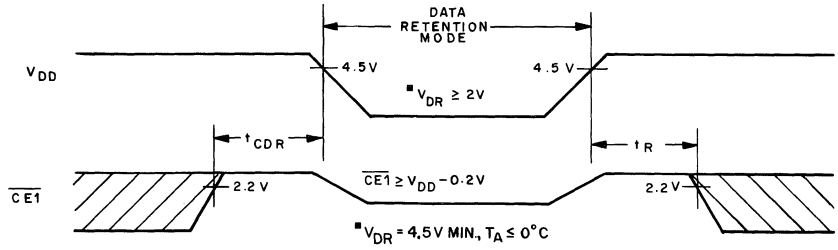
DATA RETENTION CHARACTERISTICS at T_A = -55° C to +125° C; See Fig. 4

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			ALL TYPES		
			MIN.	MAX.	
Minimum Data Retention Voltage	V_{DR} ■	$\overline{CE1} \geq V_{DD}$ -0.2 V or CE2 ≤ 0.2 V	2	—	V
Data Retention Quiescent Current	$I_{DD}DR$	V_{DD} = 3 V, $\overline{CE1}$, CE2 ≥ V_{DD} -0.2 V or CE2 ≤ 0.2 V	—	600	μA
Chip Disable to Data Retention Time	t_{CDR}	See Fig. 4	0	—	ns
Recovery to Normal Operation Time	t_R	See Fig. 4	*t_{RC}	—	

■ Power down time = 500 ms

*t_{RC} = Read Cycle Time.

DATA RETENTION WAVEFORM 1 ($\overline{CE1}$ CONTROL)



DATA RETENTION WAVEFORM 2 (CE2 CONTROL)

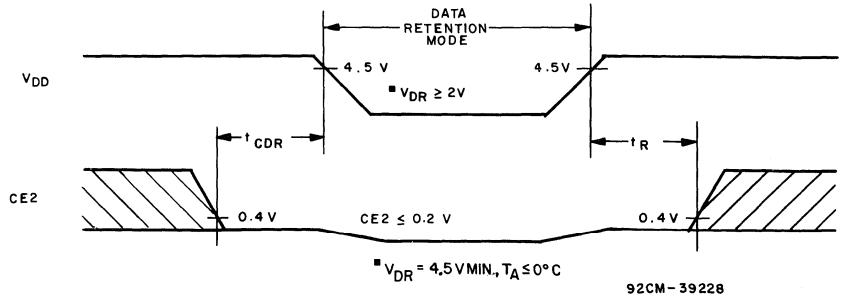
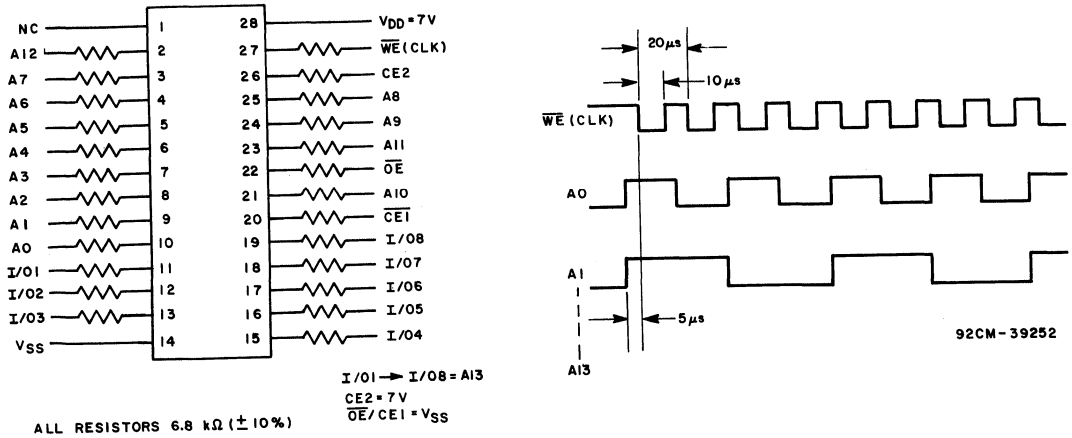


Fig. 4 - Low V_{DD} data-retention timing waveforms.

CDM6264CD/3



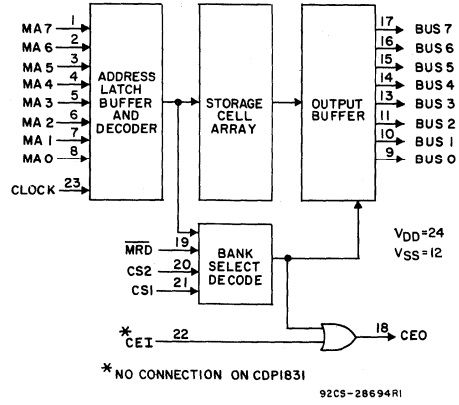
TYPE NO.	V_{DD}	TEMP.	TIME
CDM6264CD/3	7 V ± 0.5 V	+125° C	160 Hrs, Min.

Fig. 5 - Dynamic burn-in circuit.

512-Word x 8-Bit Static Read-Only Memory

Features:

- *User mask-option programs ROM's location in memory field*
- *Mask programmable*
- *On-chip latch for higher-order memory address*
- *CEO signal indicates status of chip (selected or not)*
- *Can minimize or eliminate memory decoding logic*
- *2 chip selects*
- *3-state outputs*
- *Single power supply*
- *Industry standard 24-pin packages*
- *Directly compatible with CDP1802*



Functional diagram.

ELECTRICAL CHARACTERISTICS

5-Volt data apply to both the CDP1831 and CDP1831C.
10-Volt data apply to the CDP1831 only.

Characteristic	Test Conditions			Limits at Indicated Temperatures (°C)				Units
				CDP1831 CDP1831C				
	V_{IN} (V)	V_O (V)	V_{DD} (V)	+25 -55		+125		
				Min.	Max.	Min.	Max.	
Static								
Quiescent Device Current, I_L	0, 5	—	5	—	500	—	1000	μA
	0, 10	—	10	—	500	—	1000	
Output Low Drive (Sink) Current I_{OL}	0, 5	0.4	5	0.8	—	0.48	—	mA
	0, 10	0.5	10	1.8	—	1.08	—	
Output High Drive (Source) Current, I_{OH}	0, 5	4.6	5	-0.8	—	-0.48	—	
	0, 10	9.5	10	-1.8	—	-1.08	—	
Input Leakage Current, I_{IN}	0,5	—	5	—	±1	—	±5	μA
	0, 10	—	10	—	±1	—	±5	
3-State Output Leakage Current I_{OUT}	0, 5	0, 5	5	—	±5	—	±15	
	0, 10	0, 10	10	—	±5	—	±15	

CDP1832/3, CDP1832C/3

High-Reliability CMOS 512-Word x 8-Bit Static Read-Only Memory

Features:
- *Compatible with CDP1800 and CD4000-series devices*
- *Functional replacement for industry type 2704 512 x 8 EPROM*
- *Three-state outputs*

The RCA-CDP1832/3 and CDP1832C/3 types are high-reliability 4096-bit mask-programmable CMOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems.

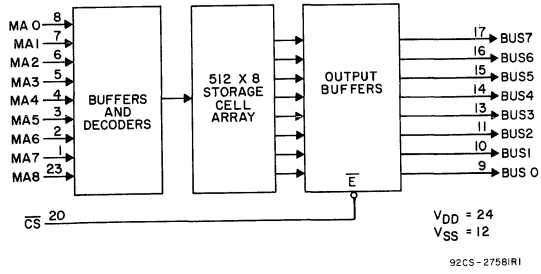
The CDP1832/3 ROMs are completely static; no clocks are required.

A Chip-Select input ($\overline{CS}$) is provided for memory expansion. Outputs are enabled when $\overline{CS}$=0.

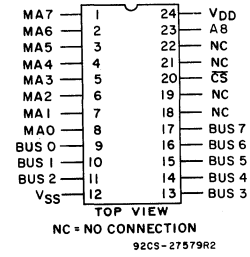
The CDP1832/3 is a pin-for-pin compatible replacement for the industry type 2704 EPROM.

The CDP1832C/3 is functionally identical to the CDP1832/3. The CDP1832/3 has an operating voltage range of 4 to 10.5 volts, and the CDP1832C/3 has a operating voltage range of 4 to 6.5 volts.

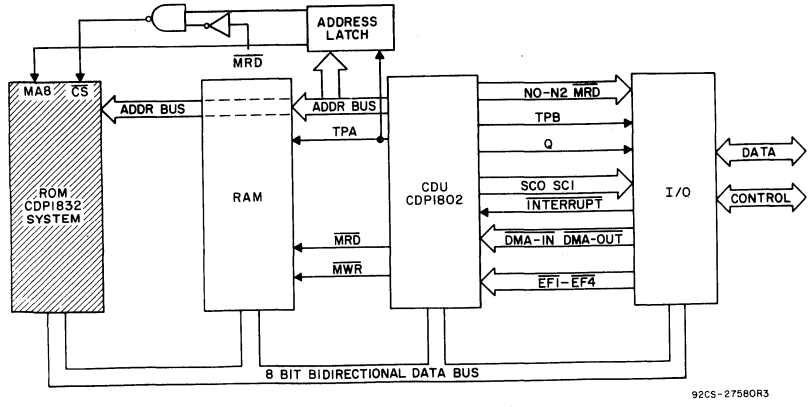
The CDP1832/3 and the CDP1832C/3 are supplied in 24-lead, hermetic, dual-in-line, side-brazed ceramic packages (D suffix). Other package styles may be available on a special order basis.



Functional diagram.



TERMINAL ASSIGNMENT



Typical CDP1802 microprocessor system.

CDP1832/3, CDP1832C/3

STATIC ELECTRICAL CHARACTERISTICS

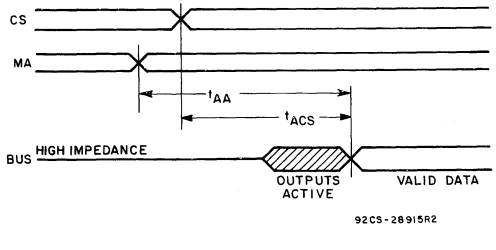
CHARACTERISTIC		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS -55°C, +25°C Min.	LIMITS -55°C, +25°C Max.	LIMITS +125°C Min.	LIMITS +125°C Max.	UNITS
Quiescent Device Current,	I_{DD}†	—	5	5	—	100	—	500	μA
		—	10	10	—	500	—	1000	
Output Low Drive (Sink) Current,	I_{OL}	0.4	0, 5	5	0.6	—	0.35	—	mA
		0.5	0, 10	10	1.5	—	0.9	—	
Output High Drive (Source) Current,	I_{OH}	4.6	0, 5	5	—	-0.5	—	-0.3	
		9.5	0, 10	10	—	-1	—	-0.65	
Output Voltage Low-Level,	V_{OL}*	—	0, 5	5	—	0.1	—	0.2	V
		—	0, 10	10	—	0.1	—	0.2	
Output Voltage High Level,	V_{OH}*	—	0, 5	5	4.9	—	4.8	—	
		—	0, 10	10	9.9	—	9.8	—	
Input Low Voltage,	V_{IL}	0.5,4.5	—	5	—	1.5	—	1.5	
		1, 9	—	10	—	3	—	3	
Input High Voltage,	V_{IH}	0.5,4.5	—	5	3.5	—	3.5	—	
		1, 9	—	10	7	—	7	—	
Input Leakage Current,	I_{IN}	Any	0, 5	5	—	±1	—	±5	μA
		Input	0, 10	10	—	±2	—	±5	
3-State Output Leakage Current,	I_{OUT}	0, 5	0, 5	5	—	±1	—	±5	
		0, 10	0, 10	10	—	±2	—	±5	
Input Capacitance,	C_{IN}*	—	—	—	—	10	—	10	pF
Output Capacitance,	C_{OUT}*	—	—	—	—	15	—	15	

*Guaranteed but not tested.

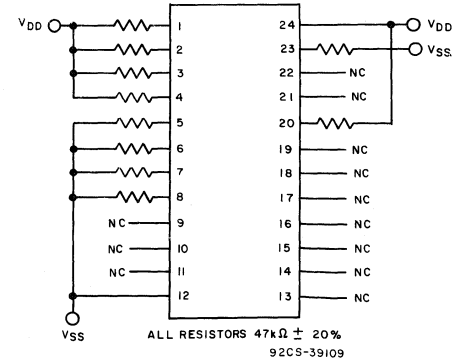
†CDP1832C/3 meets all 5-volt static electrical characteristics of the CDP1832/3 except for quiescent device current for which the limit is I_{DD}=500 μA @ -55°C/+25°C and I_{DD}=1000 μA @ +125°C.

DYNAMIC ELECTRICAL CHARACTERISTICS, Input t_r,t_f = 15 ns, C_L = 50 pF

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS -55°C, +25°C Min.	LIMITS -55°C, +25°C Max.	LIMITS +125°C Min.	LIMITS +125°C Max.	UNITS
Access Time From Address Change,	t_{AA}	5	—	840	—	1160	ns
		10	—	435	—	600	
Access Time From Chip Select,	t_{ACS}	5	—	455	—	635	
		10	—	210	—	290	



Timing waveforms.



Type No.	V_{DD}	Temp.	Time
CDP1832/3	11 ±0.5 V	125°C	160 hrs. min.
CDP1832C/3	7 ±0.5 V	125°C	160 hrs. min.

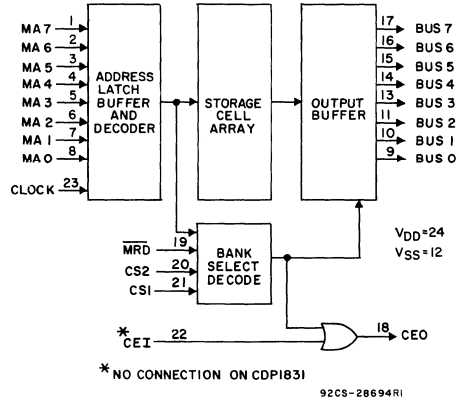
Static burn-in circuit.

CDP1833/3, CDP1833C/3

CMOS 1024-Word x 8-Bit Static Read-Only Memory

Features:

- *User mask-option programs ROM's location in memory field*
- *Mask programmable*
- *On-chip latch for higher-order memory address*
- *CEO signal indicates status of chip (selected or not)*
- *Can minimize or eliminate memory decoding logic*
- *2 chip selects*
- *3-state outputs*
- *Single power supply*
- *Industry standard 24-pin packages*
- *Directly compatible with CDP1802*



Functional diagram.

ELECTRICAL CHARACTERISTICS

5-Volt data apply to both the CDP1833 and CDP1833C.
10-Volt data apply to the CDP1833 only.

Characteristic	Test Conditions			Limits at Indicated Temperatures (°C)				Units
				CDP1833 CDP1833C				
	V_{IN} (V)	V_O (V)	V_{DD} (V)	+25 -55		+125		
				Min.	Max.	Min.	Max.	
Static								
Quiescent Device Current, I_L	0, 5	—	5	—	500	—	1000	μA
	0, 10	—	10	—	500	—	1000	
Output Low Drive (Sink) Current I_{OL}	0, 5	0.4	5	0.8	—	0.48	—	mA
	0, 10	0.5	10	1.8	—	1.08	—	
Output High Drive (Source) Current, I_{OH}	0, 5	4.6	5	-0.8	—	-0.48	—	
	0, 10	9.5	10	-1.8	—	-1.08	—	
Input Leakage Current, I_{IN}	0,5	—	5	—	±1	—	±5	μA
	0, 10	—	10	—	±1	—	±5	
3-State Output Leakage Current I_{OUT}	0, 5	0, 5	5	—	±5	—	±15	
	0, 10	0, 10	10	—	±5	—	±15	

CDP1834/3, CDP1834C/3

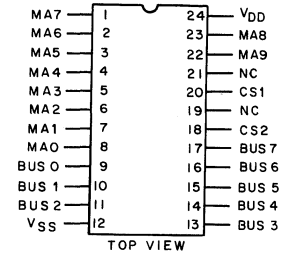
High-Reliability CMOS 1028-Word x 8-Bit Static Read-Only Memory

Features:

- *Three-state output*
- *Mask programmable chip select*
- *Completely static, no clocks required*
- *Pin-compatible with industry type 2708*

The RCA-CDP1834/3 and CDP1834C/3 are High-reliability 8192-bit mask-programmable CMOS read-only memories organized as 1024-words x 8 bits and designed for use in CDP1800-series microprocessor systems. The CDP1834-series ROM's are completely static; no clocks are required.

Two Chip-Select inputs (CS1, CS2) are provided for memory expansion. The polarity of each Chip-Select is user mask-programmable. The CDP1834-series is pin-compatible with industry type 2708 EPROM. The CDP1834C/3 is functionally identical to the CDP1834/3. The CDP1834/3 has a recommended operating voltage range of 4 to 10.5 volts and the CDP1834C/3 has a recommended operating voltage range of 4 to 6.5 volts. The CDP1834/3 and the CDP1834C/3 are supplied in 24-lead dual-in-line ceramic packages (D suffix). Other package styles may be available on a special order basis.



TERMINAL ASSIGNMENT

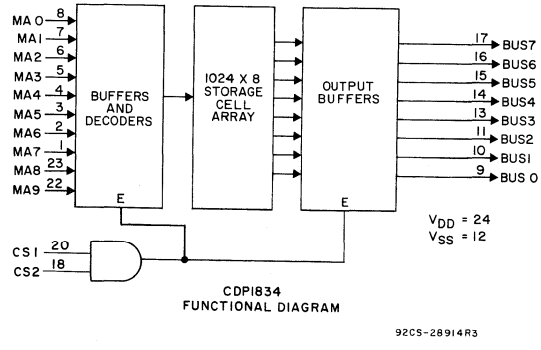


Fig. 1 — Functional diagram.

CDP1834/3, CDP1834C/3

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CONDITIONS			LIMITS				UNITS
		VO (V)	VIN (V)	VDD (V)	-55°C, +25°C		+125°C		
					Min.	Max.	Min.	Max.	
Quiescent Device Current†	IDD	— —	5 10	5 10	— —	100 500	— —	500 1000	μA
Output Low Drive (Sink) Current	IOL	0.4 0.5	0, 5 0, 10	5 10	0.8 1.8	— —	0.48 1.0	— —	mA
Output High Drive (Source) Current	IOH	4.6 9.5	0, 5 0, 10	5 10	— —	-0.8 -1.8	— —	-0.48 -1.0	mA
Output Voltage Low-Level*	VOL	— —	0,5 0, 10	5 10	— —	0.1 0.1	— —	0.2 0.2	V
Output Voltage High Level*	VOH	— —	0,5 0, 10	5 10	4.9 9.9	— —	4.8 9.8	— —	V
Input Low Voltage	VIL	0.5, 4.5 1, 9	— —	5 10	— —	1.5 3	— —	1.5 3	V
Input High Voltage	VIH	0.5, 4.5 1, 9	— —	5 10	3.5 7	— —	3.5 7	— —	V
Input Leakage Current	IIN	Any Input Any Input	0, 5 0, 10	5 10	— —	±1 ±2	— —	±5 ±5	μA
3-State Output Leakage Current	IOUT	0, 5 0, 10	5 10	5 10	— —	±1 ±2	— —	±5 ±5	μA
Input Capacitance*	CIN	—	—	—	—	10	—	10	pF
Output Capacitance*	COUT	—	—	—	—	15	—	15	pF

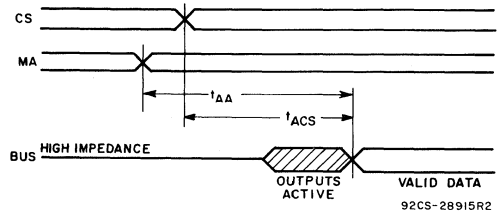
*Guaranteed but not tested

†CDP1834C/3 meets all 5 volt static electrical characteristics of the CDP1834/3 except for quiescent device current for which the limit is I_{DD} = 500 μA @ -55°C/+25°C and I_{DD} = 1000 μA @ +125°C.

DYNAMIC ELECTRICAL CHARACTERISTICS Input t_r, t_f = 15 ns, C_L = 50 pF

CHARACTERISTIC	TEST CONDITIONS VDD (V)	LIMITS				UNITS
		-55°C, +25°C		+125°C		
		Min.	Max.	Min.	Max.	
Access Time for Address Change, t_{AA}	5 10	— —	655 275	— —	855 475	ns
Access Time from Chip Select, t_{ACS}	5 10	— —	610 260	— —	795 435	ns

*Typical values are for T_A = 25°C and nominal VDD



Note: The CDP1834/3 and CDP1834C/3 must be deselected before an address change or remain selected after an address change.

Fig. 2 — Timing waveforms.

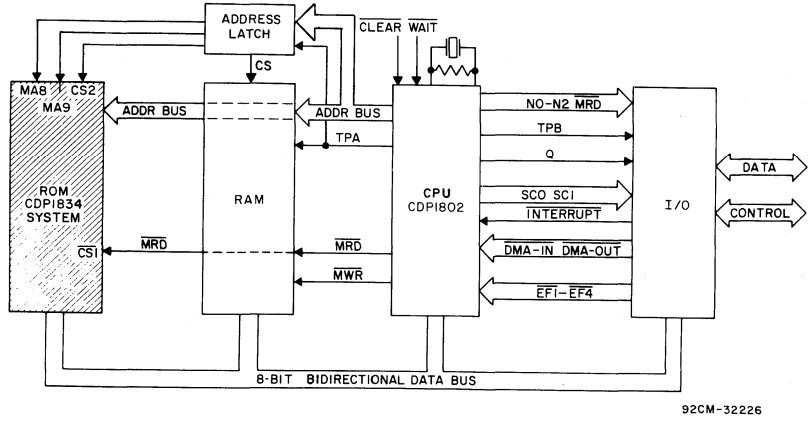
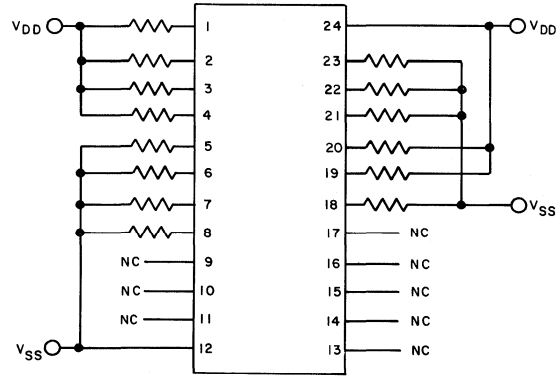


Fig. 3 — Typical CDP1802 microprocessor system.



All resistors 47KΩ ± 20%

92CS-39111

TYPE NO.	VDD	TEMP.	TIME
CDP1834/3	11 ± 0.5V	125°C	160 hrs. min.
CDP1834C/3	7 ± 0.5V	125°C	160 hrs. min.

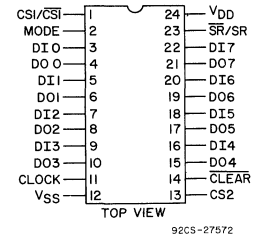
Static burn-in circuit.

CDP1852/3, CDP1852C/3

High-Reliability Byte-Wide Input/Output Port

Features:

- *Static silicon-gate CMOS circuitry*
- *Parallel 8-bit data register and buffer*
- *Handshaking via service request flip-flop*
- *Low quiescent and operating power*
- *Interfaces directly with CDP1800-series microprocessors*
- *Single voltage supply*
- *Full military temperature range (-55° C to +125° C)*



CDP1852, CDP1852C TERMINAL ASSIGNMENT

The RCA-CDP1852/3 and CDP1852C/3 are parallel, 8-bit, mode-programmable input/output ports. They are compatible and will interface directly with CDP1800 series microprocessors. They are also useful as 8-bit address latches when used with the CDP1800 multiplexed address bus and as I/O ports in general-purpose applications.

The mode control is used to program the device as an input port (mode = 0) or as an output port (mode = 1). The $\overline{SR}$/SR output can be used as a signal to indicate when data is ready to be transferred. In the input mode, a peripheral device can strobe data into the CDP1852/3, and a microprocessor can read that data by device selection. In the output mode, a microprocessor strobes data into the CDP1852/3, and hand-shaking is established with a peripheral device when the CDP1852/3 is deselected.

In the input mode, data at the data-in terminals (DI0-DI7) is strobed into the port's 8-bit register by a high (1) level on the clock line. The negative high-to-low transition of the clock latches the data in the register and sets the service request output low ($\overline{SR}$/SR = 0). When CS1/$\overline{CS1}$ and CS2 are high (CS1/$\overline{CS1}$ and CS2 = 1), the 3-state output drivers are enabled and data in the 8-bit register appear at the data-out terminals (DO0-DO7). When either CS1/$\overline{CS1}$ or CS2 goes low (CS1/$\overline{CS1}$ or CS2 =0), the data-out terminals are tristated and the service request output returns high ($\overline{SR}$/SR = 1).

In the output mode, the output drivers are enabled at all times. Data at the data-in terminals (DI0-DI7) is strobed into the 8-bit register when CS1/$\overline{CS1}$ is low (CS1/$\overline{CS1}$ = 0) and CS2 and the clock are high (1), and are present at the data-out terminals (DO0-DO7). The negative high-to-low transition of the clock latches the data in the register. The $\overline{SR}$/SR output goes high ($\overline{SR}$/SR = 1) when the device is deselected (CS1/$\overline{CS1}$ = 1 or CS2 = 0) and returns low ($\overline{SR}$/SR = 0) on the following trailing edge of the clock.

A $\overline{CLEAR}$ control is provided for resetting the port's register (DO0-DO7 = 0) and service request flip-flop (input mode: $\overline{SR}$/SR = 1 and output mode: $\overline{SR}$/SR = 0).

The CDP1852/3 is functionally identical to the CDP1852C/3. The CDP1852/3 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1852C/3 has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1852/3 and CDP1852C/3 are supplied in 24-lead, dual-in-line side-brazed ceramic packages (D suffix) that conforms to the requirements and dimensions specified in MIL-38510 Case Outline D-3. Other package styles may be available on a special order basis.

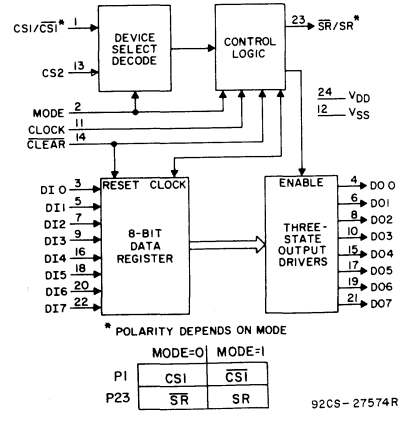


Fig. 1 - Block diagram of CDP1852/3.

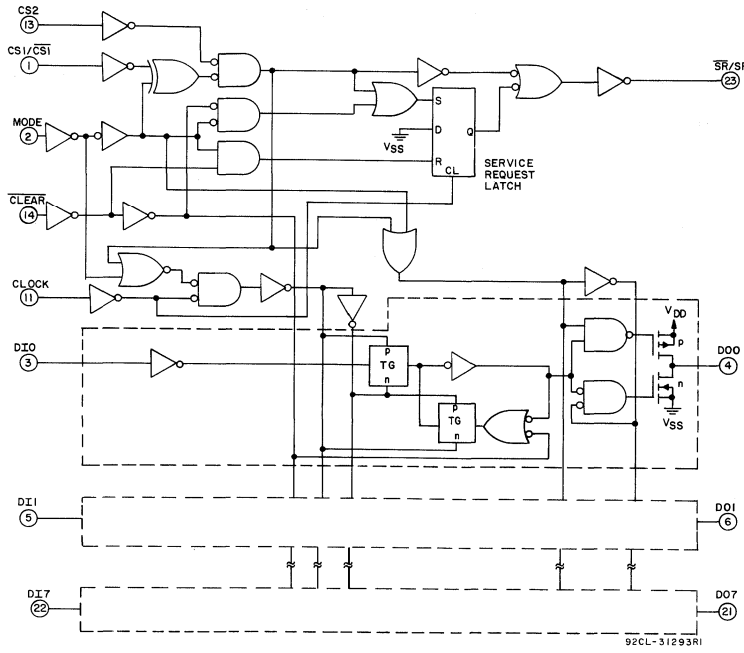
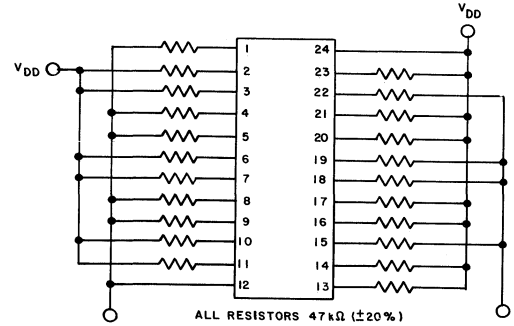


Fig. 2 - CDP1852/3 logic diagram.



TYPE No.	V_{DD}	TEMP.	TIME
CDP1852/3	11V±0.5V	+125°C	160 Hrs, MIN.
CDP1852C/3	7V±0.5V	+125°C	160 Hrs, MIN.

92CS-39014

Static burn-in circuit.

CDP1852/3, CDP1852C/3

STATIC ELECTRICAL CHARACTERISTICS, V_{IN} = 0 or V_{DD}, except as noted:

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25/-55°C		+125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current (Note 1)	I_{DD}	V_{DD} = 5 V	—	10	—	100	μA
		V_{DD} = 10 V	—	20	—	300	
Output Low Drive (Sink) Current	I_{OL}	V_{DD} = 5 V, V_O = 0.4 V	2.6	—	1.9	—	mA
		V_{DD} = 10 V, V_O = 0.5 V	6.1	—	4.1	—	
Output High Drive (Source) Current	I_{OH}	V_{DD} = 5 V, V_O = 4.6 V	-1.8	—	-1.3	—	
		V_{DD} = 10 V, V_O = 9.5 V	-4.4	—	-2.9	—	
Output Voltage Low Level	V_{OL}	V_{DD} = 5 V, I_{OL} = 0 μA	—	0.1	—	0.2	V
		V_{DD} = 10 V, I_{OL} = 0 μA	—	0.1	—	0.2	
Output Voltage High Level	V_{OH}	V_{DD} = 5 V, I_{OL} = 0 μA	4.9	—	4.8	—	
		V_{DD} = 10 V, I_{OL} = 0 μA	9.9	—	9.8	—	
Input Low Voltage	V_{IL}	V_{DD} = 5 V, V_O = 0.2, 4.8 V	—	1.5	—	1.5	
		V_{DD} = 10 V, V_O = 0.2, 9.8 V	—	3	—	3	
Input High Voltage	V_{IH}	V_{DD} = 5 V, V_O = 0.2, 4.8 V	3.5	—	3.5	—	
		V_{DD} = 10 V, V_O = 0.2, 9.8 V	7	—	7	—	
Input Leakage Low	I_{IL}	V_{DD} = 5 V, V_{IN} = 0 V	—	-1	—	-5	μA
		V_{DD} = 10 V, V_{IN} = 0 V	—	-1	—	-5	
Input Leakage High	I_{IH}	V_{DD} = 5 V, V_{IN} = 5 V	—	1	—	5	
		V_{DD} = 10 V, V_{IN} = 10 V	—	1	—	5	
3-State Output Leakage Low	I_{OZL}	V_{DD} = 5 V, V_O = 0 V	—	-1	—	-5	
		V_{DD} = 10 V, V_O = 0 V	—	-1	—	-5	
3-State Output Leakage High	I_{OZH}	V_{DD} = 5 V, V_O = 5 V	—	1	—	5	
		V_{DD} = 10 V, V_O = 10 V	—	1	—	5	
Input Capacitance	C_{IN}	Note 2	—	10	—	10	pF
Output Capacitance	C_{OUT}	Note 2	—	15	—	15	

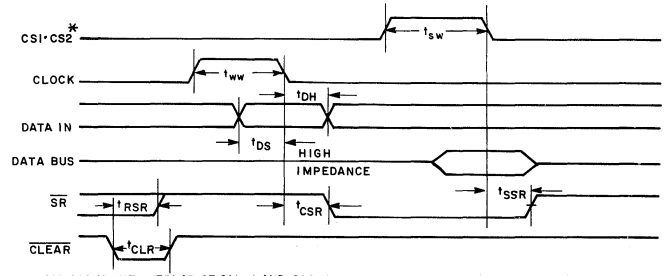
Note 1: The CDP1852C/3 meets all 5 volt Static Electrical Characteristics of the CDP1852/3 except +125° C Quiescent Device Current for which the limit is I_{DD} = 300 μA.

Note 2: Input and Output Capacitance are guarenteed but not tested.

DYNAMIC ELECTRICAL CHARACTERISTICS - MODE = 0 INPUT PORT, See Fig. 3
Input t_r, $t_f \leq 15$ ns; $C_L = 50$ pF

CHARACTERISTIC	V_{DD} V	LIMITS +25°C/-55°C Min.†	LIMITS +25°C/-55°C Max.	LIMITS +125°C Min.†	LIMITS +125°C Max.	UNITS
Select Duration t_{SW}	5	250	—	360	—	ns
	10	150	—	180	—	
Clock Pulse Width t_{WW}	5	150	—	200	—	
	10	90	—	110	—	
Clear Pulse Width t_{CLR}	5	110	—	160	—	
	10	50	—	80	—	
Data-In to Clock Fall Setup Time t_{DS}	5	-10	—	-10	—	
	10	-5	—	-5	—	
Data-In After Clock Fall Hold Time t_{DH}	5	150	—	170	—	
	10	70	—	100	—	
Propagation Delay Times:						
Clear to $\overline{SR}$ t_{RSR}	5	—	200	—	340	
	10	—	110	—	170	
Clock to $\overline{SR}$ t_{CSR}	5	—	175	—	220	
	10	—	110	—	130	
Deselect to $\overline{SR}$ t_{SSR}	5	—	175	—	240	
	10	—	110	—	120	

†Time required by a device to allow for the indicated function.



* CS1·CS2 IS THE OVERLAP OF CS1 = 1 AND CS2 = 1

MODE=0 TRUTH TABLE

CLOCK	†CS1-CS2	CLEAR	Data Out Equals
X	0	X	High Impedance
0	1	0	0
0	1	1	Data Latch
1	1	X	Data In

†CS1 · CS2 = CS1 = 1, CS2 = 1

SERVICE REQUEST TRUTH TABLE

CLOCK	CS1 or CS2 or CLEAR
SR/SR : 0	SR/SR = 1

92CM-38013

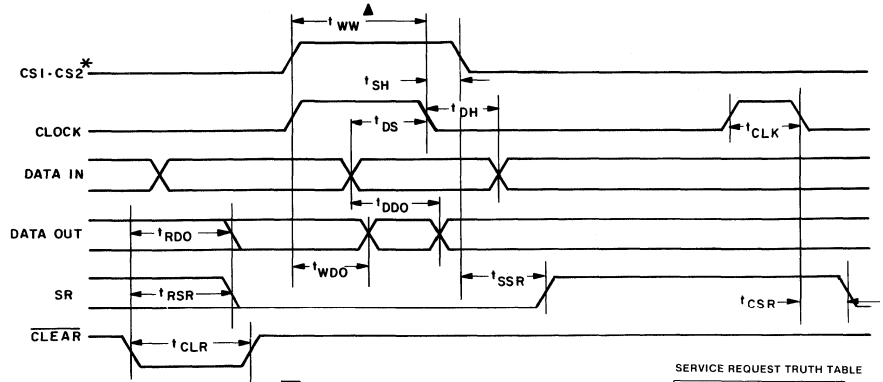
Fig. 3 - Mode = 0 input port timing waveforms and truth tables.

CDP1852/3, CDP1852C/3

DYNAMIC ELECTRICAL CHARACTERISTICS - MODE = 1 INPUT PORT, See Fig. 4
Input t_r, $t_f \leq 15$ ns; $C_L = 50$ pF

CHARACTERISTIC		V_{DD} V	LIMITS +25°C/-55°C Min.†	+25°C/-55°C Max.	+125°C Min.†	+125°C Max.	UNITS
Clock Pulse Width	t_{CLK}	5	170	—	260	—	ns
		10	90	—	130	—	
Write Width Duration	t_{WW}	5	200	—	260	—	
		10	110	—	130	—	
Clear Pulse Width	t_{CLR}	5	110	—	135	—	
		10	60	—	75	—	
Data-In to Clock Fall Setup Time	t_{DS}	5	-10	—	-10	—	
		10	-5	—	-5	—	
Data Hold from Write Termination	t_{DH}	5	130	—	170	—	
		10	70	—	90	—	
Select-After Clock-Fall Hold Time	t_{SH}	5	0	—	0	—	
		10	0	—	0	—	
Propagation Delay Times:		5	—	215	—	290	
Clear to Data	t_{RDO}	10	—	140	—	190	
Write to Data Out	t_{WDO}	5	—	250	—	350	
		10	—	130	—	190	
Data In to Data Out	t_{DDO}	5	—	150	—	200	
		10	—	80	—	100	
Clear to SR	t_{RSR}	5	—	175	—	240	
		10	—	120	—	160	
Clock to SR	t_{CSR}	5	—	170	—	240	
		10	—	90	—	120	
Deselect to SR	t_{SSR}	5	—	170	—	240	
		10	—	90	—	120	

†Time required by a device to allow for the indicated function.



CLOCK	†CS1-CS2	CLEAR	Data Out Equals
0	X	0	0
0	X	1	Data Latch
X	0	1	Data Latch
1	1	X	Data In

†CS1 · CS2 = CS1 = 0, CS2 = 1

Fig. 4 - Mode = 1 output port timing waveforms and truth tables.

CDP1853/3, CDP1853C/3

High-Reliability CMOS N-Bit 1-of-8 Decoders

Features:
- *Provides direct control of up to 7 input and 7 output devices when used with a CDP1800-series microprocessor*
- *CHIP ENABLE (CE) allows easy expansion for multi-level I/O systems*

The RCA-CDP1853/3 and CDP1853C/3 are high-reliability 1-of-8 decoders designed for use in general-purpose microprocessor systems. These devices, which are functionally identical, are specifically designed for use as gated N-bit decoders and interface directly with the 1800-series microprocessors without additional components. The CDP1853/3 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1853C/3 has a recommended operating voltage range of 4 to 6.5 volts.

When CHIP ENABLE (CE) is high, the selected output will be true (high) from the trailing edge of CLOCK A (high-to-low transition) to the trailing edge of CLOCK B (high-to-low transition). All outputs will be low when the device is not selected (CE=0) and during conditions of CLOCK A and CLOCK B as shown in Fig. 2 when used with the 1800-series microprocessor. The CDP1853/3 inputs N0, N1, N2, CLOCK A, and CLOCK B are connected to outputs N0, N1, N2, TPA, and TPB respectively, when used to decode I/O commands as shown in Fig. 5. The CHIP ENABLE (CE) input provides the capability for multiple levels of decoding as shown in Fig. 6. The CDP1853/3 can also be used as a general-purpose 1-of-8 decoder for I/O and memory system applications as shown in Fig. 4.

The CDP1853/3 and CDP1853C/3 are supplied in hermetic 16-lead dual-in-line ceramic packages (D suffix). Other package styles may be available on a special-order basis.

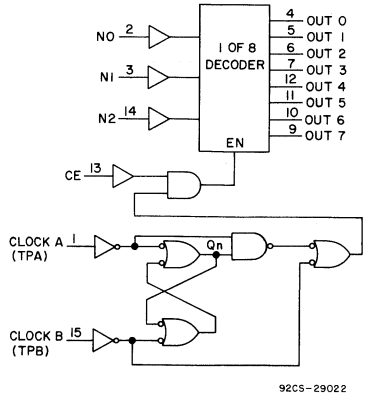
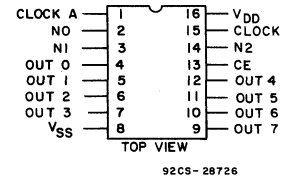


Fig. 1 - CDP1853 functional diagram.



TERMINAL ASSIGNMENT

TRUTH TABLE

CE	CL A	CL B	EN
1	0	0	Qn-1*
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

N2	N1	N0	EN	0	1	2	3	4	5	6	7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

1=High level 0=Low level X=Don't care

*Qn-1=Enable remains in previous state.

CDP1853/3, CDP1853C/3

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CONDITIONS			LIMITS				UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	-55°C, +25°C		+125°C		
					Min.	Max.	Min.	Max.	
Quiescent Device Current	I_{SS}*	—	0, 5	5	-50	—	-100	—	μA
		—	0, 10	10	-500	—	-1000	—	
Output Low Drive (Sink) Current	I_{OL}	0.4	—	5	2.3	—	1.6	—	mA
		0.5	—	10	3.7	—	2.6	—	
Output High Drive (Source) Current	I_{OH}	4.6	—	5	—	-1.7	—	-1.2	
		9.5	—	10	—	-3.7	—	-2.6	
Output Voltage Low-Level	V_{OL}**	—	0, 5	5	—	0.1	—	0.2	V
		—	0, 10	10	—	0.1	—	0.2	
Output Voltage High-Level	V_{OH}**	—	0, 5	5	4.9	—	4.8	—	
		—	0, 10	10	9.9	—	9.8	—	
Input Low Voltage	V_{IL}	0.8, 4.2	—	5	—	1.5	—	1.5	
		1, 9	—	10	—	3	—	3	
Input High Voltage	V_{IH}	0.8, 4.2	—	5	3.5	—	3.5	—	
		1, 9	—	10	7	—	7	—	
Input Leakage Low	I_{IL}	—	0	5	-1	—	-5	—	μA
		—	0	10	-1	—	-5	—	
Input Leakage High	I_{IH}	—	5	5	—	1	—	5	
		—	10	10	—	1	—	5	
Input Capacitance	C_{IN}**	—	—	—	—	10	—	10	pF
Output Capacitance	C_{OUT}**	—	—	—	—	15	—	15	

*The CDP1853C meets all 5-volt static electrical characteristics of the CDP1853 except quiescent device current for which the limits are: I_{SS} = -500 μA @ -55°C and +25°C and I_{SS} = -1000 μA @ +125°C.

**Guaranteed but not tested.

DYNAMIC ELECTRICAL CHARACTERISTICS, See Fig. 2, C_L = 100 pF, t_r,t_f = 15 ns

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			Min.	Max.	Min.	Max.	
Propagation Delay Time:		5	—	175	—	275	ns
Chip Enable (CE) to Output High	t_{EOH}	10	—	90	—	150	
Disable to Output Low	t_{EOL}	5	—	295	—	400	
		10	—	200	—	250	
N Input to Output	t_{NO}	5	—	225	—	315	
		10	—	120	—	165	
Clock A to Output High	t_{AO}	5	—	210	—	300	
		10	—	110	—	150	
Clock B to Output Low	t_{BO}	5	—	295	—	400	
		10	—	200	—	250	
Pulse Width:		5	50	—	75	—	
Clock A	t_{CACA}	10	25	—	50	—	
Clock B	t_{CBCB}	5	50	—	75	—	
		10	25	—	50	—	

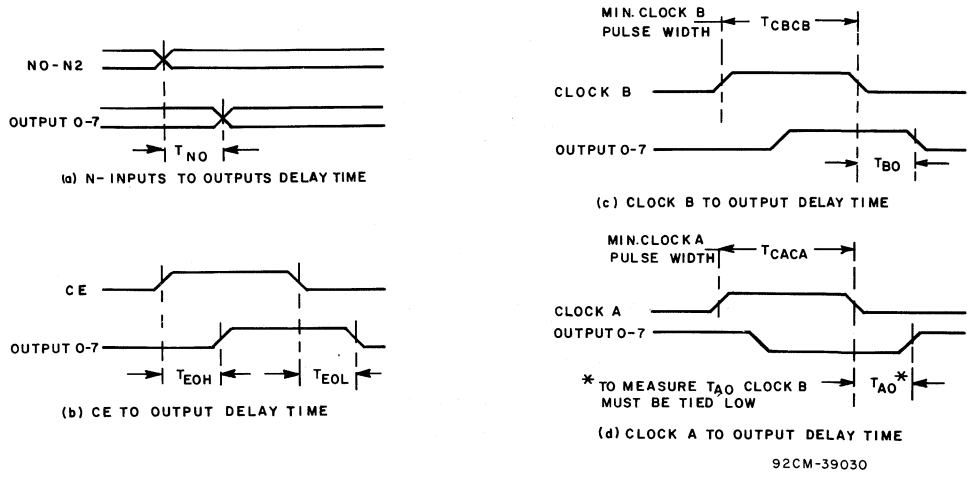


Fig. 2 - Propagation delay time diagrams.

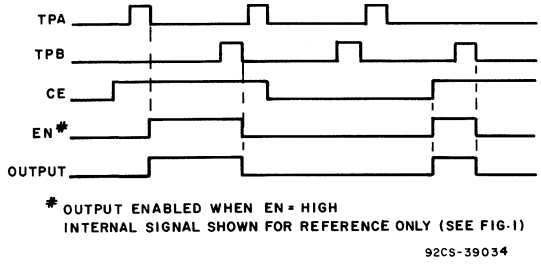


Fig. 3 - Timing diagram.

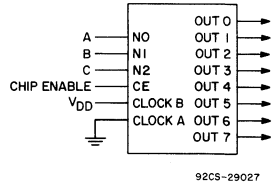
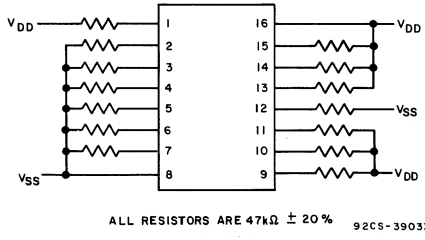


Fig. 4 - N-bit decoder used as a 1 of 8 decoder.



Type	V_{DD}	Temp.	Time
CDP1853	11±0.5 V	+125°C	160 hrs.
CDP1853C	7±0.5 V	+125°C	160 hrs.

Bias/static burn-in circuit.

CDP1853/3, CDP1853C/3

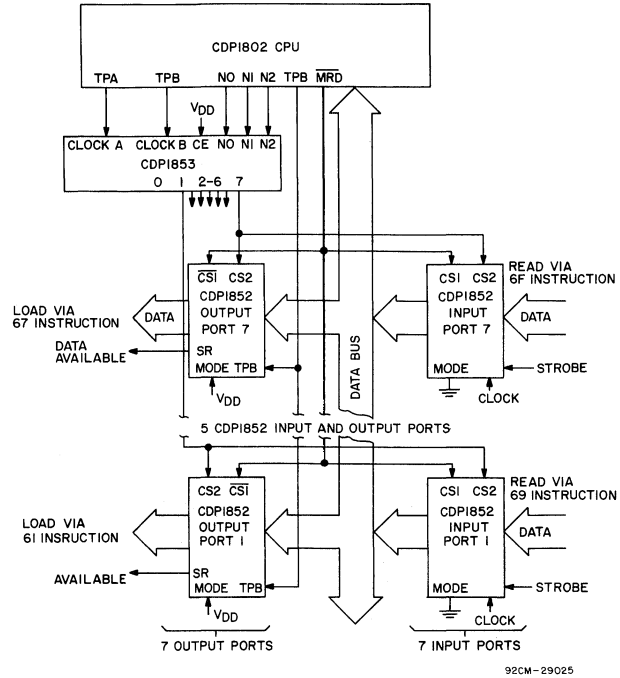


Fig. 5 - N-bit decoder in a one-level I/O system.

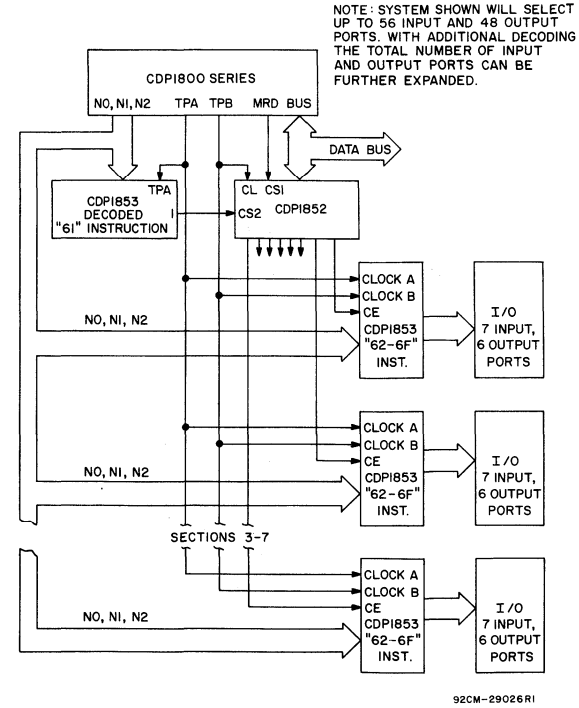


Fig. 6 - Two-level I/O using CDP1853 and CDP1852.

Advance Information/
Preliminary Data

CDP1854A/3, CDP1854AC/3

High-Reliability CMOS Programmable Universal Asynchronous Receiver/Transmitter (UART)

Features:

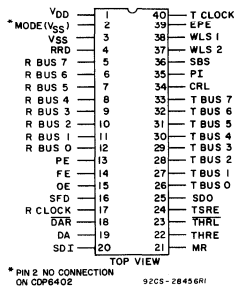
- *Two operating modes:*
  Mode 0-functionally compatible with industry types such as the TR1602A
  Mode 1-interfaces directly with CDP1800-series microprocessors without additional components
- *Full- or half-duplex operation*
- *Parity, framing, and overrun error detection*
- *Fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1½, or 2 stop bits*

The RCA CDP1854A/3 and CDP1854C/3 are high-reliability silicon-gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data. For example, these UARTs can be used to interface between a peripheral or terminal with serial I/O ports and the 8-bit CDP1800-series microprocessor parallel data bus system. The CDP1854A/3 is capable of full duplex operation, i.e., simultaneous conversion of serial input data to parallel output data and parallel input data to serial output data.

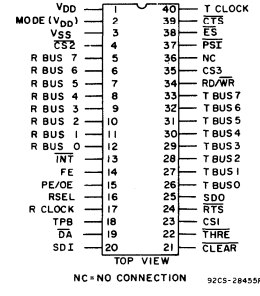
The CDP1854A/3 UART can be programmed to operate in one of two modes by using the mode control input. When the mode input is high (MODE = 1), the CDP1854A/3 is directly compatible with the CDP1800-series microprocessor system without additional interface circuitry. When the mode input is low (MODE = 0), the device is functionally compatible with industry standard UART's such as the TR1602A. It is also pin compatible with these types, except that pin 2 is used for the mode control input instead of a V_{GG} = -12 V supply connection.

The CDP1854A/3 and the CDP1854AC/3 are functionally identical. The CDP1854A/3 has a recommended operating-voltage range of 4-10.5 volts, and the CDP1854AC/3 has a recommended operating-voltage range of 4-6.5 volts.

The CDP1854A/3 and CDP1854AC/3 are supplied in hermetic 40-lead dual-in-line ceramic packages (D suffix). Other package styles may be available on a special order basis.



Mode 0
TERMINAL ASSIGNMENT



Mode 1
TERMINAL ASSIGNMENT

CDP1854A/3, CDP1854AC/3

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS				UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55°C, +25°C		+125°C		
				Min.	Max.	Min.	Max.	
Quiescent Device Current, I_{DD}	—	0, 5	5	—	500	—	1000	μA
	—	0, 10	10	—	500	—	1000	
Output Low Drive (Sink) Current, I_{OL}	0.4	0, 5	5	0.75	—	0.5	—	mA
	0.5	0, 10	10	1.80	—	1.2	—	
Output High Drive (Source) Current, I_{OH}	4.6	0, 5	5	—	-0.5	—	-0.35	mA
	9.5	0, 10	10	—	-1.0	—	-0.70	
Output Voltage High-Level, V_{OH}*	—	0, 5	5	—	0.1	—	0.2	V
	—	0, 10	10	—	0.1	—	0.2	
Output Voltage High-Level, V_{OH}	—	0, 5	5	4.9	—	4.8	—	
	—	0, 10	10	9.9	—	9.8	—	
Input Low Voltage, V_{IL}	0.5, 4.5	—	5	—	1.5	—	1.5	V
	0.5, 9.5	—	10	—	3	—	3	
Input High Voltage, V_{IH}	0.5, 4.5	—	5	3.5	—	3.5	—	
	0.5, 9.5	—	10	7	—	7	—	
Input Leakage Current, I_{IN}	—	0, 5	5	—	±1	—	±5	μA
	—	0, 10	10	—	±1	—	±5	
3-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	—	±1	—	±10	μA
	0, 10	0, 10	10	—	±1	—	±10	
Input Capacitance, C_{IN}*	—	—	—	—	10	—	10	pF
Output Capacitance, C_{OUT}*	—	—	—	—	15	—	15	

*Guaranteed but not tested

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	-55°C, +25°C		+125°C		
		Min.	Max.	Min.	Max.	
DC Operating-Voltage Range	—	4	10.5	4	6.5	V
Input Voltage Range	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Baud Rate (Receive or Transmit)	5	—	250	—	215	K bits
	10	—	520	—	430	/sec

Mode Input High (Mode = 1)

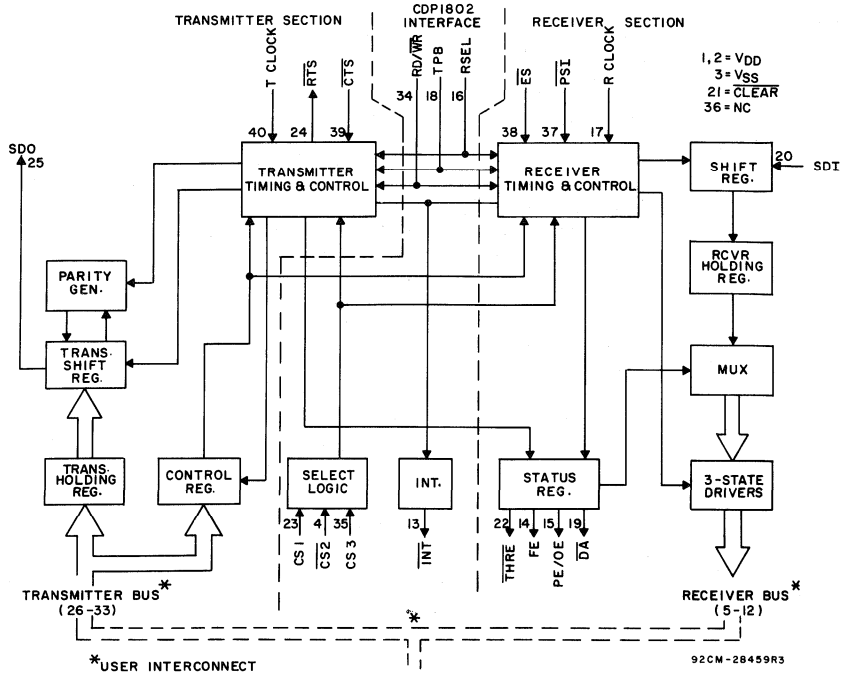


Fig. 1 — Mode 1 block diagram (CDP1800-series microprocessor compatible).

Functional Definitions for CDP1854A Terminals
Mode 1
CDP1800-Series Microprocessor Compatible
SIGNAL: FUNCTION

V_{DD}:
Positive supply voltage

MODE SELECT (MODE):
A high-level voltage at this input selects CDP1800-series microprocessor Mode operation.

V_{SS}:
Ground

$\overline{\text{CHIP SELECT 2}}$ ($\overline{\text{CS2}}$):
A low-level voltage at this input together with CS1 and CS3 selects the CDP1854A UART.

RECEIVER BUS (R BUS 7 - R BUS 0):
Receiver parallel data outputs (may be externally connected to corresponding transmitter bus terminals).

$\overline{\text{INTERRUPT}}$ ($\overline{\text{INT}}$):
A low-level voltage at this output indicates the presence of one or more of the interrupt conditions listed in Table I.

FRAMING ERROR (FE):
A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register.

PARITY ERROR or OVERRUN ERROR (PE/OE):
A high-level voltage at this ouitput indicates that either the PE or OE bit in the Status Register has been set (see Status Register Bit Assignment, Table II.

REGISTER SELECT (RSEL):
This input is used to choose either the Control/Status Registers (high input) or the transmitter/receiver data registers (low input) according to the truth table in Table III.

RECEIVER CLOCK (RCLOCK):
Clock input with a frequency 16 times the desired reciever shift rate.

TPB:
A positive input pulse used as a data load or reset strobe.

$\overline{\text{DATA AVAILABLE}}$ ($\overline{\text{DA}}$):
A low-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):
Serial data received on this input line enters the Receiver Shift Register at a point determined by the character length. A high-level input voltage must be present when data is not being received.

$\overline{\text{CLEAR}}$ ($\overline{\text{CLEAR}}$):
A low-level voltage at this input resets the Interrupt Flip-Flop, Receiver Holding Register, Control Register, and Status Register, and sets SERIAL DATA OUT (SDO) high.

$\overline{\text{TRANSMITTER HOLDING REGISTER EMPTY}}$ ($\overline{\text{THRE}}$):
A low-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

CHIP SELECT 1 (CS1):
A high-level voltage at this input together with $\overline{\text{CS2}}$ and CS3 selects the UART.

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REQUEST TO SEND ($\overline{RTS}$):
This output signal tells the peripheral to get ready to receive data. CLEAR TO SEND ($\overline{CTS}$) is the response from the peripheral. $\overline{RTS}$ is set to a low-level voltage when data is latched in the Transmitter Holding Register or TR is set high, and is reset high when both the Transmitter Holding Register and Transmitter Shift Register are empty and TR is low.

SERIAL DATA OUTPUT (SDO):
The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s) are serially shifted out on this output. When no character is being transmitted, a high level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):
Transmitter parallel data input. These may be externally connected to corresponding Receiver bus terminals.

RD/$\overline{WR}$:
A low-level voltage at this input gates data from the transmitter bus to the Transmitter Holding Register or the Control Register as chosen by register select. A high-level voltage gates data from the Receiver Holding Register or the Status Register, as chosen by register select, to the receiver bus.

CHIP SELECT 3 (CS3):
With high-level voltage at this input together with CS1 and $\overline{CS2}$ selects the UART.

PERIPHERAL STATUS INTERRUPT ($\overline{PSI}$):
A high-to-low transition on this input line sets a bit in the Status Register and causes an INTERRUPT ($\overline{INT}$ = low).

EXTERNAL STATUS ($\overline{ES}$):
A low-level voltage at this input sets a bit in the Status Register.

CLEAR TO SEND ($\overline{CTS}$):
When this input from peripheral is high, transfer of a character to the Transmitter Shift Register and shifting of serial data out is inhibited.

TRANSMITTER CLOCK (TCLOCK):
Clock input with a frequency 16 times the desired transmitter shift rate.

Table I — Interrupt Set and Reset Conditions

SET* (INT = LOW)	RESET (INT = HIGH)	
CAUSE	**CONDITION**	**TIME**
DA (Receipt of data)	Read of data	TPB leading edge
THRE** (Ability to reload)	Read of status or write of character	TPB leading edge
THRE•TSRE (Transmitter done)	Read of status or write of character	TPB leading edge
$\overline{PSI}$ (Negative edge)	Read of status	TPB trailing edge
$\overline{CTS}$ (Positive edge when $\overline{THRE•TSRE}$)	Read of status	TPB leading edge

*Interrupts will occur only after the IE bit in the Control Register (see Table IV) has been set.

**THRE will cause an interrupt only after the TR bit in the Control Register (see Table IV) has been set.

Table II — Status Register Bit Assignment

Bit	7	6	5	4	3	2	1	0
Signal	THRE	TSRE	PSI	ES	FE	PE	OE	DA
Also Available at Terminal	22*	—	—	—	14	15	15	19*

*Polarity reversed at output terminal.

Bit Signal: Function

0 — DATA AVAILABLE (DA):
When set high, this bit indicates that an entire character has been received and transferred to the Receiver Holding Register. This signal is also available at Term. 19 but with its polarity reversed.

1 — OVERRUN ERROR (OE):
When set high, this bit indicates that the Data Available bit was not reset before the next character was transferred to the Receiver Holding Register. This signal OR'ed with PE is output at Term. 15.

2 — PARITY ERROR (PE):
When set high, this bit indicates that the received parity bit does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal OR'ed with OE is output at Term. 15.

3 — FRAMING ERROR (FE):
When set high, this bit indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal is also available at Term. 14.

4 — EXTERNAL STATUS (ES):
This bit is set high by a low-level input at Term. 38 ($\overline{ES}$).

5 — PERIPHERAL STATUS INTERRUPT (PSI):
This bit is set high by a high-to-low voltage transition of Term. 37 ($\overline{PSI}$). The INTERRUPT output (Term. 13) is also asserted ($\overline{INT}$ = low) when this bit is set.

6 — TRANSMITTER SHIFT REGISTER EMPTY (TSRE):
When set high, this bit indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains set until the start of transmission of the next character.

7 — TRANSMITTER HOLDING REGISTER EMPTY (THRE):
When set high, this bit indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character. Setting this bit also sets the $\overline{THRE}$ output (Term. 22) low and causes an INTERRUPT ($\overline{INT}$ = low), if TR is high.

Description of Mode 1 Operation CDP1800-Series Microprocessor Compatible (Mode Input = V_{DD})

1. Initialization and Controls

In the CDP1800-series microprocessor compatible mode, the CDP1854A is configured to receive commands and send status via the microprocessor data bus. The register connected to the transmitter bus or the receiver bus is determined by the RD/$\overline{WR}$ and RSEL inputs as follows:

Table III — Register Selection Summary

RSEL	RD/$\overline{WR}$	Function
Low	Low	Load Transmitter Holding Register from Transmitter Bus
Low	High	Read Receiver Holding Register from Receiver Bus
High	Low	Load Control Register from Transmitter Bus
High	High	Read Status Register from Receiver Bus

In this mode the CDP1854A is compatible with a bidirectional bus system. The receiver and transmitter buses are connected to the bus. CDP1800-series microprocessor I/O control output signals can be connected directly to the CDP1854A inputs as shown in Fig. 2. The CLEAR input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting SERIAL DATA OUT (SDO) high. The Control Register is loaded from the Transmitter Bus in order to determine the operating configuration for the UART. Data is transferred from the Transmitter Bus inputs to the Control Register during TPB when the UART is selected (CS1•$\overline{CS2}$•CS3=1) and the Control Register is designated (RSEL=H, RD/$\overline{WR}$=L). The CDP1854A also has a Status Register which can be read onto the Receiver Bus (R BUS 0 - R BUS 7) in order to determine the status of the UART. Some of these status bits are also available at separate terminals as indicated in Table II.

2. Transmitter Operation

Before beginning to transmit, the TRANSMIT REQUEST (TR) bit in the Control Register (see bit assignment, Table IV) is set. Loading the Control Register with TR=1 (bit 7 = high) inhibits changing the other control bits. Therefore two loads are required: one to format the UART, the second to set TR. When TR has been set, a $\overline{TRANSMITTER\ HOLDING\ REGISTER\ EMPTY}$ ($\overline{THRE}$) interrupt will occur, signalling the microprocessor that the Transmitter Holding Register is empty and may be loaded. Setting TR also causes assertion of a low-level on the REQUEST TO SEND ($\overline{RTS}$) output to the peripheral. It is not necessary to set TR for proper operation for the UART. If desired, it can be used to enable $\overline{THRE}$ interrupts and to generate the $\overline{RTS}$ signal. The Transmitter Holding Register is loaded from the bus by TPB during execution of an output instruction. The CDP1854A is selected by CS1•$\overline{CS2}$•CS3=1, and the Holding Register is selected by RSEL=L and RD/$\overline{WR}$=L. When the $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) input, which can be connected to a peripheral device output, goes low, the Transmitter Shift Register will be loaded from the Transmitter Holding Register and data transmission will begin. If $\overline{CTS}$ is always low, the Transmitter Shift Register will be loaded on the first high-to-low edge of the clock which occurs at least ½ clock period after the trailing edge of TPB and transmission of a start bit will occur ½ clock period later (see Fig. 3). Parity (if programmed) and stop bit(s) will be transmitted following the last data bit. If the word length selected is less than 8 bits, the most significant unused bits in the transmitter shift register will not be transmitted.

One transmitter clock period after the Transmitter Shift Register is loaded from the Transmitter Holding Register, the $\overline{THRE}$ signal will go low and an interrupt will occur ($\overline{INT}$ goes low). The next character to be transmitted can then be loaded into the Transmitter Holding Register for transmission with its start bit immediately following the last stop bit of the previous character. This cycle can be repeated until the last character is transmitted, at which time a final THRE•TSRE interrupt will occur. This interrupt signals the microprocessor that TR can be turned off. This is done by reloading the original control byte in the Control Register with the TR bit = 0, thus terminating the $\overline{REQUEST\ TO\ SEND}$ ($\overline{RTS}$) signal.

SERIAL DATA OUT (SDO) can be held low by setting the BREAK bit in the Control Register (see Table IV). SDO is held low until the BREAK bit is reset.

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After detection of the first

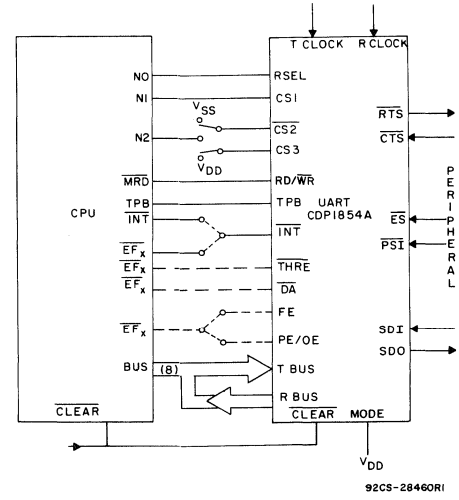

Fig. 2 — Recommended CDP1800-series connection, Mode 1 (non-interrupt driven system).

high-to-low transition on the SDI line, a valid start bit is verified by checking for a low-level input 7½ receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed) and stop bit(s) are shifted into the Receiver Shift Register by clock pulse 7½ in each bit time. The parity bit (if programmed) is checked and receipt of a valid stop bit is verified. On count 7½ of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output level) are loaded into the unused most significant bits. IF DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) status bit is set. One half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) status bits become valid for the character in the Receiver Holding Register. At this time, the Data Available status bit is also set and the DATA AVAILABLE (DA) and INTERRUPT (INT) outputs go low, signalling the microprocessor that a received character is ready. The microprocessor responds by executing an input instruction. The UART's 3-state bus drivers are enabled when the UART is selected (CS1•$\overline{CS2}$•CS3=1) and RD/$\overline{WR}$= high. Data is read when RSEL = low. When reading data, TPB latches data in the microprocessor and resets $\overline{DATA\ AVAILABLE}$ ($\overline{DA}$) in the UART. The preceding sequence is repeated for each serial character which is received from the peripheral.

4. Peripheral Interface

In addition to serial data in and out, four signals are provided for communication with a peripheral. The $\overline{REQUEST\ TO\ SEND}$ ($\overline{RTS}$) output signal alerts the peripheral to get ready to receive data. The $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) input signal is the response, signalling that the peripheral is ready. The $\overline{EXTERNAL\ STATUS}$ ($\overline{ES}$) input latches a peripheral status level, and the $\overline{PERIPHERAL\ STATUS\ INTERRUPT}$ ($\overline{PSI}$) input senses a status edge (high-to-low) and also generates an interrupt. For example, the modem $\overline{DATA\ CARRIER\ DETECT}$ line could be connected to the $\overline{PSI}$ input on the UART in order to signal the microprocessor that transmission failed because of loss of the carrier on the communications line. The PSI and ES bits are stored in the Status Register (see Table II).

Table IV — Control Register Bit Assignment

Bit	7	6	5	4	3	2	1	0
Signal	TR	BREAK	IE	WLS2	WLS1	SBS	EPE	PI

Bit Signal: Function

0 — PARITY INHIBIT (PI):
When set high parity generation and verification are inhibited and the PE Status bit is held low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission, and EPE is ignored.

1 — EVEN PARITY ENABLE (EPE):
When set high, even parity is generated by the transmitter and checked by the receiver. When low, odd parity is selected.

2 — STOP BIT SELECT (SBS):
See table below.

3 — WORD LENGTH SELECT 1 (WLS1):
See table below.

4 — WORD LENGTH SELECT 2 (WLS2):
See table below.

5 — INTERRUPT ENABLE (IE):
When set high $\overline{THRE}$, DA, THRE•TSRE, $\overline{CTS}$, and PSI interrupts are enabled (see Interrupt Conditions, Table I).

6 — TRANSMIT BREAK (BREAK):
Holds SDO low when set. Once the break bit in the control register has been set high, SDO will stay low until the break bit is reset low and one of the following occurs: $\overline{CLEAR}$ goes low; $\overline{CTS}$ goes high; or a word is transmitted. (The transmitted word will not be valid since there can be no start bit if SDO is already low. SDO can be set high without intermediate transitions by transmitting a word consisting of all zeros).

7 — TRANSMIT REQUEST (TR):
When set high, $\overline{RTS}$ is set low and data transfer through the transmitter is initiated by the initial $\overline{THRE}$ interrupt. (When loading the Control Register from the bus, this (TR) bit inhibits changing of other control flip-flops).

Bit 4	Bit 3	Bit 2	Function
WLS2	WLS1	SBS	
0	0	0	5 data bits, 1 stop bit
0	0	1	5 data bits, 1.5 stop bits
0	1	0	6 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	1	1	8 data bits, 2 stop bits

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DYNAMIC ELECTRICAL CHARACTERISTICS at t_r, t_f = 15 ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100 pF, see Fig. 3.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			Min.	Max.	Min.	Max.	
Transmitter Timing — Mode 1							
Clock Period	t_{CC}	5	240	—	280	—	ns
		10	120	—	145	—	
Pulse Width:		5	105	—	125	—	ns
Clock Low Level	t_{CL}	10	55	—	65	—	
Clock High Level	t_{CH}	5	135	—	155	—	ns
		10	65	—	80	—	
TPB	t_{TT}	5	125	—	165	—	ns
		10	70	—	80	—	
Propagation Delay Time:		5	—	425	—	485	ns
Clock to Data Start Bit	t_{CD}	10	—	205	—	235	
TPB to $\overline{\text{THRE}}$	t_{TTH}	5	—	315	—	380	ns
		10	—	155	—	185	
Clock to $\overline{\text{THRE}}$	t_{CTH}	5	—	335	—	390	ns
		10	—	160	—	190	

DYNAMIC ELECTRICAL CHARACTERISTICS at t_r, t_f = 15 ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100 pF, see Fig. 4.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			Min.	Max.	Min.	Max.	
Receiver Timing — Mode 1							
Clock Period	t_{CC}	5	240	—	280	—	ns
		10	120	—	145	—	
Pulse Width:		5	105	—	125	—	ns
Clock Low Level	t_{CL}	10	55	—	65	—	
Clock High Level	t_{CH}	5	135	—	155	—	ns
		10	65	—	80	—	
TPB	t_{TT}	5	125	—	165	—	ns
		10	70	—	80	—	
Setup Time:		5	105	—	120	—	ns
Data Start Bit to Clock	t_{DC}	10	65	—	70	—	
Propagation Delay Time:		5	—	295	—	340	ns
TPB to $\overline{\text{DATA AVAILABLE}}$	t_{TDA}	10	—	150	—	170	
Clock to $\overline{\text{DATA AVAILABLE}}$	t_{CDA}	5	—	305	—	355	ns
		10	—	150	—	170	
Clock to Overrun Error	t_{COE}	5	—	305	—	330	ns
		10	—	150	—	175	
Clock to Parity Error	t_{CPE}	5	—	305	—	330	ns
		10	—	150	—	175	
Clock to Framing Error	t_{CFE}	5	—	280	—	330	ns
		10	—	145	—	165	

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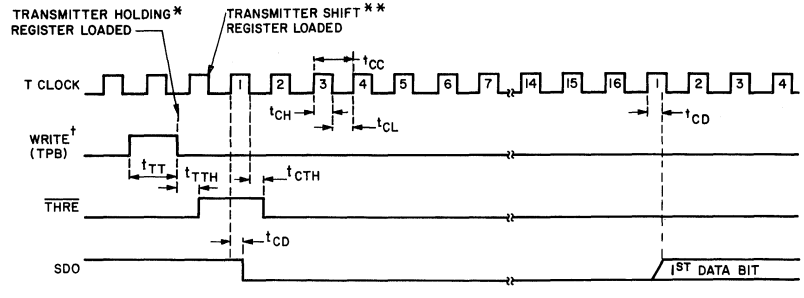


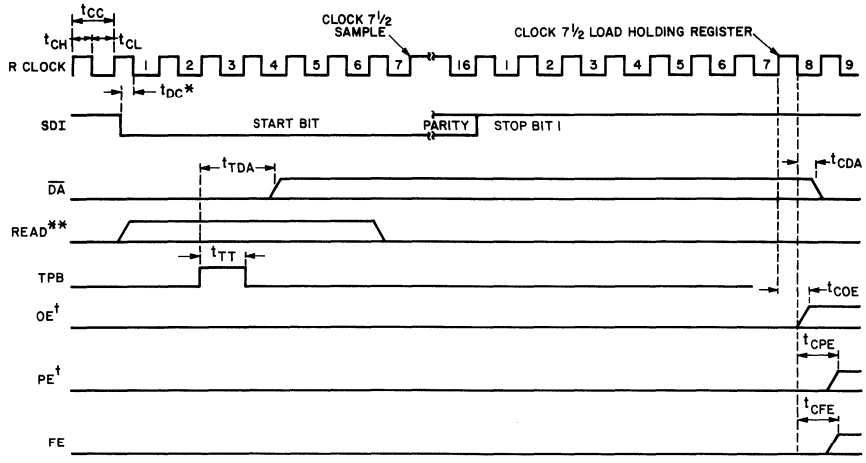
* THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF TPB.

** THE TRANSMITTER SHIFT REGISTER IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD + t_{TC} AFTER THE TRAILING EDGE OF TPB, AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER.

† WRITE IS THE OVERLAP OF TPB, CSI, AND CS3 = 1 AND $\overline{CS3}$, RD / $\overline{WR}$ = 0.

92CM-31878R1

Fig. 3 — Transmitter timing diagram — Mode 1.



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

** READ IS THE OVERLAP OF CSI, CS3, RD / $\overline{WR}$ = 1 AND $\overline{CS2}$ = 0. IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE.

† OE AND PE SHARE TERMINAL 15 AND ARE ALSO AVAILABLE AS TWO SEPARATE BITS IN THE STATUS REGISTER.

92CM-31880

Fig. 4 — Mode 1 receiver timing diagram.

Functional Definitions for CDP1854A/3 Terminals Standard Mode 0

SIGNAL: FUNCTION

V_{DD}:
Positive supply voltage.

MODE SELECT (MODE):
A low-level voltage at this input selects Standard Mode 0 Operation.

V_{SS}:
Ground.

RECEIVER REGISTER DISCONNECT (RRD):
A high-level voltage applied to this input disconnects the Receiver Holding Register from the Receiver Bus.

RECEIVER BUS (R BUS 7 - R BUS 0);
Receiver parallel data outputs.

PARITY ERROR (PE):
A high-level voltage at this output indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This output is updated each time a character is transferred to the Receiver Holding Register. PE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

FRAMING ERROR (FE):
A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

OVERRUN ERROR (OE):
A high-level voltage at this output indicates that the DATA AVAILABLE (DA) flag was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

STATUS FLAG DISCONNECT (SFD):
A high-level voltage applied to this input disables the 3-state output drivers for PE, FE, OE, DA, and THRE, allowing these status outputs to be bus connected.

RECEIVER CLOCK (RCLOCK):
Clock input with a frequency 16 times the desired receiver shift rate.

$\overline{\text{DATA AVAILABLE RESET}}$ ($\overline{\text{DAR}}$):
A low-level voltage applied to this input resets the DA flip-flop.

DATA AVAILABLE (DA):
A high-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):
Serial data received at this input enters the receiver shift register at a point determined by the character length. A high-level voltage must be present when data is not being received.

MASTER RESET (MR):
A high-level voltage at this input resets the Receiver Holding Register, Control Register, and Status Register, and sets the serial data output high.

TRANSMITTER HOLDING REGISTER EMPTY (THRE):
A high-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

$\overline{\text{TRANSMITTER HOLDING REGISTER LOAD}}$ ($\overline{\text{THRL}}$):
A low-level voltage applied to this input enters the character on the bus into the Transmitter Holding Register. Data is latched on the trailing edge of this signal.

TRANSMITTER SHIFT REGISTER EMPTY (TSRE):
A high-level voltage at this output indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains at this level

DYNAMIC ELECTRICAL CHARACTERISTICS at t_r, t_f = 15 ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100 pF, see Fig. 5.

CHARACTERISTIC		V_{DD} (V)	LIMITS -55°C, +25°C Min.	-55°C, +25°C Max.	+125°C Min.	+125°C Max.	UNITS
CPU Interface — WRITE Timing — Mode 1							
Pulse Width TPB	t_{TT}	5	125	—	165	—	ns
		10	70	—	80	—	
Setup Time: RSEL to Write	t_{RSW}	5	20	—	10	—	ns
		10	25	—	25	—	
Data to Write	t_{DW}	5	65	—	75	—	ns
		10	45	—	50	—	
Hold Time: RSEL after Write	t_{WRS}	5	-10	—	-20	—	ns
		10	5	—	5	—	
Data after Write	t_{WD}	5	95	—	105	—	ns
		10	55	—	55	—	

DYNAMIC ELECTRICAL CHARACTERISTICS at t_r, t_f = 15 ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100 pF, see Fig. 6.

CHARACTERISTIC		V_{DD} (V)	LIMITS -55°C, +25°C Min.	-55°C, +25°C Max.	+125°C Min.	+125°C Max.	UNITS
CPU Interface — READ Timing — Mode 1							
Pulse Width TPB	t_{TT}	5	125	—	165	—	ns
		10	70	—	80	—	
Setup Time: RSEL to TPB	t_{RST}	5	15	—	0	—	ns
		10	20	—	10	—	
Hold Time: RSEL after TPB	t_{TRS}	5	-10	—	-25	—	ns
		10	5	—	0	—	
Propagation Delay Time: Read to Data Valid Time	t_{RDV}	5	—	360	—	420	ns
		10	—	165	—	195	
RSEL to Data Valid Time	t_{RSDV}	5	—	250	—	295	ns
		10	—	125	—	145	

CDP1854A/3, CDP1854AC/3

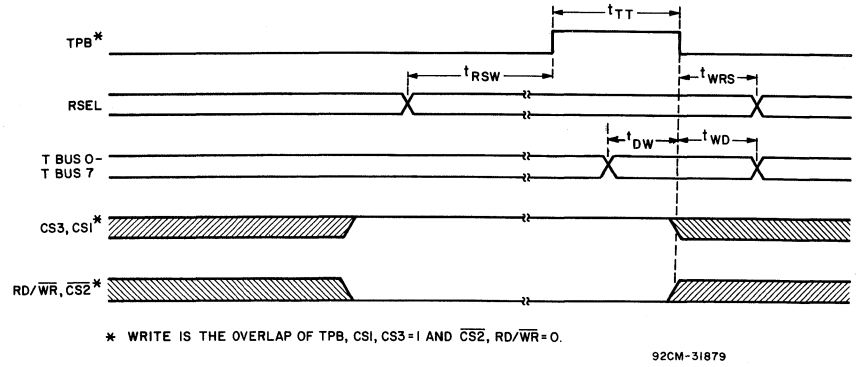


Fig. 5 — Mode 1 CPU interface (WRITE) timing diagram.

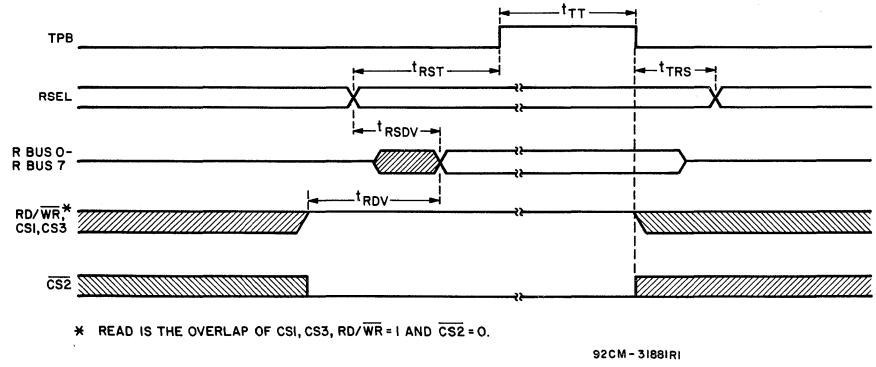


Fig. 6 — Mode 1 CPU interface (READ) timing diagram.

until the start of transmission of the next character.

SERIAL DATA OUTPUT (SDO):
The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop (bit(s)) are serially shifted out on this output. When no character is being transmitted, a high-level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):
Transmitter parallel data inputs.

CONTROL REGISTER LOAD (CRL):
A high-level voltage at this input loads the Control Register with the control bits (PI, EPE, SBS, WLS1, WLS2). This line may be strobed or hardwired to a high-level input voltage.

PARITY INHIBIT (PI):
A high-level voltage at this input inhibits the parity generation and verification circuits and will clamp the PE output low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission.

STOP BIT SELECT (SBS):
This input selects the number of stop bits to be transmitted after the parity bit. A high-level selects two stop bits, a low-level selects one stop bit. Selection of two stop bits with five data bits programmed selects 1.5 stop bits.

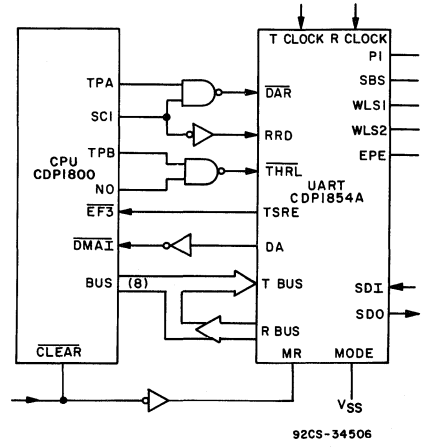


Fig. 7 — Mode 0 connection diagram.

WORD LENGTH SELECT 2 (WLS2):
WORD LENGTH SELECT 1 (WLS1):
These two inputs select the character length (exclusive of parity) as follows:

WLS2	WLS1	Word Length
Low	Low	5 Bits
Low	High	6 Bits
High	Low	7 Bits
High	High	8 Bits

EVEN PARITY ENABLE (EPE):
A high-level voltage at this input selects even parity to be generated by the transmitter and checked by the receiver. A low-level input selects odd parity.

TRANSMITTER CLOCK (TCLOCK):
Clock input with a frequency 16 times the desired transmitter shift rate.

Description of Standard Mode 0 Operation (Mode Input = V_{SS})

1. Initialization and Controls

The MASTER RESET (MR) input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting the SERIAL DATA OUTPUT (SDO) signal high. Timing is generated from the clock inputs, Transmitter Clock (TCLOCK) and Receiver Clock (RCLOCK), at a frequency equal to 16 times the serial data bit rate. When the receiver data input rate and the transmitter data output rate are the same, the TCLOCK and RCLOCK inputs may be connected together. The CONTROL REGISTER LOAD (CRL) input is pulsed to store the control inputs PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECT (SBS), and WORD LENGTH SELECTs (WLS1 and WLS2). These inputs may be hardwired to the proper voltage levels (V_{SS} or V_{DD}) instead of being dynamically set and CRL may be hardwired to V_{DD}. The CDP1854A/3 is then ready for transmitter and/or receiver operation.

2. Transmitter Operation

For the transmitter timing refer to Fig. 10. At the beginning of a typical transmitting sequence the Transmitter Holding Register is empty (THRE is HIGH). A character is transferred from the transmitter bus to the Transmitter holding Register by applying a low pulse to the $\overline{\text{TRANSMITTER HOLDING REGISTER LOAD (THRL)}}$ input causing THRE to go low. If the Transmitter Shift Register is empty (TSRE is HIGH) and the clock is low, on the next high-to-low transition of the clock the character is loaded into the Transmitter Shift Register preceded by a start bit. Serial data transmission begins ½ clock period later with a start bit and 5-8 data bits followed by the parity bit (if programmed) and stop bit(s). The THRE output signal goes high ½ clock period later on the high-to-low transition of the clock. When THRE goes high, another character can be loaded into the Transmitter Holding Register for transmission beginning with a start bit immediately following the last stop bit of the previous character. This process is repeated until all characters have been transmitted. When transmission is complete, THRE and Transmitter Shift Register Empty (TSRE) will both be high. The format of serial data is shown in Fig. 12. Duration of each serial output data bit is determined by the transmitter clock frequency (f_{CLOCK}) and will be 16/f CLOCK.

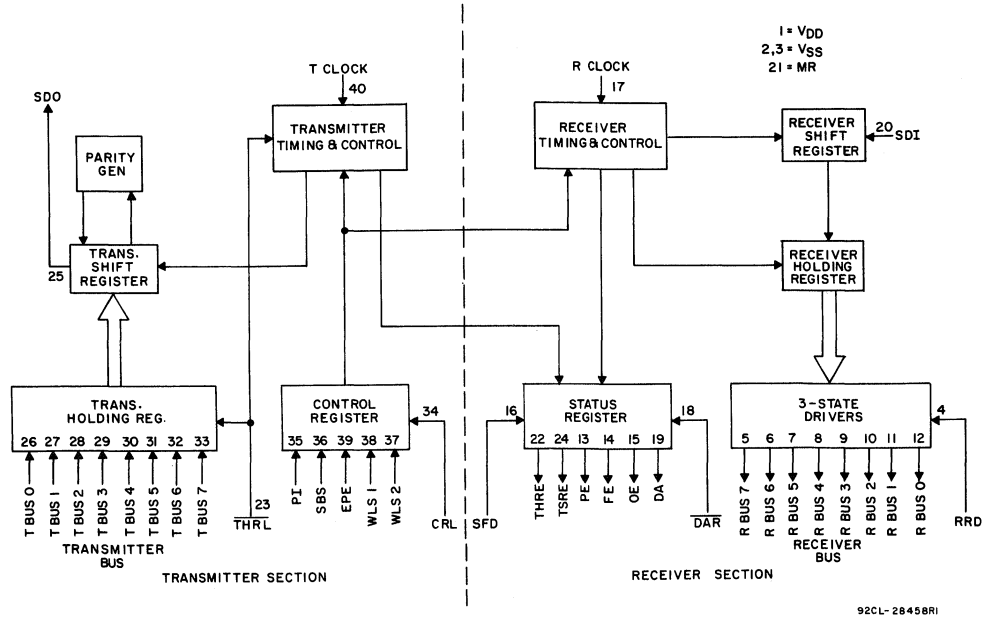


Fig. 8 — Mode 0 block diagram (industry standard compatible).

CDP1854A/3, CDP1854AC/3

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After the detection of a high-to-low transition on the SDI line, a divide-by-16 counter is enabled and a valid start bit is verified by checking for a low-level input 7½ receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed), and stop bit(s) are shifted into the Receiver Shift Register at clock pulse 7½ in each bit time. If programmed, the parity bit is checked, and receipt of a valid stop bit is verified. On count 7½ of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output voltage level) are loaded into the unused most significant bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) signal is raised. One-half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) signals become valid for the character in the Receiver Holding Register. The DA signal is also raised at this time. The 3-state output drivers for DA, OE, PE and FE are enabled when STATUS FLAG DISCONNECT (SFD) is low. When RECEIVER REGISTER DISCONNECT (RRD) goes low, the receiver bus 3-state output drivers are enabled and data is available at the RECEIVER BUS (R BUS 0 - R BUS 7) outputs. Applying a negative pulse to the $\overline{\text{DATA AVAILABLE RESET (DAR)}}$ resets DA. The preceding sequence of operation is repeated for each serial character received. A receiver timing diagram is shown in Fig. 11.

DYNAMIC ELECTRICAL CHARACTERISTICS at t_r, t_f = 15 ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100 pF, see Fig. 9.

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		-55°C, +25°C		+125°C		
		Min.	Max.	Min.	Max.	
Interface Timing — Mode 0						
Pulse Width: CRL t_{CRL}	5	105	—	125	—	ns
	10	55	—	65	—	
Pulse Width: MR t_{MR}	5	340	—	385	—	ns
	10	160	—	175	—	
Setup Time: Control Word to CRL t_{CWC}	5	80	—	85	—	ns
	10	40	—	60	—	
Hold Time: Control Word after CRL t_{CCW}	5	65	—	65	—	ns
	10	45	—	45	—	
Propagation Delay Time: SFD High to SOD t_{SFDH}	5	—	175	—	195	ns
	10	—	105	—	115	
SFD Low to SOD t_{SFDL}	5	165	—	195	—	ns
	10	90	—	105	—	
RRD High to Receiver Register High Impedance t_{RRDH}	5	—	185	—	205	ns
	10	—	110	—	130	
RRD Low to Receiver Register Active t_{RRDL}	5	165	—	195	—	ns
	10	90	—	105	—	

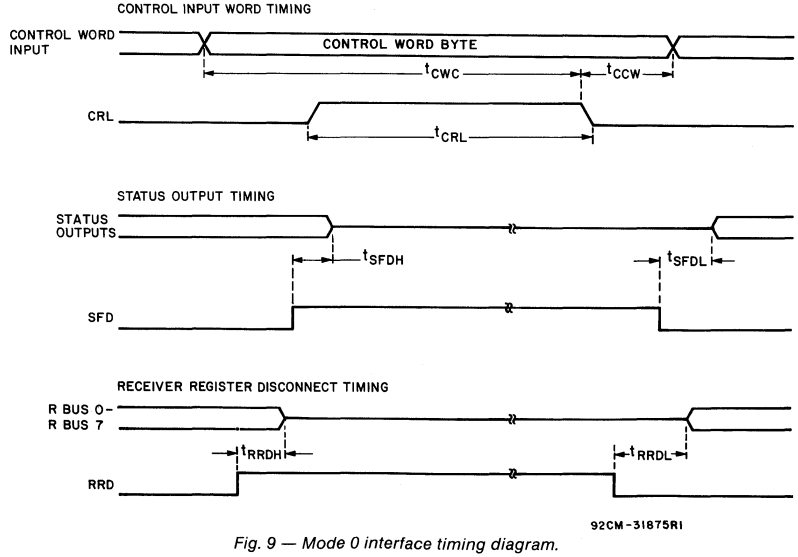
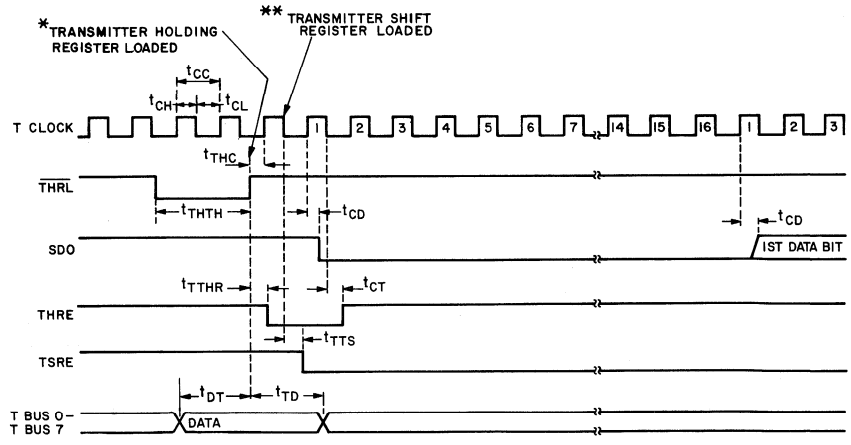


Fig. 9 — Mode 0 interface timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at t_r, t_f = 15 ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100 pF, see Fig. 10.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			Min.	Max.	Min.	Max.	
Transmitter Timing — Mode 0							
Clock Period	t_{CC}	5	240	—	280	—	ns
		10	120	—	145	—	
Pulse Width:		5	105	—	125	—	ns
Clock Low Level	t_{CL}	10	55	—	65	—	
Clock High Level	t_{CH}	5	135	—	155	—	ns
		10	65	—	80	—	
$\overline{THRL}$	t_{THTH}	5	140	—	165	—	ns
		10	80	—	85	—	
Setup Time:		5	205	—	235	—	ns
$\overline{THRL}$ to Clock	t_{THC}	10	120	—	140	—	
Data to $\overline{THRL}$	t_{DT}	5	25	—	30	—	ns
		10	20	—	25	—	
Hold Time:		5	60	—	95	—	ns
Data after $\overline{THRL}$	t_{TD}	10	45	—	75	—	
Propagation Delay Time:		5	—	435	—	505	ns
Clock to Data Start Bit	t_{CD}	10	—	205	—	235	
Clock to THRE	t_{CT}	5	—	345	—	420	ns
		10	—	175	—	200	
$\overline{THRL}$ to THRE	t_{TTHR}	5	—	275	—	325	ns
		10	—	145	—	165	
Clock to TSRE	t_{TTS}	5	—	345	—	405	ns
		10	—	165	—	190	



* THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF $\overline{THRL}$.

** THE TRANSMITTER SHIFT REGISTER, IF EMPTY, IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD + t_{THC} AFTER THE TRAILING EDGE OF $\overline{THRL}$, AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER.

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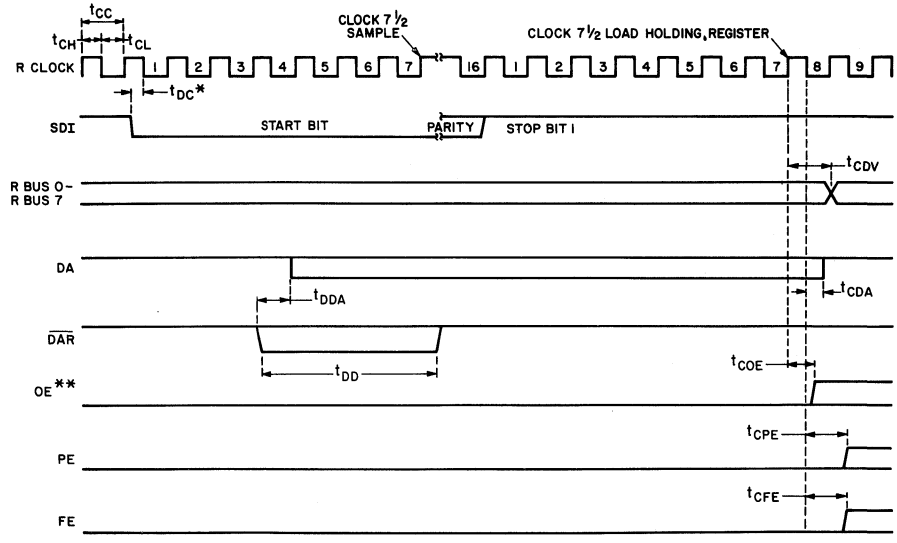
Fig. 10 — Mode 0 transmitter timing diagram.

CDP1854A/3, CDP1854AC/3

DYNAMIC ELECTRICAL CHARACTERISTICS at t_r, t_f = 15 ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100 pF, see Fig. 11.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			Min.	Max.	Min.	Max.	
Receiver Timing — Mode 0							
Clock Period	t_{CC}	5	240	—	280	—	ns
		10	120	—	145	—	
Pulse Width: Clock Low Level	t_{CL}	5	105	—	125	—	ns
		10	55	—	65	—	
Clock High Level	t_{CH}	5	135	—	155	—	ns
		10	65	—	80	—	
$\overline{\text{DATA AVAILABLE RESET}}$	t_{DD}	5	75	—	90	—	ns
		10	45	—	50	—	
Setup Time: Data Start Bit to Clock	t_{DC}	5	105	—	130	—	ns
		10	65	—	85	—	
Propagation Delay Time: $\overline{\text{DATA AVAILABLE RESET}}$ to Data Available	t_{DDA}	5	—	240	—	280	ns
		10	—	130	—	145	
Clock to Data Valid	t_{CDV}	5	—	360	—	420	ns
		10	—	175	—	195	
Clock to Data Available	t_{CDA}	5	—	320	—	375	ns
		10	—	155	—	180	
Clock to Overrun Error	t_{COE}	5	—	365	—	415	ns
		10	—	170	—	190	
Clock to Parity Error	t_{CPE}	5	—	275	—	320	ns
		10	—	135	—	155	
Clock to Framing Error	t_{CFE}	5	—	270	—	320	ns
		10	—	135	—	165	



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

** IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE.

92CM-31877

Fig. 11 — Mode 0 receiver timing diagram.

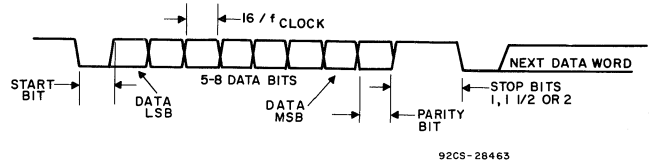
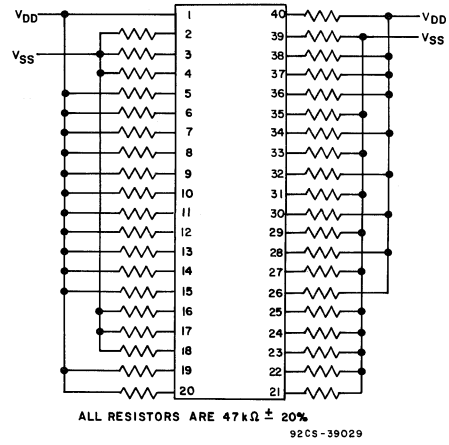


Fig. 12 — Serial data word format.



Type	V_{DD}	Temp.	Time
CDP1854A/3	11 ± 0.5V	+125°C	160 hrs.
CDP1854AC/3	7 ± 0.5V	+125°C	160 hrs.

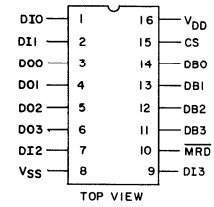
Fig. 13 — Bias/static burn-in circuit.

CDP1856/3, CDP1856C/3, CDP1857/3, CDP1857C/3

High-Reliability 4-Bit Bus Buffers/Separators

Features:

- *Provides easy connection of memory and I/O devices to CDP1800-series microprocessor data bus.*
- *Non-inverting fully buffered data transfer*



92CS-28097

TERMINAL ASSIGNMENT

The RCA-CDP1856/3, CDP1856C/3, CDP1857/3, and CDP1857C/3 are 4-bit CMOS non-inverting bus separators designed for use in CDP1800-series microprocessor systems. They can be controlled directly by a 1800-series microprocessor without the use of additional components.

The CDP1856/3 is designed for use as a bus or separator between the 1800-series microprocessor data bus and memories. The CDP1857/3 is designed for use as a bus buffer or separator between the 1800-series microprocessor data bus and I/O devices. Both types provide a chip-select (CS) input signal which, when high (1), enables the bus-separator three-state output drivers. The direction of data flow, when enabled is controlled by the MRD input signal.

In the CDP1856 when the MRD signal = 0 (low), it enables the three-state bus drivers (DB0 - BD3) and outputs data from the DATA-IN terminals to the data bus. When MRD = 1 (high), it disables the three-state bus drivers and enables the three-state data output drivers (DO0-DO3), thus transferrring data from the data bus to the DATA-OUT terminals.

In the CDP1857/3, when MRD = 1, it enables the three state bus drivers (DB0-DB3) and transfers data from the DATA-IN lines onto the data bus. When MRD = 0, it disables the three-state bus drivers (DB0-BD3) and enables the three-state data output drivers (DO0-D03), thus transferring data from the data bus to the DATA-OUT terminals.

The CDP1856/3 or CDP1857/3 can be used as a bi-directional bus buffer by connecting the corresponding DI and DO terminals (Fig. 2). The MRD output signal from the 1800 series microprocessor has the correct polarity to control the CDP1856/3 when this device is used as a memory data bus buffer/separator, or the CDP1857/3 when it is used as I/O bus buffer/separator. Therefore, the 1800 series microprocessor MRD signal can be connected directly to the MRD input of either device. See Function Tables I and II for use of the CDP1856/3 as a memory data bus buffer/separator and CDP1857/3 as an I/O bus buffer-/separator.

The CDP1856/3 and CDP1857/3 are functionally identical to the CDP1856C/3 and CDP1857C/3 respectively. The CDP1856/3 and CDP1857/3 have a recommended operating-voltage range of 4 to 10.5 volts, and the CDP1856C/3 and CDP1857C/3 have a recommended operating-voltage range of 4 to 6.5 volts. The CDP1856/3, CDP1856C/3, CDP1857/3 and CDP1857C/3 are supplied in 16-lead hermetic, dual-in-line side-brazed ceramic packages (D suffix) that conform to the requirements and dimensions specified in MIL-38510 Case Outline D-2. Other package styles may be available on a special order basis.

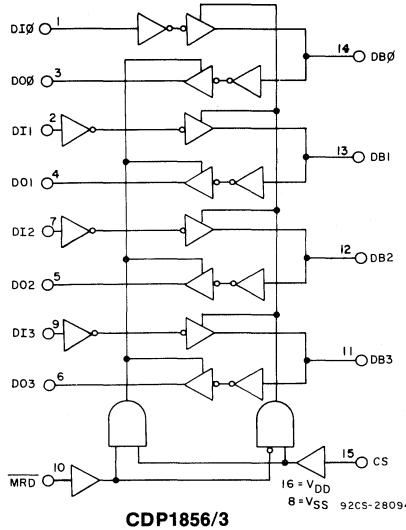
CDP1857/3 FUNCTION TABLE I
For I/O Bus Separator Operation

CS	$\overline{MRD}$	DATA BUS OUT DB0-DB3	DATA OUT DO0-DO3
0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	HIGH IMPEDANCE	DATA BUS
1	1	DATA IN	HIGH IMPEDANCE

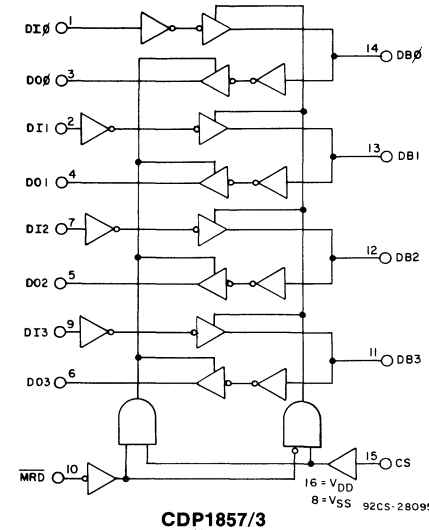
CDP1856/3 FUNCTION TABLE II
For Memory Data Bus Separator Operation

CS	$\overline{MRD}$	DATA BUS OUT DB0-DB3	DATA OUT DO0-DO3
0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	DATA IN	HIGH IMPEDANCE
1	1	HIGH IMPEDANCE	DATA BUS

CDP1856/3, CDP1856C/3, CDP1857/3, CDP1857C/3



CDP1856/3
CDP1856C/3



CDP1857/3
CDP1857C/3

Functional diagrams.

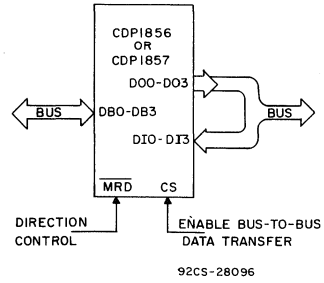
Electrical Characteristics

5-Volt data apply to the CDP1856, the CDP1856C, the CDP1857 and the CDP1857C.
10-Volt data apply to the CDP1856 and the CDP1857 only.

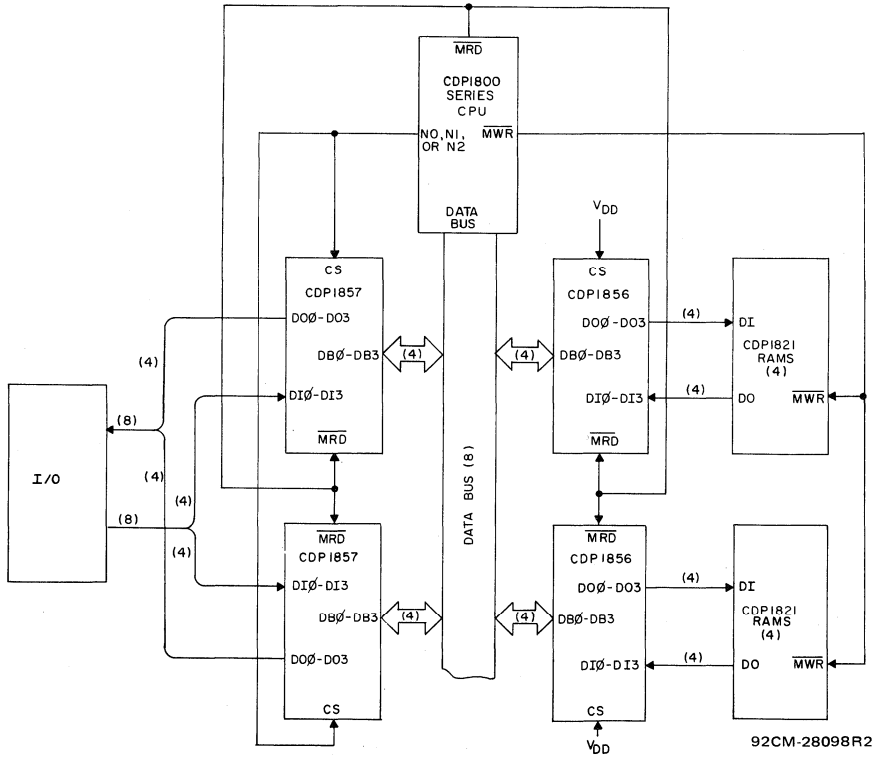
Characteristic	Test Conditions			Limits at Indicated Temperatures (°C)				Units
				CDP1856 CDP1856C		CDP1857 CDP1857C		
	V_{IN} (V)	V_O (V)	V_{DD} (V)	+25 -55		+125		
				Min.	Max.	Min.	Max.	
Static								
Quiescent Device Current, I_L	—	—	5	—	100	—	1000	μA
	—	—	10	—	100	—	1000	
Output Low Drive (Sink) Current, I_{OL}	—	0.4	5	2.0	—	1	—	mA
	—	0.5	10	2.6	—	2.2	—	
Output High Drive (Source) Current, I_{OH}	—	4.6	5	-1.4	—	-1	—	
	—	9.5	10	-2.6	—	-2.2	—	
Input Leakage Current, I_{IN}	0, 5	—	5	—	±1	—	±5	μA
	0, 10	—	10	—	±1	—	±5	
3-State Output Leakage Current, I_{OUT}	—	—	5	—	±1	—	±15	
	—	—	10	—	±1	—	±15	

CDP1856/3, CDP1856C/3, CDP1857/3, CDP1857C/3

TYPICAL APPLICATIONS

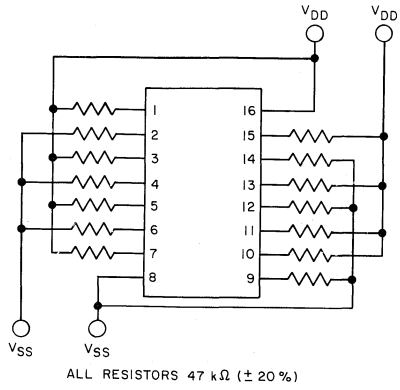


CDP1856 and CDP1857 bidirectional bus buffer operation.



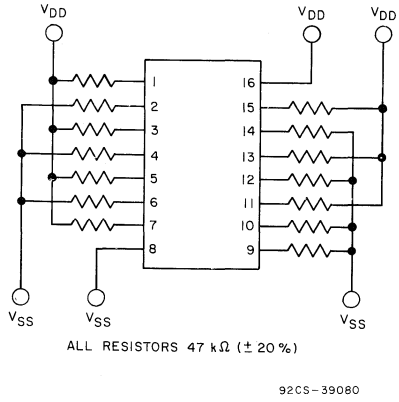
CDP1856 and CDP1857 bus separator operation.

CDP1856/3, CDP1856C/3, CDP1857/3, CDP1857C/3



TYPE NO.	V_{DD}	TEMP. (MIN.)	TIME (MIN.)
CDP1856/3	11 V ± 0.5 V	125° C	160 Hrs.
CDP1856C/3	7 V ± 0.5 V	125° C	160 Hrs.

Static-burn-in circuit for CDP1856/3 and CDP1856C/3.



TYPE NO.	V_{DD}	TEMP. (MIN.)	TIME (MIN.)
CDP1857/3	11 V ± 0.5 V	125° C	160 Hrs.
CDP1857C/3	7 V ± 0.5 V	125° C	160 Hrs.

Static-burn-in circuit for CDP1857/3 and CDP1857C/3.

CDP1858/3, CDP1858C/3

High-Reliability 4-Bit Latch and Decoder Memory Interface

Features:

- *Provides easy connection of memory devices to CDP1802 microprocessor*
- *Non-inverting fully buffered data transfer*

The RCA-CDP1858/3 and CDP1858C/3 are CMOS 4-bit latch decode circuits designed for use in CDP1800 series microprocessor systems. These devices have been specifically designed for use as memory-system decoders and interface directly with the 1800-series microprocessor multiplexed address bus at maximum clock frequency.

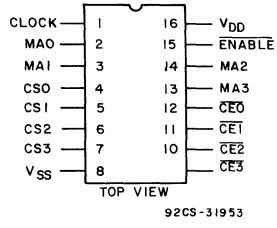
The CDP1858/3 is functionally identifed to the CDP1858C/3. The CDP1858/3 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1858C/3 has a recommended operating-voltage range of 4 to 6.5 volts.

The CDP1858/3 interfaces the 1800-series microprocessor address bus and up to 32 CDP1822 256 x 4 RAM's to provide a 4K byte RAM system. No additional components are required. The CDP1858/3 generates the chip selects required by the CDP1822 RAM. The chip select outputs are a function of the address bits connected to inputs MA0 through MA3.

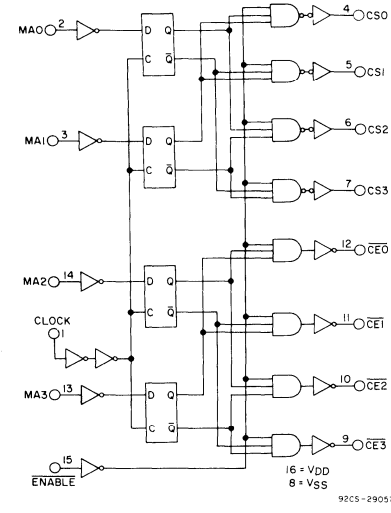
The MA0-MA3 address bits are latched at the trailing edge of TPA (generated by the CDP1802). When $\overline{\text{ENABLE}}$ = 1 (V_{DD}), the $\overline{\text{CS}}$ outputs = 0 (V_{SS}), and the CE outputs = 1. When $\overline{\text{ENABLE}}$ = 0, the outputs are enabled and correspond to the binary decode of the inputs. The $\overline{\text{ENABLE}}$ input can be used for memory system expansion.

The CDP1858/3 is also compatible with non-multiplexed address bus microprocessors. By connecting the CLOCK input to 1 (V_{DD}), the latches are in the data following mode and the decoded outputs can be used in general-purpose memory-system applications.

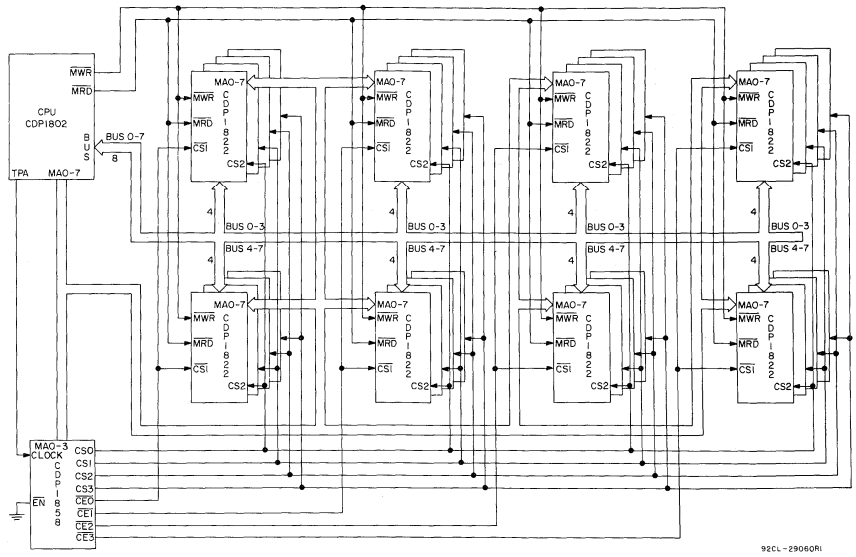
The CDP1858/3 and CDP1858C/3 are supplied in 16-lead, dual-in-line side-brazed ceramic packages (D suffix) that conform to the requirements and dimensions specified in MIL-38510 Case Outline D-2. Other package styles may be available on a special order basis.



TERMINAL ASSIGNMENT



Functional diagram.



4K byte RAM system using the CDP1858 and CDP1822.

STATIC ELECTRICAL CHARACTERISTICS
5-V Data Apply to the CDP1858 and the CDP1858C.
10-V Data Apply to the CDP1858 only.

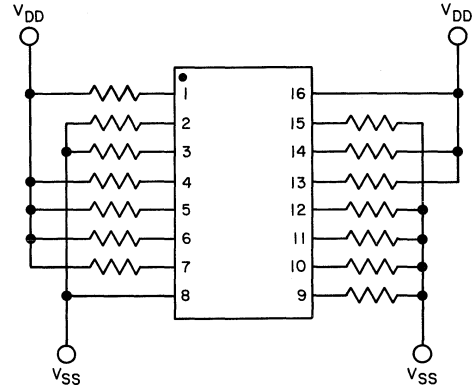
CHARACTERISTIC		TEST CONDITIONS			LIMITS CDP1858 CDP1858C				UNITS
					+25/-55° C		+125° C		
		V_{DD} (V)	V_I (V)	V_O (V)	Min.	Max.	Min.	Max.	
Quiescent Device Current,	I_L	5	0, 5	—	—	100	—	1000	μA
		10	0, 10	—	—	100	—	1000	
Output Low Drive (Sink) Current	I_{OL}	5	0, 5	0.4	1.6	—	1	—	mA
		10	0, 10	0.5	3.6	—	2.2	—	
Output High Drive (Source) Current,	I_{OH}	5	0, 5	4.6	-1.6	—	-1	—	
		10	0, 10	9.5	-3.6	—	-2.2	—	
Input Leakage Current,	I_{IN}	5	0, 5	—	—	±1	—	±5	μA
		10	0, 10	—	—	±1	—	±5	

CDP1858/3, CDP1858C/3

DECODE TRUTH TABLE

$\overline{\text{ENABLE}}$	DATA INPUTS		CS0	CS1	CS2	CS3	$\overline{\text{CE0}}$	$\overline{\text{CE1}}$	$\overline{\text{CE2}}$	$\overline{\text{CE3}}$
	MA1	MA0								
0	0	0	1	0	0	0	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	0	0				
0	1	0	0	0	1	0				
0	1	1	0	0	0	1				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	0	0	0	0	1	1	1	1

X = MA3, MA2, MA1, MA0 DON'T CARE



ALL RESISTORS 47 kΩ (± 20 %)

92CS-39671

TYPE NO.	V_{DD}	TEMP.	TIME
CDP1858/3	11 V ± 0.5 V	+ 125°C	160 Hrs. MIN.
CDP1858C/3	7 V ± 0.5 V	+ 125°C	160 Hrs. MIN.

Static burn-in circuit.

CDP1859/3, CDP1859C/3

High-Reliability 4-Bit Latch and Decoder Memory Interface

Features:

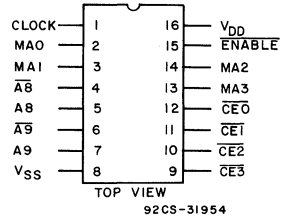
- *Provides easy connection of memory devices to CDP1802 microprocessor*
- *Non-inverting fully buffered data transfer*

The RCA-CDP1859/3 and CDP1859C/3 are CMOS 4-bit latch decode circuits designed for use in CDP1800 series microprocessor systems. These devices have been specifically designed for use as memory-system decoders and interface directly with the 1800-series microprocessor multiplexed address bus at maximum clock frequency.

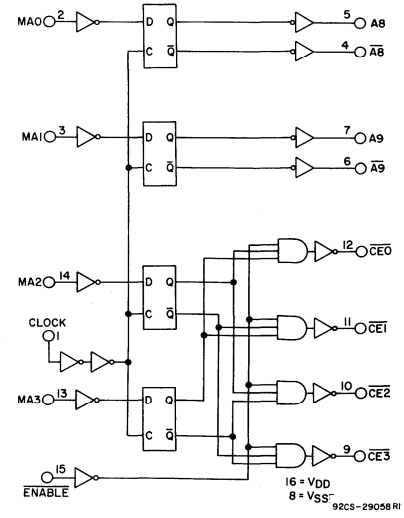
The CDP1859/3 is functionally identical to the CDP1859C/3. The CDP1859/3 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1859C/3 has a recommended operating-voltage range of 4 to 6.5 volts.

The CDP1859/3 interfaces the 1800-series microprocessor address bus and up to 32 CDP1821 1024 x 1 RAMs to provide a 4K byte RAM system. The CDP1859/3 generates the chip selects required by the CDP1821 RAM. The chip select outputs are a function of the address bits connected to inputs MA2 and MA3. The address bits connected to inputs MA0 and MA1 are latched by the trailing edge of TPA (generated by the 1800-series microprocessor) to provide the two additional address lines required by the CDP1821 when used in a CDP1800 series microprocessor-based system. When $\overline{ENABLE}$ = 1, the CE outputs are 1's; when $\overline{ENABLE}$ = 0, the CE outputs are enabled and correspond to the binary decode of the MA2 and MA3 inputs. $\overline{ENABLE}$ does not affect the latching or state of outputs A8, $\overline{A8}$, A9 or $\overline{A9}$.

The CDP1859/3 and CDP1859C/3 are supplied in 16-lead, dual-in-line side-brazed ceramic packages (D suffix) that conform to the requirements and dimensions specified in MIL-38510 Case Outline D-2. Other package styles may be available on a special order basis.

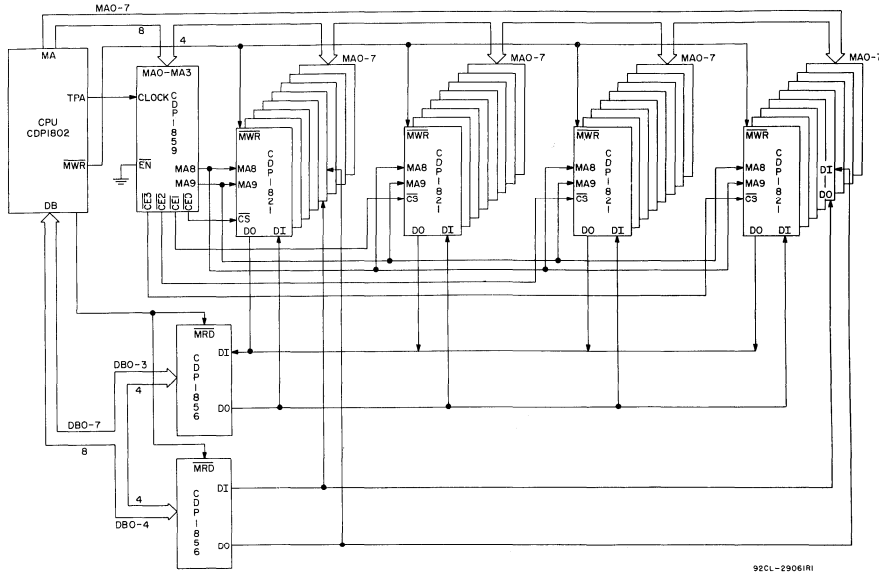


TERMINAL ASSIGNMENT



Functional diagram.

CDP1859/3, CDP1859C/3



4K byte RAM system using the CDP1859, CDP1856, and CDP1821.

STATIC ELECTRICAL CHARACTERISTICS
5-V Data Apply to the CDP1859 and the CDP1859C.
10-V Data Apply to the CDP1859 only.

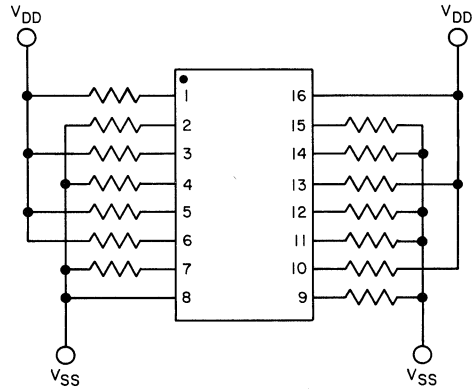
CHARACTERISTIC		TEST CONDITIONS			LIMITS CDP1859 CDP1859C				UNITS
					+25/-55° C		+125° C		
		V_{DD} (V)	V_I (V)	V_O (V)	Min.	Max.	Min.	Max.	
Quiescent Device Current,	I_L	5	0, 5	—	—	500	—	1000	μA
		10	0, 10	—	—	500	—	1000	
Output Low Drive (Sink) Current	I_{OL}	5	0, 5	0.4	1.6	—	1	—	mA
		10	0, 10	0.5	3.6	—	2.2	—	
Output High Drive (Source) Current,	I_{OH}	5	0, 5	4.6	-1.6	—	-1	—	
		10	0, 10	9.5	-3.6	—	-2.2	—	
Input Leakage Current,	I_{IN}	5	0, 5	—	—	±1	—	±5	μA
		10	0, 10	—	—	±1	—	±5	

CDP1859/3, CDP1859C/3

DECODE TRUTH TABLE

$\overline{\text{ENABLE}}$	DATA INPUTS		A8	A9	$\overline{\text{A8}}$	$\overline{\text{A9}}$	$\overline{\text{CE0}}$	$\overline{\text{CE1}}$	$\overline{\text{CE2}}$	$\overline{\text{CE3}}$
	MA0	MA1								
0	0	0	0	0	1	1	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	1	0				
0	1	0	1	0	0	1				
0	1	1	1	1	0	0				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	NOT AFFECTED BY $\overline{\text{ENABLE}}$				1	1	1	1

X = MA3, MA2, MA1, MA0 DON'T CARE



ALL RESISTORS 47 kΩ (± 20 %)

92CS-39696

TYPE NO.	V_{DD}	TEMP.	TIME
CDP1859/3	11 V ± 0.5 V	+125° C	160 HRS MIN
CDP1859C/3	7 V ± 0.5 V	+125° C	160 HRS MIN

Static burn-in circuit.

Radiation-Hardened CMOS/SOS LSI Devices for Aerospace

Radiation-Hardened CMOS/SOS LSI Devices for Aerospace

The unique features of SOS (Silicon on Sapphire) combined with silicon gate technology and CMOS architecture result in LSI/VLSI circuits characterized by low power consumption, high internal circuit speeds, and overall superior radiation resistance. SOS devices are immune to latch-up and can be designed with very high packing densities. Other technologies may have some of these features but in balancing all the desirable features for Space Technology, SOS comes out ahead in all categories.

RCA offers a complete family of CMOS Silicon-on-Sapphire devices that are specifically designed and hardened for use in aerospace systems that require high tolerance to total-dose, transient, and cosmic radiation single-event-upset. These devices are screened to RCA/1R specifications as indicated in the screening table.

The family consists of RAMS, ROMS, and selected members of the EPIC 8-bit-slice family. Special I/O and support circuits are provided with both gate-array and standard-cell semicustom circuits.

Many of the devices listed are in constant development and improvement. Contact RCA Sales or Marketing for the most recent performance data.

Index to Radiation-Hardened Devices for Aerospace

Available to /1R Screening (RCA's Modified Class S for LSI Devices)†

Type No.	Description
CMM5104	4096-Word x 1-Bit Static RAM
CMM5114	1024-Word x 4-Bit Static RAM
CMM6167	16K-Word x 1-Bit Static RAM
EPIC Chip Set	
GP001	8-Bit General Processor Unit (GPU)
GP501	Emulating Controller
GP502	Microprogram Sequencer '2910'
GP503	8-Bit x 8-Bit Multiplier
GP511	Voltage-Level Converter and Buffer
GP301	512-Word x 8-Bit ROM
GP302	256-Word x 16-Bit ROM
Planned Additions to the EPIC Chip Set	
GP514	Double Address Select Unit
GP515	Double Register Select Unit
GP516	Bus Interface Unit
GP517	Interrupt Control and Timing Unit

†Selected EPIC Devices are Available to RCA /3 Screening. (Objective data is provided.)

Radiation Tolerance for the Hardened CMOS/SOS Family

Total Dose	$> 10^5$ rads (Si)
Latch-Up	Not Possible
Transient Survival	$\geq 10^{12}$ rads (Si)/Second
Single-Event-Upset (SEU)	Less than 10^{-8} errors/bit-day

Screening

/1R Screening Flow

Screen	Method	Reqmt.	Notes
Wafer Lot Acceptance Including SEM	5007	100%	
Radiation Verification (If Required)	1019	Sample	
Nondestructive Bond Pull	1019	100%	
Internal Visual	Military Cond A. (Modified)	100%	1
Pre-Seal Bake	—	100%	
Stabilization Bake	1008 Cond. C 24 Hours	100%	
Temperature Cycling	1010 Cond. C	100%	
Constant Acceleration	2001 Cond. E Y1 Dir.	100%	
Particle Impact Noise Detection (PIND)	2020 Cond. A	100%	
Serialization	—	100%	
Radiographic 1-View	2012	100%	
Initial (Pre Burn-In) Electrical Parameters at 25°C.	Per Applicable Device Spec.	100%	
Burn-In Test 160 Hours @ 125°C Dynamic	1015	100%	2
Interim Electrical Test 1 Percent Defective Allowable (10%)	—	100% All Tests	
24-Hour Static Burn-In @ 125°C. (With Delta Requirements)	—	100%	2
Interim Electrical Test 2		100%	
24-Hour Static Burn-In @ 125°C. (With Delta Requirements)		100%	2
Interim Electrical Test 3		100%	
Percent Defective Allowable (5%) Functional (3%)		All Tests	3
240-Hour Dynamic Burn-In (With Delta Requirements)	1015	100%	2
Interim (Post Burn-In) Electrical Parameters @ 25°C.	Per Applicable Device Spec.	100%	
Percent Defective Allowable (5%) Functional (3%)		All Tests	
Final Electrical Test @ -55/+125°C	—	100%	
Seal	1014		
A) Fine	Cond. A or B	100%	
B) Gross	Cond. C	100%	
Group A Quality Conformance Testing	5005	100%	
External Visual	2009	100%	

Notes:

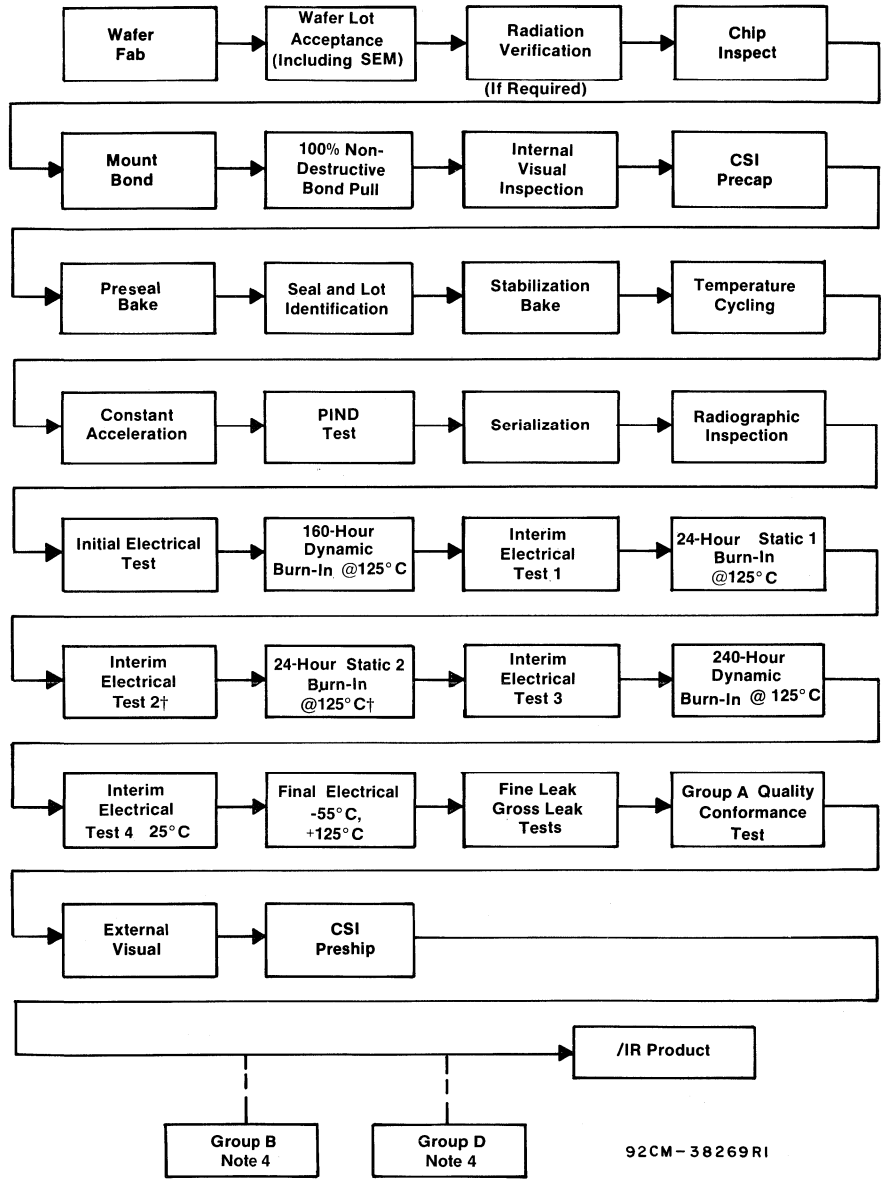
1. Visual Inspection for Hi-Rel 1R Product.
   Military Condition 'A' which is now specified for Class S Microcircuits, is difficult to apply to LSI devices. Therefore, RCA performs Visual Inspection on Class S LSI devices to Military Condition 'A' for Bond Inspection (3.1.4), internal leads (3.1.5) and package condition (3.1.6). All other Visual Inspection is to Military Condition 'B' except as follows:
   A. High magnification inspection is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required and at 30X to 60X for low magnification.
   B. Criteria 3.2.1.1 and 3.2.1.2, metallization scratches and voids, are not applied to metallization over the step surrounding the contact cut and in the contact itself.
   C. Criteria 3.1.6.1C has the following notes added: Glassivated areas of the die are excluded from the criteria of 3.1.6.1C when the particle or material is attached only at the top surface of the passivation.
   D. 3.2.1.7 is applied to areas of sufficient complexity on each chip to assure general alignment and contact coverage. These areas are inspected at 200X to 300X and consist only of the area exposed to the immediate field of view.
   E. 3.2.2 Diffusion and passivation faults are inspected only in two opposing corners of the chip except on SOS product (see H).
   F. During CSI screening, if individual devices are observed to have defects that clearly violate 3.2.1.1 or 3.2.1.2 at the contact cut or 3.2.2 they are rejected and removed from the lot, but are not counted against any lot acceptance criteria.
   G. 3.2.3C. Cracks greater than 5 mils are rejected only if they point to or cross the grid line (SOS Technology).
   H. SOS devices are inspected for complete islands, bridging between islands, and missing adjacent contacts from a row in a contact chain. The 1-mil wire clearance criteria is deleted.

(Notes continued on next page)

Screening

Notes (continued):

2. Refer to the technical data on individual types for burn-in circuit information.
3. RAMs receive one 24-hour static burn-in with 1's stored, and a second 24-hour static burn-in with 0's stored. Logic devices receive a single 48-hour burn-in with interim electrical test 2 omitted.
4. Groups B and D conformance tests are optional and are only performed if they are indicated by a separate line item on the customer P.O. and accepted by RCA.



†See Note 2.

Reliability

CMOS/SOS Life-Test Summary for /1R Product

At 125°C, $V_{DD} \geq 7$ Volts (Screened Units for Aerospace Applications)

Type	Production Period	Quantity	Device Hours	Out of Specification	
				Leakage	Functional
1821 1K x 1 RAM	1978	397	752,000	1	0
RAMs, Controller, Arrays	82-83	385	385,000	0	0
1821 1K x 1 RAM	1982	629	706,000	0	0
1821 Radiation-Hardened 1K x 1 RAM	1982	138	179,000	0	0
GP001 Radiation-Hardened General Processor	1983	35	105,000	0	0
GP502 Radiation-Hardened Sequencer	1983	45	45,000	1	0
632 Gate Radiation-Hardened Universal Array	1983	25	31,000	0	0
1K x 4 Radiation-Hardened	1983	122	95,000	0	0
4K x 1 Radiation-Hardened	1983	269	262,000	0	0
1821 1K x 1 RAM	1984	45	95,000	0	0
1K x 4 RAM	1984	77	77,000	0	0
Total SOS		2,167	2,682,000	2	0
Failure Rate % Per 1000, 125° C., 7-Volt Rate Extrapolated to 55° C, 5 Volt (1.0 eV), Failures Per 10^9 Hours (FITS)				0.114 1.9	0.034 0.5

/1R Product Information:

Die Attach ..... Epoxy
Manufacturing Location ..... USA

Data Supplied With Order of /1R Packaged Devices:

A) Certificate of Conformance Including Burn-In and Group A Attributes Data
B) Pre and Post Variable Data and Delta Calculations for Static I and Static II Burn-In and Dynamic II Burn-In
C) Copy of X-Ray and SEM Reports
D) Radiation Report
E) Groups B and D Attributes Data (If Ordered)

Rad-Hard CMOS/SOS RAMs

The following memories use CMOS/SOS technology and are designed for use in memory systems where low power and simplicity in use are desired. The CMM5114 and CMM5104 have TTL compatibility on all I/O terminals to permit easy system integration.

Type No.	Description
CMM5114	1024-Word x 4-Bit Static RAM
CMM5104	4096-Word x 1-Bit Static RAM
*CMM6167	16,384-Word x 1-Bit Static RAM

*Preliminary data

The devices are ideal for aerospace applications. They provide latch-up-free operation under transient radiation, greater than 10^5 rads (Si) total dose, transient survival $\geq 10^{12}$ rads (Si)/second and single-event-upset (SEU) capability of less than 10^{-8} errors/bit-day.

The CMM5114 and CMM5104 are available in either an 18-lead dual-in-line side-brazed ceramic package, 24-lead ceramic flat pack, or 24-contact leadless chip carrier. The CMM6167 is available in the 24-lead ceramic flat pack.

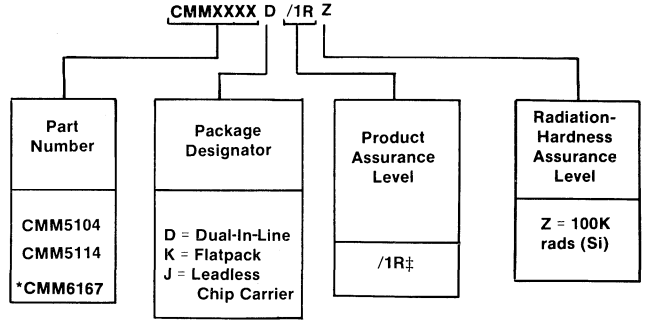
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR DIC PACKAGES:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A =-55° to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	6.5	V

Guide to the Part Number, Package Designator, and Product Assurance Level of High-Reliability CMM5104/CMM5114/CMM6167 Series.



*The CMM6167 is currently available in the 24-lead flat pack (K suffix). Other packages will be introduced as required.
‡Selected devices are available to RCA /3 screening.

CMM5104/1RZ

High-Reliability, Radiation-Hardened CMOS 4096-Word by 1-Bit Static RAM Aerospace Class S Screening

Radiation Features

- *Radiation hardened to 100K rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec, 20-ns pulse*

Features

- *Fast access time (t_{AVQV}): 200 ns at T_A=25° C*
- *Single power supply: 4.5 V to 6.5 V*
- *Low standby and operating power*
- *All inputs and outputs TTL compatible*
- *Fully static operation*
- *3-state output*
- *Industry-standard 18-pin DIL*
- *Also available in 24-lead flat pack*

The RCA CMM5104/1RZ is a 4096-bit static random-access memory organized as 4096 words x 1 bit using CMOS/SOS technology. It is designed for use in memory systems where low power and simplicity in use are desirable.

This technology permits operation in high-radiation environments. It is insensitive to neutrons, cannot latch up at any dose rate and is resistant to single-event upset caused by cosmic rays or heavy ions.

TTL compatibility on all I/O terminals permits easy system integration. The data-out signal has the same polarity as the input data. A separate data input and a separate tri-state output are used.

The CMM5104/1RZ is available in an industry-standard pinout configuration, 18-lead ceramic dual-in-line side-brazed package (D suffix), that conforms to the requirements and dimensions specified in MIL-38510 Case Outline D-6. The part is also available in a 24-lead ceramic flat pack (K suffix).

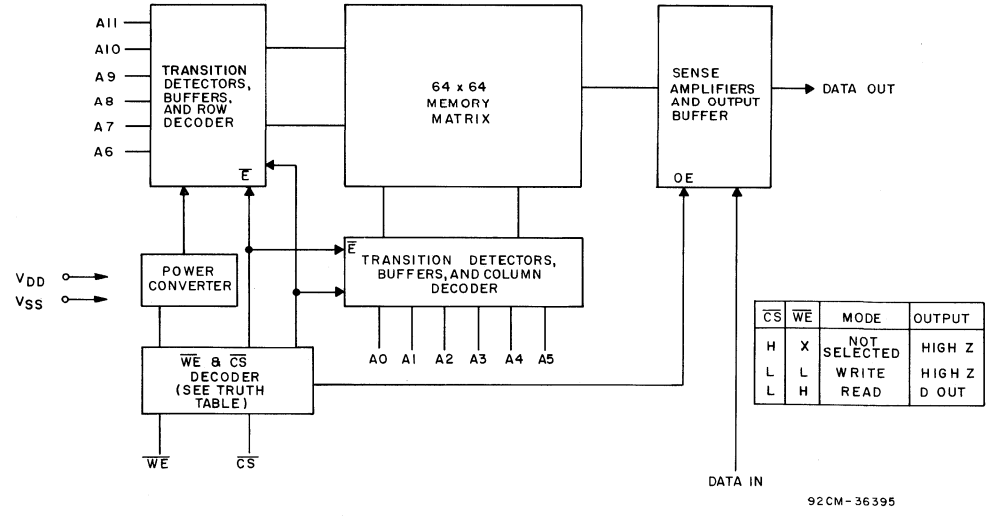


Fig. 1 - Functional block diagram.

CMM5104/1RZ

STATIC ELECTRICAL CHARACTERISTICS, V_{DD}=5 V ± 5%, V_{IN}= 0 V or V_{DD}, Except as Noted

CHARACTERISTIC		CONDITION	LIMITS						UNITS
		V_O	-55° C, +25° C		+125° C		POST RADIATION +25° C‡		
		(V)	Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent Device Current	I_{DD}	—	—	0.1•	—	1•	—	1•	mA
Output Low Drive (Sink) Current	I_{DN}	0.4	4•	—	2.5•	—	2.5•	—	
Output High Drive (Source) Current	I_{DP}	V_{DD}-0.4	3•	—	2•	—	2•	—	
Output Voltage Low Level	V_{OL}	—	—	0.1	—	0.1	—	0.1	V
Output Voltage High Level	V_{OH}	—	V_{DD}-0.1	—	V_{DD}-0.1	—	V_{DD}-0.1	—	
Input Low Voltage	V_{IL}	—	—	0.8•	—	0.8•	—	0.8•	
Input High Voltage	V_{IH}	—	$V_{DD}/2$•	—	$V_{DD}/2$•	—	$V_{DD}/2$•	—	
Input Leakage Current	I_{IN}	—	—	±2•	—	±10•	—	±10•	μA
3-State Output Leakage Current	I_{OZ}	—	—	±5•	—	±30•	—	±30•	
Operating Device Current *	I_{OPR}	—	—	3.5	—	4	—	4	mA
Operating Device Current (Deselected)*	I_{OPRD}	—	—	0.1	—	1	—	1	
Input Capacitance §	C_{IN}	—	—	5	—	5	—	5	pF
Output Capacitance§	C_{OUT}	—	—	7	—	7	—	7	

•Limit with black (•) designate actual measurement, all other limits are designer's parameters under given test conditions.

‡ Radiation measurements are made on 2 samples/wafer. The limits shown are for within 1 hour of radiating to 100 K rads (Si).

* Operating current measured using 1-MHz cycle and C_L = 50 pF.

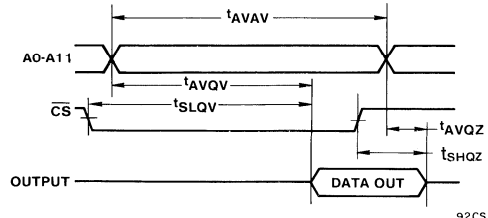
§ Capacitance measurements are made with no bias applied.

DYNAMIC ELECTRICAL CHARACTERISTICS, V_{DD}=5 V ± 5%, C_L=50 pF

CHARACTERISTIC		LIMITS						UNITS
		-55° C, +25° C		+125° C		POST RADIATION +25° C‡		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read-Cycle Times (Fig. 2)								
Read Cycle	t_{AVAV}	200	—	250	—	250	—	ns
Access From Address	t_{AVQV}	—	200•	—	250•	—	250•	
Access From $\overline{CS}$	t_{SLQV}	—	220•	—	280•	—	280•	
Output Hold from Address	t_{AVQZ}	—	80	—	100	—	100	
Output Hold from $\overline{CS}$	t_{SHQZ}	—	80	—	100	—	100	

•Limit with black (•) designate actual measurement, all other limits are designer's parameters under given test conditions.

‡Radiation measurements are made on 2 samples/wafer. The limits shown are for within 1 hour of radiating to 100 K rads (Si).



TIMING MEASUREMENT IS REFERENCED TO $V_{DD}/2$.

Fig. 2 - Read-cycle timing waveforms.

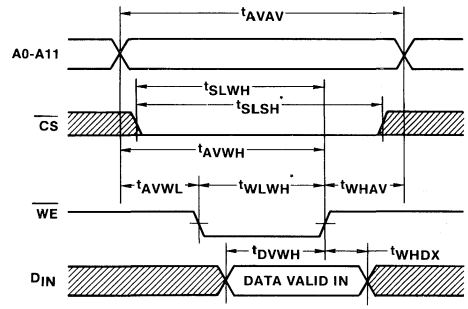
DYNAMIC ELECTRICAL CHARACTERISTICS, V_{DD}=5 V ± 5%, C_L=50 pF

CHARACTERISTIC		LIMITS						UNITS
		-55° C, +25° C		+125° C		POST RADIATION +25° C‡		
		Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Times (Fig. 3)								
Write Cycle	t_{AVAV}	200•	—	250•	—	250•	—	ns
Write Pulse Width*	t_{WLWH}	125•	—	145•	—	145•	—	
Address Set-up to Beginning of Write	t_{AVWL}	0•	—	0•	—	0•	—	
Address Set-up to End of Write	t_{AVWH}	160•	—	205•	—	205•	—	
Address Hold Time	t_{WHAV}	40•	—	45•	—	45•	—	
$\overline{CS}$ to Write Set-up Time	t_{SLWH}	160•	—	205•	—	205•	—	
$\overline{CS}$ Pulse Width*	t_{SLSH}	180•	—	220•	—	220•	—	
Data to Write Set-up Time	t_{DVWH}	100•	—	120•	—	120•	—	
Data Hold from Write	t_{WHDX}	5•	—	10•	—	10•	—	

•Limit with black (•) designate actual measurement, all other limits are designer's parameters under given test conditions.

‡Radiation measurements are made on 2 samples/wafer. The limits shown are for within 1 hour of radiating to 100 K rads (Si).

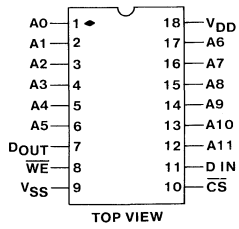
*$\overline{CS}$ and $\overline{WE}$ must overlap for at least t_{WLWH} min. value. t_{DVWH} min. must occur during this overlap.



TIMING MEASUREMENT IS REFERENCED TO $V_{DD}/2$. 92CS-37690

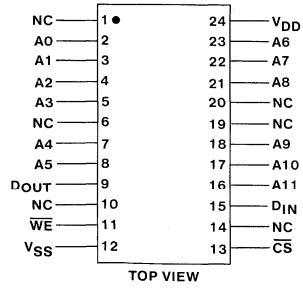
*$\overline{CS}$ AND $\overline{WE}$ MUST OVERLAP FOR AT LEAST t_{WLWH} MIN. VALUE. t_{DVWH} MIN. MUST OCCUR DURING THIS OVERLAP.

Fig. 3 - Write-cycle timing waveforms.



TERMINAL ASSIGNMENT FOR D PACKAGE (18-LEAD, CERAMIC DUAL-IN-LINE SIDE-BRAZED)

92CS-37683



TERMINAL ASSIGNMENT FOR K PACKAGE (24-LEAD, CERAMIC FLATPACK)

92CS-37687

CMM5104/1RZ

DATA RETENTION CHARACTERISTICS; See Fig. 4

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		-55°C, +25°C		+125°C		POST RADIATION +25°C[a]		
	V_{DD} (V)	Min.	Max.	Min.	Max.	Min.	Max.	
Minimum Data Retention Voltage V_{DR}	—	—	2•	—	2.5•	—	2.5•	V
Data Retention Quiescent Current $I_{DD}DR$	—	—	40•	—	400•	—	400•	μA
V_{DD} to V_{DR} Rise and Fall Time t_r, t_f	5	1	—	1	—	1	—	μs

•Limit with black (•) designate actual measurement, all other limits are designer's parameters under given test conditions.

[a]Radiation measurements are made on 2 samples/wafer. The limits shown are for within 1 hour of radiating to 100 K rads (Si).

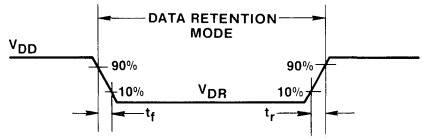


Fig. 4 - Low V_{DD} data retention timing waveforms.

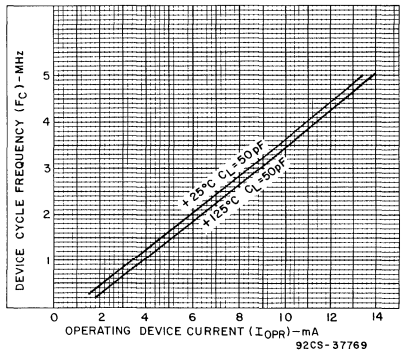


Fig. 5 - Typical operating device-current (selected) as a function of cycle frequency.

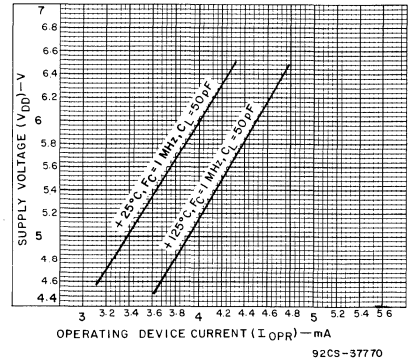


Fig. 6 - Typical operating device-current (selected) as a function of supply voltage.

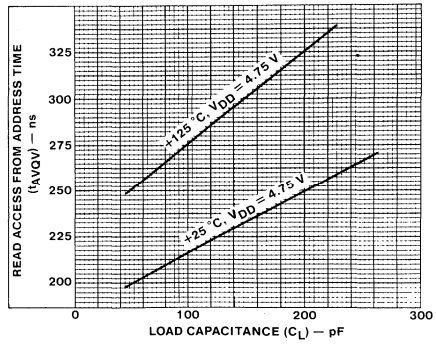


Fig. 7 - Read access from address time (t_{AVQV}) as a function of load capacitance. (Time measurements made at 50% V_{DD} point.]

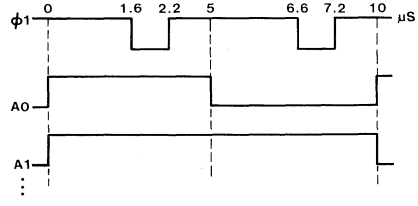
Burn-In and Life-Test Circuits and Timing Waveforms

Test	Temperature	Minimum Duration	V_{DD}
Dynamic I	125°C	160 hr	7 V
Static I	125°C	24 hr	7 V
Static II	125°C	24 hr	7 V
Dynamic II	125°C	240 hr	7 V
Life Test	125°C	1000 hr	5.5 V Min.

All Inputs are Connected Through a 1 to 6-KΩ Resistor to the Following:

Test	Dynamic I[a]			Static I[b]			Static II[c]			Dynamic II[a]			Life Test[a]		
Package	D	J	K	D	J	K	D	J	K	D	J	K	D	J	K
Pin No.															
1	A_0	—	—	V_{DD}	—	—	V_{SS}	—	—	A_0	—	—	A_0	—	—
2	A_1	A_0	A_0	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A_1	A_0	A_0	A_1	A_0	A_0
3	A_2	A_1	A_1	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A_2	A_1	A_1	A_2	A_1	A_1
4	A_3	A_2	A_2	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A_3	A_2	A_2	A_3	A_2	A_2
5	A_4	A_3	A_3	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A_4	A_3	A_3	A_4	A_3	A_3
6	A_5	—	—	V_{DD}	—	—	V_{SS}	—	—	A_5	—	—	A_5	—	—
7		A_4	A_4		V_{DD}	V_{DD}		V_{SS}	V_{SS}		A_4	A_4		A_4	A_4
8	ϕ_1	A_5	A_5	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	ϕ_1	A_5	A_5	ϕ_1	A_5	A_5
9	V_{SS}			V_{SS}			V_{SS}			V_{SS}			V_{SS}		
10	A_{13}	—	—	V_{DD}	—	—	V_{SS}	—	—	A_{13}	—	—	A_{13}	—	—
11	A_{12}	ϕ_1	ϕ_1	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A_{12}	ϕ_1	ϕ_1	A_{12}	ϕ_1	ϕ_1
12	A_{11}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A_{11}	V_{SS}	V_{SS}	A_{11}	V_{SS}	V_{SS}
13	A_{10}	A_{13}	A_{13}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A_{10}	A_{13}	A_{13}	A_{10}	A_{13}	A_{13}
14	A_9	—	—	V_{DD}	—	—	V_{SS}	—	—	A_9	—	—	A_9	—	—
15	A_8	A_{12}	A_{12}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A_8	A_{12}	A_{12}	A_8	A_{12}	A_{12}
16	A_7	A_{11}	A_{11}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A_7	A_{11}	A_{11}	A_7	A_{11}	A_{11}
17	A_6	A_{10}	A_{10}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A_6	A_{10}	A_{10}	A_6	A_{10}	A_{10}
18	V_{DD}	A_9	A_9	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{DD}	A_9	A_9	V_{DD}	A_9	A_9
19	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
20	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
21	—	A_8	A_8	—	V_{DD}	V_{DD}	—	V_{SS}	V_{SS}	—	A_8	A_8	—	A_8	A_8
22	—	A_7	A_7	—	V_{DD}	V_{DD}	—	V_{SS}	V_{SS}	—	A_7	A_7	—	A_7	A_7
23	—	A_6	A_6	—	V_{DD}	V_{DD}	—	V_{SS}	V_{SS}	—	A_6	A_6	—	A_6	A_6
24	—	V_{DD}	V_{DD}	—	V_{DD}	V_{DD}	—	V_{DD}	V_{DD}	—	V_{DD}	V_{DD}	—	V_{DD}	V_{DD}

[a]The following timing waveforms are used for the Dynamic and Life Tests.



A1 TO A13 ARE SUCCESSIVE DIVISIONS BY 2 BASED ON A0

92CS-37686

[b]Memory array is pre-initialized with all 1's.

[c]Memory array is pre-initialized with all 0's.

NOTE: Pin 7 on D-type package, and Pin 9 on J and K packages are the outputs connected to $V_{DD}/2$ in High Z state.
- indicates no connection.
ϕ_1 is connected to $\overline{WE}$ on all packages (D, J, and K).
A_{13} is connected to $\overline{CS}$ on all packages (D, J, and K).

Delta Limits and Calculations

Parameter	Absolute Limit	Delta Limit
I_{DD}	100 μA	±30 μA
I_{DN} and I_{DP}	—	±10% of 0 hr value
I_{OZ}	5 μA	±500 nA

Delta Calculation	Initial Reading	Final Reading
I	Interim Electrical Tests I	Interim Electrical Tests II
II	Interim Electrical Tests I	Interim Electrical Tests III
III	Interim Electrical Tests I	Interim Electrical Tests IV

CMM5114/1RZ

High-Reliability, Radiation-Hardened CMOS 1024-Word by 4-Bit Static RAM Aerospace Class S Screening

Radiation Features

- *Radiation hardened to 100K rads (S_i)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit day*
- *Latch-up free under transient radiation*
- *Resistance to upset under transient radiation rate of up to 1 x 10^{10} rads (S_i)/sec*

Other Features:

- *Single power supply: 4.5 V to 6.5 V*
- *Low standby and operating power*
- *All inputs and outputs TTL compatible*
- *Common data inputs and outputs*
- *Fully static operation*
- *3-state output*
- *Industry-standard 18-pin DIL weld seal*
- *Also available in 24-lead flat pack*

The RCA-CMM5114/1RZ is a 1024-word by 4-bit static random-access memory using CMOS/SOS technology. It is designed for use in memory systems where low power and simplicity in use are desirable. TTL compatibility on all I/O terminals permits easy system integration.

CMOS/SOS technology permits operation in high-radiation environments. It is insensitive to neutrons, cannot latch up at any dose rate and is resistant to single-event upset caused by cosmic rays or heavy ions.

The CMM5114/1RZ is available in an industry-standard pinout configuration, 18-lead ceramic dual-in-line side-brazed package weld seal (D suffix), that conforms to the requirements and dimensions specified in MIL-38510 Case Outline D-6. The part is also available in a 24-lead ceramic flat pack (K suffix)

OPERATIONAL MODES			
FUNCTION	$\overline{CS}$	$\overline{WE}$	**DATA PINS**
Read	0	1	Output: Dependent on data
Write	0	0	Input
Not Selected	1	X	High-Impedance

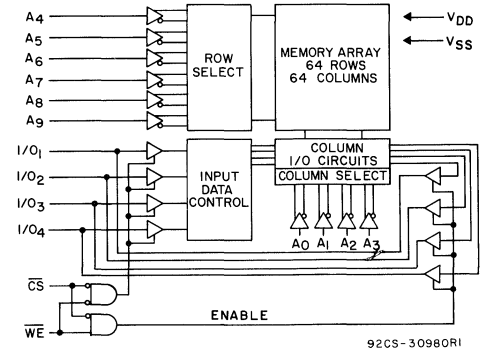


Fig. 1 - Functional block diagram for CMM5114/1RZ.

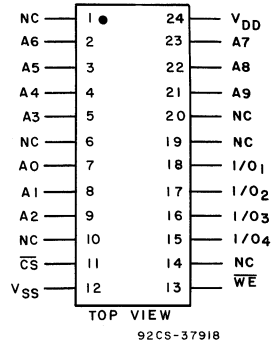
STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%

CHARACTERISTIC		CONDITIONS	LIMITS						UNITS
			-55°C, +25°C		+125°C		POST RADIATION ‡ +25°C		
			Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent Device Current	I_{DD}	V_{IN} = 0 V or V_{DD}, $V_{\overline{CS}} = V_{DD}$	—	0.1 •	—	1 •	—	1 •	mA
Operating Device Current	I_{DD1} *	Outputs open circuited: cycle time = 1 μs	—	5 •	—	6 •	—	6 •	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	2.6 •	—	1.7 •	—	1.7 •	—	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{DD}$ -0.4 V	1.8 •	—	1.1 •	—	1.1 •	—	mA
Output Voltage Low Level	V_{OL}	—	—	0.1	—	0.2	—	0.2	V
Output Voltage High Level	V_{OH}	—	V_{DD} -0.1 V	—	V_{DD} -0.2 V	—	V_{DD} -0.2 V	—	V
Input Low Voltage	V_{IL}	—	—	0.8 •	—	0.8 •	—	0.8 •	V
Input High Voltage	V_{IH}	—	$V_{DD}/2$•	—	$V_{DD}/2$•	—	$V_{DD}/2$•	—	V
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{DD}	—	±2 •	—	±10 •	—	±10 •	μA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0 V or V_{DD}	—	±5 •	—	±50 •	—	±50 •	μA
Input Capacitance	C_{IN}	—	—	5	—	5	—	5	pF
Output Capacitance	C_{OUT}	—	—	7	—	7	—	7	pF

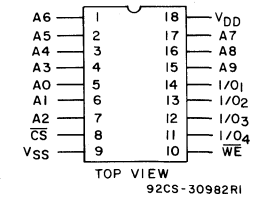
• Limit with black dot (•) designates actual measurement, all other limits are designer's parameters under given test conditions.

‡ Radiation measurements are made on 2 samples/wafer. The limits shown are for within 1 hour of radiating to 100 K rads (Si).

* Operating current measured using 1-MHz cycle and C_L = 50 pF.



TERMINAL ASSIGNMENT FOR K PACKAGE (24-LEAD, CERAMIC FLATPACK)



TERMINAL ASSIGNMENT FOR D PACKAGE (18-LEAD, CERAMIC DUAL-IN-LINE SIDE-BRAZED)

CMM5114/1RZ

DYNAMIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%, C_L = 50 pF

CHARACTERISTIC		LIMITS						UNITS
		-55° C, +25° C		+125° C		POST RADIATION ‡ +25° C		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read-Cycle Times (Fig. 2)								
Read Cycle	t_{AVAV}	200 •	—	250 •	—	250 •	—	ns
Access	t_{AVQV}	—	200 •	—	250 •	—	250 •	
Chip Selection to Output Valid	t_{SLQV}	—	160 •	—	200 •	—	200 •	
Chip Selection to Output Active	t_{SLQA}	20	—	20	—	20	—	
Output 3-State from Deselection	t_{SHQZ}	—	100	—	140	—	140	
Output Hold from Address Change	t_{AVQZ}	30	110	55	150	30	150	
Write-Cycle Times (Fig. 3)								
Write Cycle	t_{AVAV}	200 •	—	250 •	—	250 •	—	ns
Write Pulse Width	t_{WLWH}*	120 •	—	150 •	—	150 •	—	
Address Hold Time from Write Enable	t_{WHAV}	40 •	—	40 •	—	40 •	—	
Address to Write Set-up Time	t_{AVWL}	0 •	—	0 •	—	0 •	—	
Address Set-up to End of Write	t_{AVWH}	150 •	—	200 •	—	200 •	—	
Chip Select Pulse Width	t_{SLSH}*	150 •	—	200 •	—	200 •	—	
Chip Select to Write Set-up Time	t_{SLWH}	150 •	—	200 •	—	200 •	—	
Data to Write Set-up Time	t_{DVWH}	60 •	—	75 •	—	75 •	—	
Data Hold from Write	t_{WHDX}	5 •	—	5 •	—	5 •	—	

• Limit with black dot (•) designates actual measurement, all other limits are designer's parameters under given test conditions.

‡ Radiation measurements are made on 2 samples/wafer. The limits shown are for within 1 hour of radiating to 100 K rads (Si).

* $\overline{CS}$ and $\overline{WE}$ must overlap for at least t_{WLWH} min. t_{DVWH} min. must occur during this overlap.

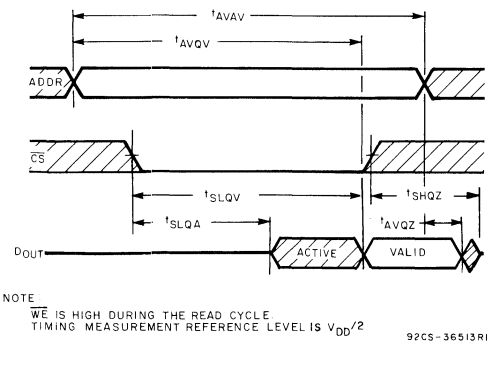


Fig. 2 - Read-cycle timing waveforms.

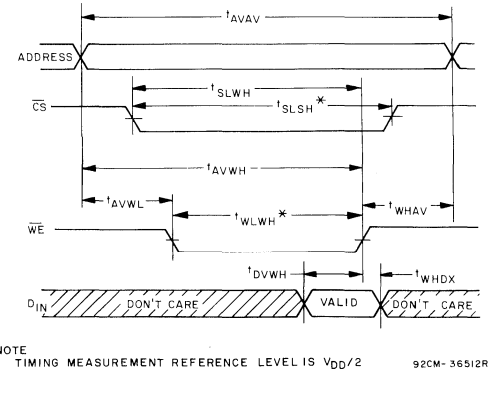


Fig. 3 - Write-cycle timing waveforms.

DATA RETENTION CHARACTERISTICS; See Fig. 4

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		-55° C +25° C		+125° C		POST RADIATION ‡ +25° C		
	V_{DD} (V)	Min.	Max.	Min.	Max.	Min.	Max.	
Minimum Data Retention Voltage V_{DR}	—	—	2 •	—	2.5 •	—	2.5 •	V
Data Retention Quiescent Current $I_{DD}DR$	—	—	50 •	—	500 •	—	500 •	μA
V_{DD} to V_{DR} Rise and Fall Time t_r, t_f	5	1	—	1	—	1	—	μs

• Limit with black dot (•) designate actual measurement, all other limits are designer's parameters under given test conditions.

‡ Radiation measurements are made on 2 samples/wafers. The limits shown are for within 1 hour of radiating to 100 K rads (Si).

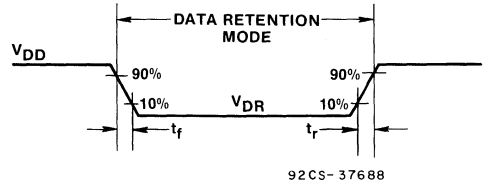


Fig. 4 - Low V_{DD} data retention timing waveforms.

CMM5114/1RZ

Table II — Burn-In and Life-Test Circuits and Timing Waveforms

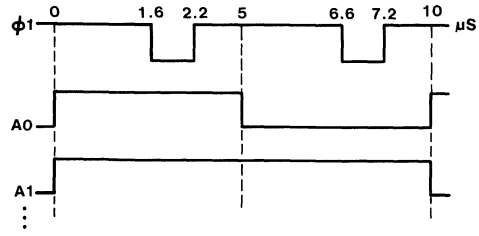
Test	Temperature	Minimum Duration	V_{DD}
Dynamic I	125°C	160 hr	7 V
Static I	125°C	24 hr	7 V
Static II	125°C	24 hr	7 V
Dynamic II	125°C	240 hr	7 V
Life Test	125°C	1000 hr	5.5 V Min.

All Inputs are Connected Through a 2 to 15-KΩ Resistor to the Following:

Test Package	Dynamic I[a]			Static I[b]			Static II[c]			Dynamic II[a]			Life Test[a]		
	D	J	K	D	J	K	D	J	K	D	J	K	D	J	K
Pin No.															
1	A6	—	—	V_{DD}	—	—	V_{SS}	—	—	A6	—	—	A6	—	—
2	A5	A6	A6	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A5	A6	A6	A5	A6	A6
3	A4	A5	A5	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A4	A5	A5	A4	A5	A5
4	A3	A4	A4	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A3	A4	A4	A3	A4	A4
5	A0	A3	A3	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A0	A3	A3	A0	A3	A3
6	A1	—	—	V_{DD}	—	—	V_{SS}	—	—	A1	—	—	A1	—	—
7	A2	A0	A0	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A2	A0	A0	A2	A0	A0
8	A14	A1	A1	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A14	A1	A1	A14	A1	A1
9	V_{SS}	A2	A2	V_{SS}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A2	A2	V_{SS}	A2	A2
10	$\phi 1$	—	—	V_{DD}	—	—	V_{SS}	—	—	$\phi 1$	—	—	$\phi 1$	—	—
11	A13	A14	A14	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A13	A14	A14	A13	A14	A14
12	A12	V_{SS}	V_{SS}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A12	V_{SS}	V_{SS}	A12	V_{SS}	V_{SS}
13	A11	$\phi 1$	$\phi 1$	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A11	$\phi 1$	$\phi 1$	A11	$\phi 1$	$\phi 1$
14	A10	—	—	V_{DD}	—	—	V_{SS}	—	—	A10	—	—	A10	—	—
15	A9	A13	A13	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A9	A13	A13	A9	A13	A13
16	A8	A12	A12	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A8	A12	A12	A8	A12	A12
17	A7	A11	A11	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	A7	A11	A11	A7	A11	A11
18	V_{DD}	A10	A10	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{DD}	A10	A10	V_{DD}	A10	A10
19	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
20	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
21	—	A9	A9	—	V_{DD}	V_{DD}	—	V_{SS}	V_{SS}	—	A9	A9	—	A9	A9
22	—	A8	A8	—	V_{DD}	V_{DD}	—	V_{SS}	V_{SS}	—	A8	A8	—	A8	A8
23	—	A7	A7	—	V_{DD}	V_{DD}	—	V_{SS}	V_{SS}	—	A7	A7	—	A7	A7
24	—	V_{DD}	V_{DD}	—	V_{DD}	V_{DD}	—	V_{DD}	V_{DD}	—	V_{DD}	V_{DD}	—	V_{DD}	V_{DD}

NOTE: Dash (—) indicates no connection.

[a]The following timing waveforms are used for the Dynamic and Life Tests.



92CS-37686

A1 to A14 are successive divisions by 2 based on A0

[b]Memory array is pre-initialized with all 1's.
[c]Memory array is pre-initialized with all 0's.

Table III — Delta Limits and Calculations

Parameter	Absolute Limit	Delta Limit
I_{DD}	100 μA	± 30 μA
I_{OL} and I_{OH}	—	± 10% of 0 hr value
I_{OZ}	5 μA	± 500 nA

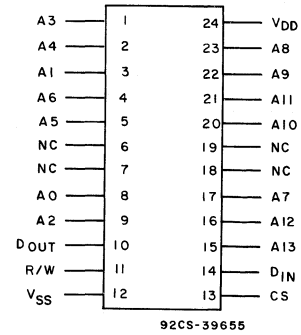
Delta Calculation	Initial Reading	Final Reading
I	Interim Electrical Tests I	Interim Electrical Tests II
II	Interim Electrical Tests I	Interim Electrical Test III
III	Interim Electrical Tests I	Interim Electrical Tests IV

CMM6167/1RZ

High-Reliability, Radiation-Hardened CMOS 16,384-Word by 1-Bit Static RAM Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 100k rads (Si)*
- *Cosmic ray upset immunity typically 2×10^{-9} errors/bit day*
- *Latch-up free under transient radiation*
- *Transient upset $> 10^{10}$ rads/sec, 20-ns pulse*

Features:
- *Fast access time (t_{AVQV}): 125 ns at T_A=25° C*
- *Single power supply: 4.5 V to 6.5 V*
- *Low standby and operating power*
- *All inputs and outputs CMOS compatible*
- *Fully static operation*
- *3-state output*



TERMINAL ASSIGNMENT

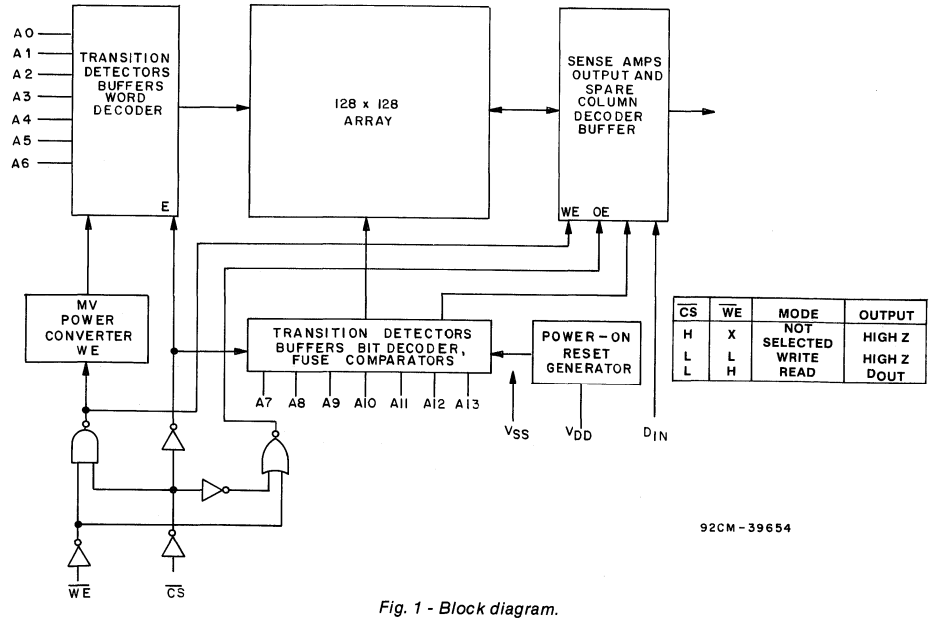


Fig. 1 - Block diagram.

CMM6167/1RZ

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%

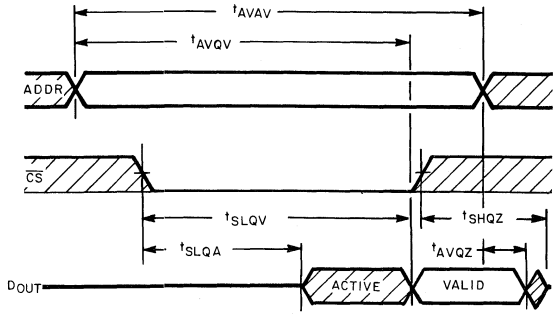
CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		-55° C, +25° C		+125° C		POST RADIATION† +25° C		
		Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent Device Current, I_{DD}	V_{IN} = 0 V or V_{DD}, V_{CS} = V_{DD}	—	0.1•	—	1•	—	4•	mA
Operating Device Current, I_{DD1}★	Cycle time = 1 μs	—	4.5•	—	5•	—	6•	
Output (Sink) Current, I_{OL}	V_{OUT} = 0.4 V	5•	—	3.5•	—	3.5•	—	
Output (Source) Current, I_{OH}	V_{OUT} = V_{DD} -0.4 V	3•	—	2•	—	2•	—	
Output Voltage, Low Level, V_{OL}		—	0.1	—	0.2	—	0.2	V
Output Voltage, High Level, V_{OH}		V_{DD} -0.1 V	—	V_{DD} -0.2 V	—	V_{DD} -0.2 V	—	
Input Low Voltage, V_{IL}		—	1.5•	—	1.5•	—	1.5•	
Input High Voltage, V_{IH}		3.5•	—	3.5•	—	3.5•	—	
Input Leakage Current, I_{IN}	V_{IN} = 0 V or V_{DD}	—	±2•	—	±10•	—	±10•	μA
3-State Output Leakage Current, I_{OZ}	Applied Voltages = 0 V or V_{DD}	—	±5•	—	±50•	—	±50•	
Input Capacitance, C_{IN}*		—	5	—	5	—	5	pF
Output Capacitance, C_{OUT}*		—	7	—	7	—	7	

•Limit with black dot (•) designates actual measurement, all other limits are designer's parameters under given test conditions.
†Radiation measurements are made on 2 samples/wafer. The limits shown are for within 1 hour of radiating to 100k rads (Si).
★Operating current measured using 1-MHz cycle and C_L = 50 pF.
*Capacitance measurements are made with no bias applied.

DYNAMIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%

CHARACTERISTIC		LIMITS						UNITS
		-55° C, +25° C		+125° C		POST RADIATION† +25° C		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read-Cycle Times (Fig. 2)								
Read Cycle Time,	t_{AVAV}	125	—	150•	—	150	—	ns
Address Access Time,	t_{AVQV}	—	125•	—	150•	—	150•	
Chip Select Access Time	t_{SLQV}	—	125•	—	150•	—	150•	
Chip Selection to Output Active	t_{SLQA}	5	—	5	—	5	—	
Output 3-State from Deselection	t_{SHQZ}	—	40	—	50	—	50	
Output Hold from Address Change	t_{AVQZ}	5	—	5	—	5	—	
Write-Cycle Times (Fig. 3)								
Write Cycle Time	t_{AVAV}	115	—	140	—	140	—	ns
Write Pulse Width	t_{WLWH}*	75•	—	95•	—	95•	—	
Address Hold Time from End of Write	t_{WHAV}	20	—	20	—	20	—	
Address Valid to Write Set-up	t_{AVWL}	0	—	0	—	0	—	
Address Valid to End of Write	t_{AVWH}	95•	—	120•	—	120•	—	
Address Valid to Chip Selection	t_{AVSL}	0•	—	0•	—	0•	—	
Chip Selection to End of Write	t_{SLWH}	95•	—	120•	—	120•	—	
Data Valid to End of Write	t_{DVWH}	30•	—	40•	—	40•	—	
Data Hold Time from End of Write	t_{WHDX}	20•	—	25•	—	25•	—	

•Limit with black dot (•) designates actual measurement, all other limits are designer's parameters under given test conditions.
*CS and WE must overlap for at least t_{WLWH} min. - t_{DVWH} min. must occur during this overlap.
†Radiation measurements are made on 2 samples/wafer. The limits shown are for within 1 hour of radiating to 100k rads (Si).

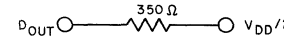


NOTE:
$\overline{WE}$ IS HIGH DURING THE READ CYCLE.
TIMING MEASUREMENT REFERENCE LEVEL IS $V_{DD}/2$

92CS-36513RI

Fig. 2 - Read-cycle timing waveforms.

AC TEST CONDITIONS
INPUT HIGH/LOW VOLTAGES: V_{DD}/V_{SS}
INPUT RISE/FALL TIMES: 6 NS
INPUT TIMING REFERENCE LEVEL: $V_{DD}/2$
OUTPUT TIMING REFERENCE LEVEL: $V_{DD}/2$
OUTPUT LOAD:

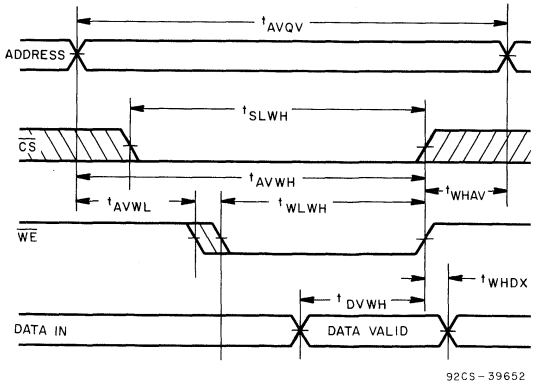


92CS-39655

Burn-In and Life-Test Circuits and Timing Waveforms

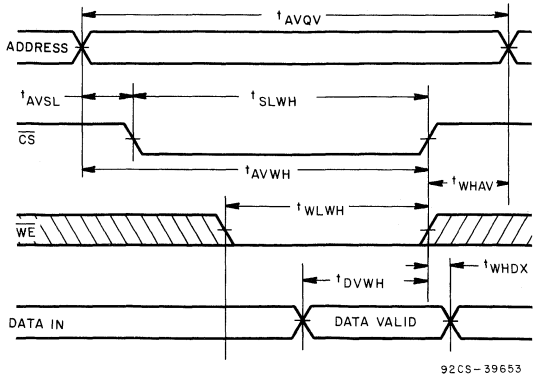
Test	Temperature	Duration	V_{DD}
Dynamic I	125° C	160 hr	7 V
Static I	125° C	24 hr	7 V
Static II	125° C	24 hr	7 V
Dynamic II	125° C	240 hr	7 V
Life Test	125° C	1000 hr	5.5 V Min.

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



92CS-39652

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)



92CS-39653

Fig. 3 - Write-cycle timing waveforms.

Delta Limits and Calculations

Parameter	Absolute Limit	Delta Limit
I_{DD}	100 μA	± 30 μA
I_{OL} and I_{OH}	—	± 10% of 0 hr value
I_{OZ}	5 μA	± 500 nA

Delta Calculation	Initial Reading	Final Reading
I	Interim Electrical Tests I	Interim Electrical Tests II
II	Interim Electrical Tests I	Interim Electrical Test III
III	Interim Electrical Tests I	Interim Electrical Tests IV

The EPIC Family

The emulation and programmable IC family formerly known as the GPU chip set, composed of several CMOS/SOS chips, is a high-performance microcomputer "building block" set which can be used to replace existing minicomputers by emulating (adapting) the minicomputers software for a wide variety of new applications with unique architecture, at comparable or increased speed and greatly reduced power.

The EPIC family represents the culmination of several years of engineering effort to develop a versatile microcomputer chip set which can be used for computing and signal processing.

The primary environment for the chip set is bit-slice micro/miniprocessors that are microprogrammable. The figure below shows the block diagram for such an architecture made up of a control section and a processing section. A typical control section consists of a microprogram memory, a microprogram sequencer or controller, and some additional logic. The microprogram memory (ROM or RAM) contains the microinstructions that specify the steps through which the machine sequences and controls the parallel operation of the bit-slices. The sequencer provides the macroinstruction decode logic, and determines how the next microprogram address is generated for sequencing the microprogram.

The size of the microprogram memory expands vertically as a function of the number of macroinstructions in the instruction set. The width of the microinstruction is expanded by cascading a number of similar memory chips.

All arithmetic and logic operations are carried out in the processing section which is composed of functionally equivalent bit-slice chips. In general, a typical slice contains some or all of the following: an ALU, a multiple word register file, a shifter, input and output data lines, and control inputs.

In the basic configuration shown, the microprocessor fetches macroinstructions from the system's main memory under the direction of microinstructions read from its microprogram memory. The operation code of the macroinstruction is "interpreted" by the microprogram sequencer, i.e. mapped into a microprogram memory address and then executed as a series of microsteps. The operand portion (if any) of the macroinstruction is routed to the bit-slices and used either in computations or in main memory address manipulation.

The system's main memory contains the machine-level instructions. The microprogram memory of the control section contains microprograms that define the macroinstructions; thus it gives the machine its "personality" or specific instruction set. Note that the microprogram memory also generates control pulses timed to control the rest of the system. These pulses could typically be latching data into registers or enabling data onto buses.

The EPIC family contains a number of LSI CMOS/SOS chips which, in various combinations, can be configured into microprogrammable computers with great flexibility of architecture, data format, and overall capability. In addition to all the advantages of CMOS technology, the SOS technology offers excellent tolerance to radiation, an important factor in aerospace applications.

The EPIC family centers around an 8-bit slice, two controllers or sequencers, an interrupt controller, an 8 x 8 bit multiplier slice, RAM and ROM, and a number of automated gate arrays that integrate the logic required to join the major system blocks into a minimum parts computer system.

Currently Available Devices (Objective Data)

General Processor	GP001
Emulating Controller	GP501
"2910" Type Controller	GP502
Multiplier (8 x 8)	GP503
Double Address Select Unit	GP514
Double Register Select Unit	GP515
Bus Interface Unit	GP516
Interrupt Control Unit	GP517
Voltage Level Converter and Buffer	GP511
Mask-Programmable ROM (512 x 8)	GP301
Mask-Programmable ROM (256 x 16)	GP302
Mask-Programmable ROM (512 x 16) with Pipeline Register	GP305

Applicable memories: Static CMOS/SOS

RAM (4096 x 1)	CMM5104/1RZ
RAM (1024 x 4)	CMM5114/1RZ
RAM (16384 x 1)	CMM6167/1RZ

For details, see section on RAMs.

A system is built around the 8-bit slice GP001 with the GP501 or the GP502 as a sequencer in the control section.

An alternative to using the peripheral devices (GP514, GP515 and GP516) is to implement a specific architecture through the semicustom approach using automated gate arrays or standard cells. (See Semicustom section.)

The GP503 and GP517 are stand-alone devices that enhance system performance. The multiplier (GP503) is useful where multiplication in software is too slow.

The level converter GP511 allows interfacing between 5- and 10-volt systems in either direction.

Note that in case of breadboarding or evaluation, where speed is not paramount, the EPIC parts can also be operated at 5 volts. In this instance, voltage level converters are avoided and the QMOS high-speed MSI parts (74HC series) are excellent choices for tying the bit-slices and the controller together in a working computer system.

All EPIC parts are available in both radiation-hardened and non-radiation-hardened versions.

Development Aids for Generating Microcode

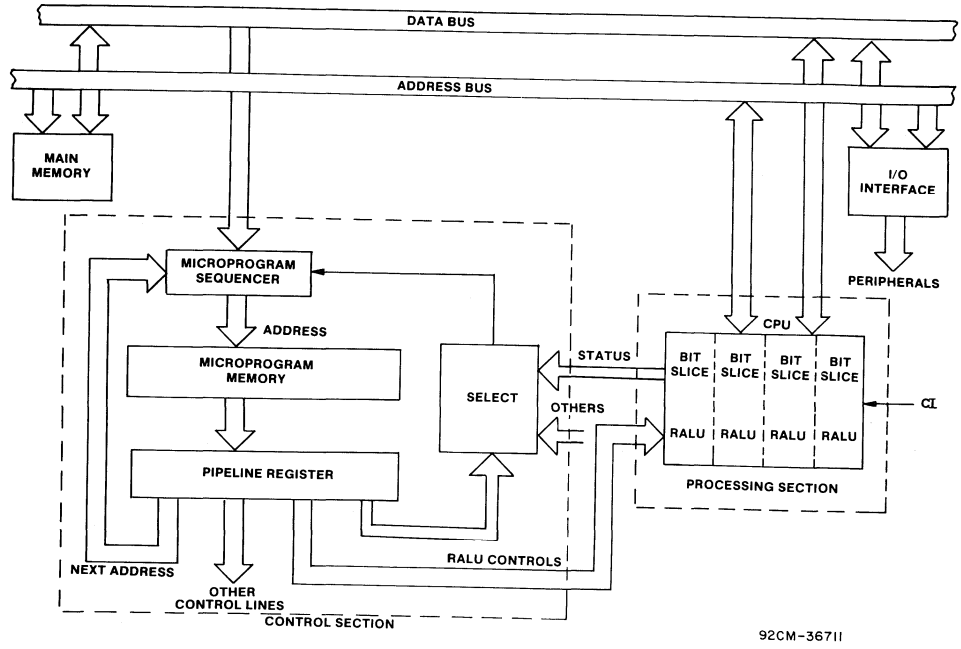
At least two manufacturers offer bit-slice development systems. Generally two approaches are offered for developing object code. The microcode can be developed by cross software installed on a big computer. The cross software include a Meta assembler which allows user definitions of mnemonics. The program is then downloaded via an RS232 port into a writeable control store in the development system for further debugging. The other approach is a stand-alone station with terminal, keyboard, and floppy disk with a Meta assembler and other software generally operating under CP/M, or an IBM-PC/XT/AT under PC-DOS.

For further information contact directly the companies:

1. STEP ENGINEERING
   756 Pastoria Avenue, Sunnyvale, CA. 94086

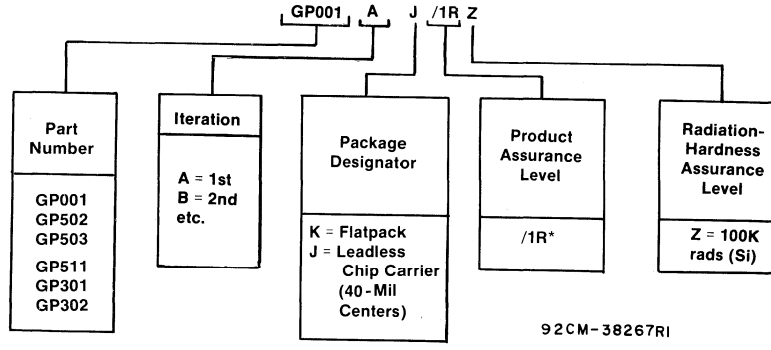
2. HILEVEL TECHNOLOGY, INC.
   18902 Bardeen Way, Irvine, CA. 92715

The EPIC Family



Basic microprogrammable bit-slice microcomputer.

Guide to the Part Number, Package Designator, and Product Assurance Level of the High-Reliability EPIC Chip Set.



*Selected EPIC devices are available to RCA /3 screening.

GP001A/1RZ

Advance Information/
Preliminary Data

CMOS/SOS 8-Bit General Processor Unit (GPU)

Aerospace Class S Screening

Features:

- *Fully static operation to 10 MHz*
- *Full military temperature range operation*
- *16 dual-access 8-bit general-purpose registers*
- *8-bit parallel Arithmetic Logic Circuit (ALC)*
- *Expandable*
- *Separate data input and data output*
- *Tri-state outputs*
- *Pipeline operation*

Radiation Features:

- *Radiation hardened to 100K rads (Si)*
- *Latch-up free under transient radiation*
- *Resistance to upset under transient radiation rate of up to 1 x 10^{10} rads (Si)/sec*

The RCA GP001 is an 8-bit, central-processing-unit bit slice intended for use in CPU's, peripheral controllers, micro-programmable computers, and dedicated controllers. It is a high-speed, low-power CMOS/SOS device that can be cascaded, allowing it to efficiently emulate any computer whose word lengths are in multiples of eight bits.

The performance of the GP001 is the result of the coordinated exercise of several distinct subfunctions: a two-port register file, a port 1 buffer register, (P1B), a port 2 buffer register (P2B), a left data type selector (LDTS), a right data type selector (RDTS), an arithmetic logic circuit (ALC), a shifter, a boundary and connect control, separate data input and data output paths and a temporary storage (TS) flip-flop. All of these functions are shown in Fig. 1. The GPU is capable of full-cycle-operation up to 10 MHz; that is, it can access two operands from the file, operate on them through the ALC and store the result in the register file. A more detailed description of each of these subfunctions and their operation is presented below.

The GP001A/1RZ is available in a 64-lead ceramic flat pack (K suffix) and in a 48-contact leadless chip carrier (J suffix).

ARCHITECTURE

Register File

The register file contains 16 words of 8-bits each. The file is parallel-word organized with two 8-bit outputs reflecting the contents of the register enabled to the respective ports. The two output ports are referred to hereafter as port 1 and port 2. Any two words addressed by the addresses R and T can be read simultaneously at port 1 and port 2, respectively. Identical data appears at both ports if R and T are equal. Port 1 is addressed via the 4-bit R address; port 2 is addressed via the 4-bit T address.

Data is stored into a selected register through a separate write-data path and under direct control of the load clock (LC). The register addressed by the R address field (port 1) receives data which replaces its previous contents when the load clock goes high. When the clock returns low, the data is locked into the register, i.e., the register is disconnected from the write-data path. Note that it is not possible to write into a register addressed by the T address field.

Port Buffers P1B and P2B

Ports 1 and 2 are connected to port buffers 1 and 2, P1B and P2B, respectively. These buffers operate in different modes under control of the load clock and some of the programming bit fields: S (source select), M (destination select), and A (ALC function).

Port 1 Buffer (P1B) - Port buffer P1B can operate in three different modes, depending on bit-fields S and M. In mode 1, P1B functions as a latch for the direct-input data, DI. In this mode P1B follows DI while LC is low. Data is latched, retaining the value of DI, at the time of the rising clock edge.

In mode 2, port buffer P1B becomes a master/slave register and takes its input (Port 1) from the register file. In this mode, hereafter referred to as the master/slave mode, the contents of the register file are written into the master when the load clock is high. At the negative-going edge of the clock, the slave is isolated from the master and retains its contents. New data can be entered at the next negative-going clock edge. In mode 2 address field R does not affect buffer P1B when the load clock is low. If R or the contents of the register file (R) change while the clock is low, port buffer P1B will retain its data from the last high-to-low clock transition. This mode is used for writing into the register file from DI.

In mode 3, the P1B buffer **in combination** with the addressed register file forms a master/slave function. While the load clock is high, data is written into the addressed register file (R). At the negative-going clock edge, the data is locked in

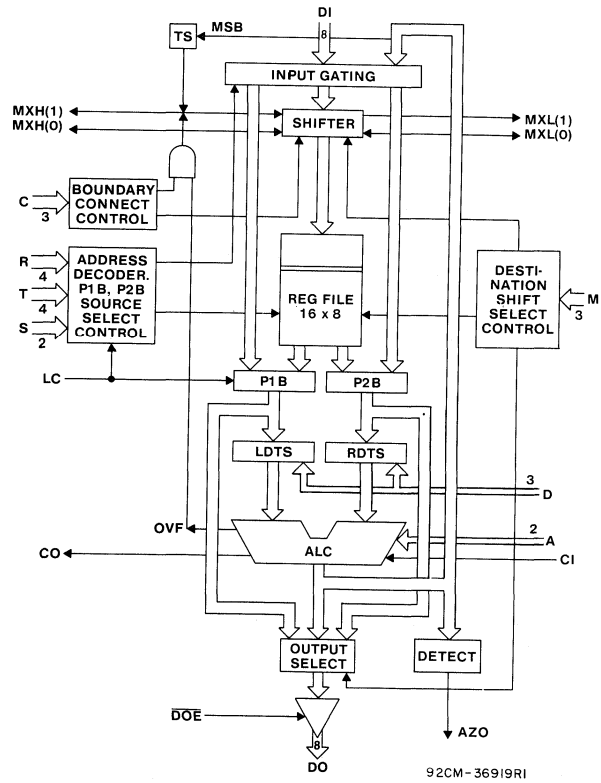
the master while the slave (P1B) follows the contents of the register file. At the next rising clock edge, the master is once more write-enabled while the contents in the slave are locked up for the duration of the high clock cycle.

If the address field R changes while the clock is low, new data is entered into the slave (P1B). The operation of P1B during the low clock cycle, if the address is changed, is the only difference between modes 2 and 3. Mode 3 is referred to hereafter as the slave mode.

Port Buffer P2B - Port buffer P2B can also operate in three modes determined by the control fields A and S and the address field T. In the first mode, mode 1, P2B is simply a data follower to incoming data from DI, and is independent of the clock.

In mode 2, which is similar to the slave mode described for P1B, port buffer P2B **in combination** with the register file addressed by T forms a master/slave register. As long as the load clock is low, the slave follows the contents of the master, i.e., the register file addressed by T. At the rising clock edge, the master is disconnected and the contents of the slave are stored. At the next negative-going clock edge, the slave can change if the contents of the master change. As described earlier, if the address T changes while the clock is low, P2B will follow the contents of the newly addressed register file. (Note that there is no write path into a register file addressed by T.)

In mode 3, P2B is simply disconnected from the master (register file) by control bits S and A. Whatever the contents were at the time of disabling, they remain indefinitely until the mode is changed.



CMOS 8-BIT GPU

Fig. 1 - Block diagram of the CMOS 8-bit general processor unit, GP001.

GP001A/1RZ

Data Sources for Register File

The 3-bit M field determines the source of the data to be written into the register file. If M = 100, the load clock is disabled and nothing can be written into the register file. If M = 000 and S = 01, DI is written into the register file. If M = 001, 010, or 011, the output of the shifter is written into the register file. If M = 101, 110, or 111, the output of the ALC is written into the register file.

Arithmetic-Logic-Circuit (ALC) Operations

The two data type selectors select data for the ALC inputs primarily under control of the D bit field. The left data type selector (LDTS) receives data from P1B and supplies the left ALC port with P1B unmodified, P1B complemented, all zeroes, or P1B right-shifted one bit. For right shift (via LDTS) the A bits must also be programmed (A = 01). In the case where the left operand of the LDTS (P1B) is shifted right one bit, the most significant bit (i.e., the bit that is shifted in) is controlled by the C bit field. For C = 001, the most significant bit of LDTS receives its input from MXH(1), and the least significant bit of LDTS is output to MXL(1). For some values of C, a sign extended shift is caused: i.e., the most significant bit of the left ALC operand is set equal to bit 7 of P1B.

The right data type selector (RDTS) receives data from P2B and supplies the right ALC port with P2B unmodified, P2B complemented, or all zeros. The ALC, controlled by the A bits, provides three basic functions from the GPU: ADD, logical OR, and logical AND. There is one-carry-input to the least significant bit, and one carry-output from the most significant bit. A group look-ahead carry circuit is incorporated in the ALC.

The GPU detects boundary conditions during arithmetic operations and indicates overflow. Overflow is defined as a change in the sign bit when performing addition or subtraction. For example, if the sign bit goes to a one state (negative) during the addition of two positive numbers, overflow has occurred. The GPU detects overflow by taking the exclusive OR of the carry-into and the carry-out of the most significant bit. The overflow signal output is time-shared with shift data on the MHX(1) pin under control of the C bits.

Detection of an all-zero output (AZO) of the ALC is also provided. An external pull-up resistor is required for the AZO output, permitting a wire-OR when more than one GPU is used. An all-zero group status is represented by a logical 1 on the bused AZO; a not-all zero group status is represented by a logical zero.

Note that for logical operations, the carry-out always equals the carry-in. Of course, the carry bit will not affect the result of AND and OR operations.

The ALC functions and data-type operands that can be selected are combined in a matrix in Fig. 2, which shows the various functions that can be implemented by programming the A and D fields. The basic arithmetic and logical functions are:

ADD	AND
SUBTRACT	OR
COMPLEMENT	NAND
INCREMENT	NOR
CLEAR	SHIFT RIGHT AND ADD
PASS	

D \ A	00	01	10	11	MNEMONICS 00	01	10	11
000	$\overline{R}$+CI	$\overline{R}$+CI	0	$\overline{R}$	COMP R [1]	COMP R [1]	CLR	NOT R
001	L+$\overline{R}$+CI	L+$\overline{R}$+CI	L ∧ $\overline{R}$	L ∨ $\overline{R}$	SUB L, R [2]	SUB L, R [2]	INHL, R [4]	IMP R, L [5]
010	$\overline{L}$+$\overline{R}$+CI	$\frac{L}{2}$+$\overline{R}$+CI	$\overline{L}$ ∧ $\overline{R}$	$\overline{L}$ ∨ $\overline{R}$		SUB $\frac{L}{2}$, R [3]	NOR L, R	NAND L, R
011	$\overline{L}$+CI	$\overline{L}$+CI	0	$\overline{L}$	COMP L [1]	COMP L [1]	CLR	NOT L
100	R+CI	R+CI	0	R	INC R [3]	INC R [3]	CLR	PASS R
101	L+R+CI	L+R+CI	L ∧ R	L ∨ R	ADD L, R	ADD L, R	AND L, R	OR L, R
110	$\overline{L}$+R+CI	$\frac{L}{2}$+R+CI	$\overline{L}$ ∧ R	$\overline{L}$ ∨ R	SUB R, L [2]	ADD $\frac{L}{2}$, R [4]	INH R, L [4]	IMP L, R [5]
111	L+CI	L+CI	0	L	INC L [3]	INC L [3]	CRL	PASS L

∧ = AND, ∨ = OR, ∀ = EX. OR

NOTES:
1. CI = 1, TWO'S COMPLEMENT
2. CI = 1, TWO'S COMPLEMENT ARITHMETIC
3. CI = 1
4. INH L, R = L ∧ $\overline{R}$ } INHIBIT FUNCTION
   INH R, L = $\overline{L}$ ∧ R }
   L ∀ R = (L ∧ $\overline{R}$) ∨ ($\overline{L}$ ∧ R)
5. IMP R, L = $\overline{L}$ ∨ $\overline{R}$ } IMPLICATION FUNCTION
   IMPL, R = $\overline{L}$ ∨ R }
   L ∀ R = (L ∨ $\overline{R}$) ∧ ($\overline{L}$ ∨ R)

92CM-36920

Fig. 2 - Operand and arithmetic-logic unit function matrix.

The shift right one bit and ADD function is useful in implementing multiply algorithms. Note also that P1B-P2B and P2B-P1B subtractions can be done. Exclusive OR and exclusive NOR functions can be performed, but require more than one microcycle.

Shift Operations

In addition to the one-bit right shift of LDTS described above, there is a dedicated shifter providing powerful left-right shift capability on the output of the ALC before it is stored back in the register file. The shift-select logic is capable of straight-through (no shift) operation, shifting the ALC output one bit position right, two bit positions right, or one bit position left. The destination of the shifted data is always the register specified by the port 1 address (R field). Direct data input (DI) to the register file from the data input pins also flows through the shifter (unshifted). Again, data is written into the register specified by the port 1 address. The shift function is determined directly by the M bits. The M field can also disable the load clock to the register file, thereby preventing data from being written. The C bits control shifting indirectly; they are the boundary connect control.

During a shift operation, the user has a wide choice as to the shift carry that replaces the vacant bit position. For example, for M = 010 and C = 010, a one-bit right shift takes place with a 1 going into the most significant bit position.

The C field, which is the boundary connect control, determines what is input and output to four leads. MXH(1) and MXH(0) are the most significant shift bits and bidirectional pins. MXL(1) and MXL(0) are the least significant shift bits; of these, MXL(0) is bidirectional while MXL(1) represents tristate output only.

The C bits provide three general classes of states for the four MX shift pins. The first class configures the GPU for normal intercircuit shift operations in a multiple GPU machine (C = 001). The second class of states causes the overflow status indicator to be output on MXH(1) while zero or one is shifted into the shifter (C = 010 or 011). The third class of states causes special outputs to be connected to the MXH bits for left shifts and MSB extension for right shifts.

The C field conditions the data paths of the MX bits for shift operations; if a shift is not specified by the M bits, the C-bit decoding does not affect the data entering the shifter. C = 000 turns off the MXH bits regardless of the M-bit control; however, the MXL bits are not affected.

The Temporary Storage (TS) Bit

Bit 7 of the ALC output can be latched into the D-type flip-flop temporary storage bit, TS. TS is enabled for input only when C = 111. To store data in TS, the C bits must change to a value other than 111 before bit 7 of the ALC changes. Whenever TS holds meaningful data, C must never be allowed to equal 111, which could possibly happen on a transition of the C bits, for example, from 011 to 100.

Data Output

The GPU can output 8-bits in parallel on the data output (DO) pins if the data output enable ($\overline{DOE}$) signal is low. One of three values can be output on DO: the output of the ALC, the output of P1B, or the output of P2B. The M bit field controls the output gating.

For application information, refer to ICAN-7202, "An Introduction to the Use of the General-Processor Unit, GP001."

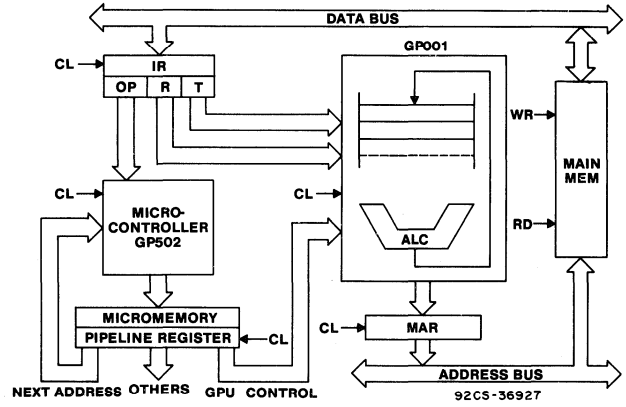


Fig. 3 - Typical microprogrammed architecture using 8-bit GPU slices, GP001.

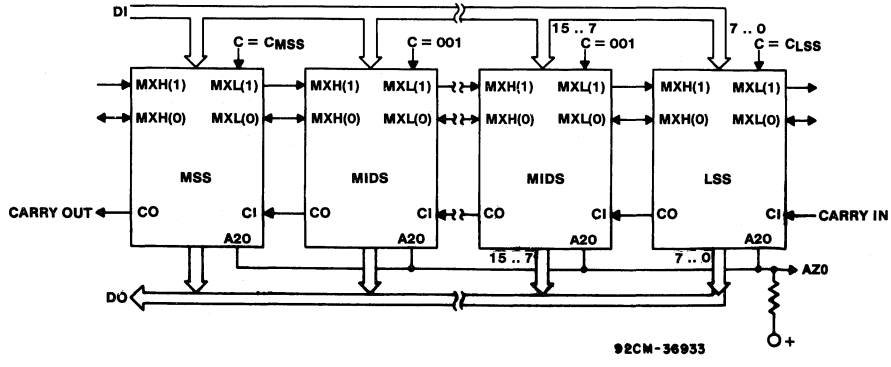


Fig. 4 - Concatenation of general processor units.

GP001A/1RZ

Input/Output Fields of GP001

A	S	D	M	C	CI	$\overline{DOE}$	LC	INPUT CONTROL FIELDS
2	2	3	3	3	1	1	1	Number of Bits

R	T	DI	MX *	DATA/ADDRESS INPUT FIELDS
4	4	8	3	Number of Bits

DO	CO	AZO	MX *	DATA OUTPUT FIELDS
8	1	1	4	Number of Bits

* 3 bits in the MX shift field are bi-directional. MXL1 is output only.

Definition of Fields for GP001

FIELD	FUNCTION
Control	
A	Select ALU Function
S	Select Source and Mode for Port Buffers
D	Select Left and Right Data Type into ALC
M	Select Data Path and Destination
C	Select Boundary Conditions for Shifts
$\overline{CI}$	Carry Input
$\overline{DOE}$	Data Output Enable
LC	Clock
Input Data/Address	
R	Address Field for Write/Read Register File
T	Address Field for Read Only Register File
DI	Data Input
MX *	Bits to be Shifted In
Output	
DO	Data Output
CO	Carry Out
AZO	Accumulator all Zero
MX *	Bits Shifted Out

* 3 bits in the MX field are bi-directional.

Pin/Signal List for GP001 in 48-Lead LCC

PIN NO.	MNEMONIC	DESCRIPTION	INPUT/ OUTPUT
1	V_{SS}	0 Volt, Ground Reference	—
2	DO3	Data Output, bit 3	O
3	DO4	Data Output, bit 4	O
4	DO5	Data Output, bit 5	O
5	DO6	Data Output, bit 6	O
6	DO7	Data Output, bit 7	O
7	$\overline{CO}$	Carry Out	O
8	$\overline{DOE}$	Data Out Enable	I
9	AZO	All Zero Detect Out	O
10	MXH0	Multiplexer-Shift High, bit 0	I/O
11	MXH1	Multiplexer-Shift High, bit 1	I/O
12	C0	Boundary, Connect Control bit 0	I
13	C1	Boundary, Connect Control bit 1	I
14	C2	Boundary, Connect Control bit 2	I
15	DI7	Data Input bit 7	I
16	DI6	Data Input bit 6	I
17	DI5	Data Input bit 5	I
18	DI4	Data Input bit 4	I
19	DI3	Data Input bit 3	I
20	DI2	Data Input bit 2	I
21	DI1	Data Input bit 1	I
22	DI0	Data Input bit 0	I
23	S1	Source Select Control bit 1	I
24	S0	Source Select Control bit 0	I

PIN NO.	MNEMONIC	DESCRIPTION	INPUT/ OUTPUT
25	V_{DD}	Power Supply	—
26	R2	Port 1 Register Select bit 2	I
27	R3	Port 1 Register Select bit 3	I
28	T2	Port 2 Register Select bit 2	I
29	T3	Port 2 Register Select bit 3	I
30	R1	Port 1 Register Select bit 1	I
31	T1	Port 2 Register Select bit 1	I
32	T0	Port 2 Register Select bit 0	I
33	R0	Port 1 Register Select bit 0	I
34	M1	Destination Select Control bit 1	I
35	M0	Destination Select Control bit 0	I
36	M2	Destination Select Control bit 2	I
37	MXL0	Multiplexer Shift Low bit 0	I/O
38	MXL1	Multiplexer Shift Low bit 1	O
39	LC	Load Clock	I
40	D2	Data Type Select Control bit 2	I
41	A0	ALU Control bit 0	I
42	A1	ALU Control bit 1	I
43	C1	Carry In	I
44	D1	Data Type Select Control bit 1	I
45	D0	Data Type Select Control bit 0	I
46	DO0	Data Output bit 0	O
47	DO1	Data Output bit 1	O
48	DO2	Data Output bit 2	O

TABLES FOR MICROPROGRAMMING THE GP001

ALC Functions

A	FUNCTION	OPERANDS
00	ADD	LEFT + RIGHT + CARRY-IN
01	ADD	LEFT + RIGHT + CARRY-IN
10	AND	LEFT AND RIGHT
11	OR	LEFT OR RIGHT

Source Select Control — S-Bit

S	Register File		P1B	P2B	
00	M≠000	No Effect	SLAVE TO REG(R)	A≠01	SLAVE TO REG(T)
	M=000	Write Inhibit		A=01	P2B-VALUE NOT CHANGING
01	M≠000	No Effect	M≠000 Latch for DI	A≠01	SLAVE TO REG(T)
	M=000	Write Enable	M=000 Master/Slave Mode	A=01	P2B-VALUE NOT CHANGING
10	M≠000	No Effect	SLAVE TO REG(R)	A≠01	FOLLOWS DI
	M=000	Write Inhibit		A=01	SLAVE TO REG(T)
11	M≠000	*R(0) ← 1	SLAVE TO REG(R+1)	A≠01	FOLLOWS DI
	M=000	Write Inhibit		A=01	SLAVE TO REG(T)

*LSB of R-Address is forced to one, thus only odd-address register can be accessed.

Data Type Selector Control — D-Bit

D	Left Data Type Select		Right Data Type Select	MXL(1)	
000	0		$\overline{P2B}$	M≠011	HIGH Z
				M=011	ALC(1)
001	P1B		$\overline{P2B}$	M≠011	HIGH Z
				M=011	ALC(1)
010	A≠01	$\overline{P1B}$	$\overline{P2B}$	M≠011	A≠01: HIGH Z; A=01: P1B(0)
	A=01	½ * P1B*		M=011	ALC(1)
011	$\overline{P1B}$		0	M≠011	HIGH Z
				M=011	ALC(1)
100	0		P2B	M≠011	HIGH Z
				M=011	ALC(1)
101	P1B		P2B	M≠011	HIGH Z
				M=011	ALC(1)
110	A≠01	$\overline{P1B}$	P2B	M≠011	A≠01: HIGH Z; A=01: P1B(0)
	A=01	½ * P1B*		M=011	ALC(1)
111	P1B		0	M≠011	HIGH Z
				M=011	ALC(1)

*Shifted right one bit. The value of this vacant (MSB) bit is determined by the C-bits.

GP001A/1RZ

Boundary and Connect Control — C-Bits

C	Shift Carries †				Left Data Type Select*	MXH(1)	MXH(0)		TS
	Left 1 Bit	Right 1 Bit	Right 2 Bits						
	Bit 0	Bit 7	Bit 7	Bit 6	Bit 7				
000	MXL(0)	ALC(7)⊕OVF**	ALC(7)⊕OVF**	ALC(7)⊕OVF**	PIB(7)	INPUT	INPUT		DISABLED
001	MXL(0)	MXH(0)	MXH(1)	MXH(0)	MXH(1)	INPUT	M≠01x	ALC(7)	DISABLED
							M=01x	Input	
010	1	1	1	1	UNDEF.	OVF	M≠01x	ALC(7)	DISABLED
							M=01x	HIGH Z	
011	0	0	0	0	UNDEF.	OVF	M≠01x	ALC(7)	DISABLED
							M=01x	HIGH Z	
100	MXL(0)	ALC(7)⊕OVF**	ALC(7)⊕OVF**	ALC(7)⊕OVF**	P1B(7)	ALC(6)	M≠01x	ALC(7)	DISABLED
							M=01x	HIGH Z	
101	MXL(0)	MXH(0)	TS	MXH(0)	TS	TS	M≠01x	ALC(7)	DISABLED
							M=01x	Input	
110	MXL(0)	MXH(0)	P2B(7)	MXH(0)	P2B(7)	P2B(7)	M≠01x	ALC(7)	DISABLED
							M=01x	Input	
111	MXL(0)	MXH(0)	P2B(7)	MXH(0)	P2B(7)	P2B(7)	M≠01x	ALC(7)	ENABLED
							M=01x	Input	

*Applicable only when D=x10 and A=01.

**MSB is set to Bit 7 of ALC output unless there is an overflow. Then the MSB is set to $\overline{\text{BIT 7}}$ of the ALC output.

†Signifies bits to be shifted into positions left empty by a shift operation.

Destination Select Control — M-Bits

M	DO*	SHIFTER	MXL(1)		MXL(0)	MXH(0)		LC	Source of Write-Data for Register File		P1B MODE	
000	ALC		D≠x10 or A≠01	High Z	HIGH Z	C≠000	ALC(7)	Enabled	S≠01	Write Inhibit	S≠01	Slave to Reg(R)
			D=x10 and A=01	P1B(0)		C=000	HIGH Z		S=01	DI	S=01	Master/Slave to Reg(R)
001	ALC	Shift left 1 bit	D≠x10 or A≠01	High Z	INPUT	C≠000	ALC(7)	Enabled	SHIFTER		S≠01	Slave to Reg(R)
			D=x10 and A=01	P1B(0)		C=000	HIGH Z				S=01	Latch for DI
010	ALC	Shift right 1 bit	D≠x10 or A≠01	High Z	ALC(0)	INPUT		Enabled	SHIFTER		S≠01	Slave to Reg(R)
			D=x10 and A=01	P1B(0)							S=01	Latch for DI
011	ALC	Shift right 2 bits	D≠x10 or A≠01	ALC(1)	ALC(0)	INPUT		Enabled	SHIFTER		S≠01	Slave to Reg(R)
			D=x10 and A=01	P1B(0)							S=01	Latch for DI
100	ALC		D≠x10 or A≠01	High Z	HIGH Z	C≠000	ALC(7)	Disabled	WRITE INHIBIT		S≠01	Slave to Reg(R)
			D=x10 and A=01	P1B(0)		C=000	HIGH Z				S=01	Latch for DI
101	ALC		D≠x10 or A≠01	High Z	HIGH Z	C≠000	ALC(7)	Enabled	ALC		S≠01	Slave to Reg(R)
			D=x10 and A=01	P1B(0)		C=000	HIGH Z				S=01	Latch for DI
110	P2B		D≠x10 or A≠01	High Z	HIGH Z	C≠000	ALC(7)	Enabled	ALC		S≠01	Slave to Reg(R)
			D=x10 and A=01	P1B(0)		C=000	HIGH Z				S=01	Latch for DI
111	P1B		D≠x10 or A≠01	High Z	HIGH Z	C≠000	ALC(7)	Enabled	ALC		S≠01	Slave to Reg(R)
			D=x10 and A=01	P1B(0)		C=000	HIGH Z				S=01	Latch for DI

*When $\overline{\text{DOE}}$=1, the DO pins are in the high-impedance state.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +11V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING FOR K PACKAGE TYPES):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	5	10.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 10 V ± 5%

CHARACTERISTIC		CONDITIONS	LIMITS						UNITS
			-55°C, +25°C		+125°C		POST ‡ RADIATION +25°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN} = 0 V or V_{DD}	—	2.5	—	3.0	—	3.0	mA
Operating Device Current	I_{OPR} (Note 3)	Open Circuit Outputs Cycle Time = 200 ns	—	10	—	12	—	12	mA
		Open Circuit Outputs Cycle Time = 1000 ns	—	2.5	—	3.0	—	3.0	mA
Input Leakage Current Low	I_{IL}	V_{IN} = 0 (Note 1)	—	20	—	40	—	40	μA
Input Leakage Current High	I_{IH}	V_{IN} = V_{DD} (Note 1)	—	20	—	40	—	40	μA
3-State Output Leakage Current	I_{OZL}	Applied Voltage = 0 V (Note 1)	—	20	—	40	—	40	μA
3-State Output Leakage Current	I_{OZH}	Applied Voltage = V_{DD} (Note 1)	—	20	—	40	—	40	μA
Output (Sink) Current (Note 4)	I_{OL1}	V_{OUT} = 0.5 V	8	—	6	—	6	—	mA
Output (Sink) Current	I_{OL2}	V_{OUT} = 0.5 V	4	—	3.0	—	3.0	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{DD} -0.5 V	2.25	—	1.75	—	1.75	—	mA
Output Voltage Low Level	V_{OL}	Note 2	—	0.5	—	0.5	—	0.5	V
Output Voltage High Level	V_{OH}	Note 2	9.5	—	9.5	—	9.5	—	V
Input Low Voltage	V_{IL}	V_{OUT} = 1 V or 9 V	—	3	—	3	—	3	V
Input High Voltage	V_{IH}	V_{OUT} = 1 V or 9 V	7	—	7	—	7	—	V

‡ The limits shown are for tests performed within 1 hour of radiating to 100 Krads (Si).

Notes: 1. All other inputs (non-measured) are held at opposite logic level.
2. Input levels shall be V_{DD} and V_{SS}. Outputs open.
3. Measured while running the vector set.
4. AZO.

GP001A/1RZ

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V

CHARACTERISTIC		CONDITIONS	LIMITS						UNITS
			-55°C, +25°C		+125°C		POST ‡ RADIATION +25°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN} = 0 V or V_{DD}	—	0.5	—	1.0	—	1.0	mA
Operating Device Current	I_{OPR}	Open Circuit Outputs Cycle Time = 200 ns	—	3	—	4	—	4	mA
		Open Circuit Outputs Cycle Time = 1000 ns	—	1	—	1.5	—	1.5	mA
Input Leakage Current Low	I_{IL}	V_{IN} = 0 (Note 1)	—	10	—	20	—	20	μA
Input Leakage Current High	I_{IH}	V_{IN} = V_{DD} (Note 1)	—	10	—	20	—	20	μA
3-State Output Leakage Current	I_{OZL}	Applied Voltage = 0 V (Note 1)	—	10	—	20	—	20	μA
3-State Output Leakage Current	I_{OZH}	Applied Voltage = V_{DD} (Note 1)	—	10	—	20	—	20	μA
Output (Sink) Current	I_{OL1}	V_{OUT} = 0.4 V	4	—	3	—	3	—	mA
Output (Sink) Current	I_{OL2}	V_{OUT} = 0.4 V	1.25	—	1	—	1	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{DD} -0.4 V	1.25	—	1	—	1	—	mA
Output Voltage Low Level	V_{OL}	Note 2	—	0.5	—	0.5	—	0.5	V
Output Voltage High Level	V_{OH}	Note 2	4.5	—	4.5	—	4.5	—	V
Input Low Voltage	V_{IL}	V_{OUT} = 0.5 V or 4.5 V	—	1.5	—	1.5	—	1.5	V
Input High Voltage	V_{IH}	V_{OUT} = 0.5 V or 4.5 V	3.5	—	3.5	—	3.5	—	V

‡ The limits shown are for within 1 hour of radiating to 100 Krads (Si).

Notes: 1. All other inputs (non-measured) are held at opposite logic level.
2. Input levels shall be V_{DD} and V_{SS}.
3. Measured while running the vector set.
4. AZO.

DYNAMIC ELECTRICAL CHARACTERISTICS, V_{DD} = 10 V ± 5%

CHARACTERISTIC	PROP. DELAY	MAXIMUM LIMITS			UNITS	FIG.
		-55°C, +25°C	+125°C	POST ‡ RADIATION +25°C		
A → ALU (OR) → DO	t_{PD}	95	120	120	ns	5
LC → AZO_{LH}	t_{PD}	165	200	200	ns	6
S → P1B → DO	t_{PD}	70	90	90	ns	7
LC → ALU (ADD) → DO	t_{PD}	75	95	95	ns	8
LC → ALU (AND) → DO	t_{PD}	85	105	105	ns	8
LC → ALU (OR) → DO	t_{PD}	75	95	95	ns	8
LC → MXH0	t_{PD}	90	115	115	ns	9
LC → MXH1	t_{PD}	75	95	95	ns	9
LC → MXL0	t_{PD}	75	95	95	ns	9
LC → MXL1	t_{PD}	80	100	100	ns	9
(R) → P1B → DO	t_{PD}	95	120	120	ns	10
(T) → P2B → DO	t_{PD}	95	120	120	ns	10
CI → CO	t_{PD}	30	40	40	ns	11

‡ Radiation measurements are made on two samples/wafer. The limits shown are for tests performed within one hour of radiating to 100 Krads (Si).

DYNAMIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V

CHARACTERISTIC	PROP. DELAY	MAXIMUM LIMITS			UNITS	FIG.
		-55°C, +25°C	+125°C	POST ‡ RADIATION +25°C		
A → ALU (OR) → DO		200	250	250		5
LC → AZO_{LH}		330	410	410		6
S → P1B → DO		145	180	180		7
LC → ALU (ADD) → DO		170	210	210		8
LC → ALU (AND) → DO		190	230	230		8
LC → ALU (OR) → DO		160	200	200		8
LC → MXH0	t_{PD}	190	230	230	ns	9
LC → MXH1		185	230	230		9
LC → MXL0		180	225	225		9
LC → MXL1		180	225	225		9
(R) → P1B → DO		220	275	275		10
(T) → P2B → DO		220	275	275		10
CI → CO		70	90	90		11

‡ Radiation measurements are made on two samples/wafer. The limits shown are for tests performed within one hour of radiating to 100 Krads (Si).

Timing Diagrams for Dynamic Electrical Characteristics

Figure numbers are referred to in Dynamic Electrical Characteristics Charts.

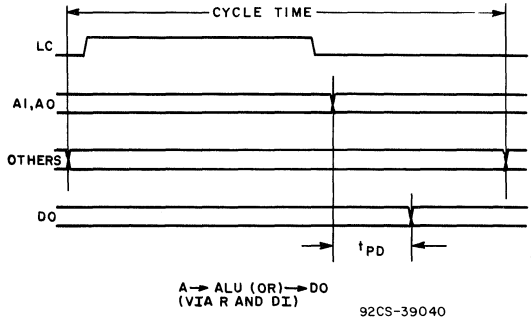


Fig. 5

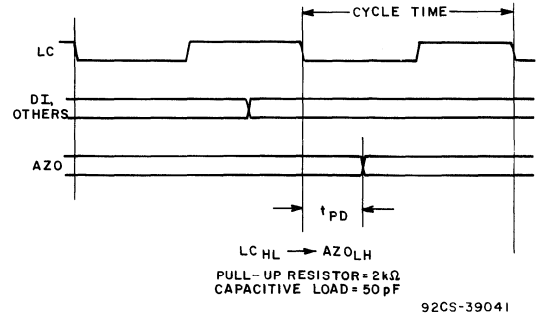


Fig. 6

GP001A/1RZ

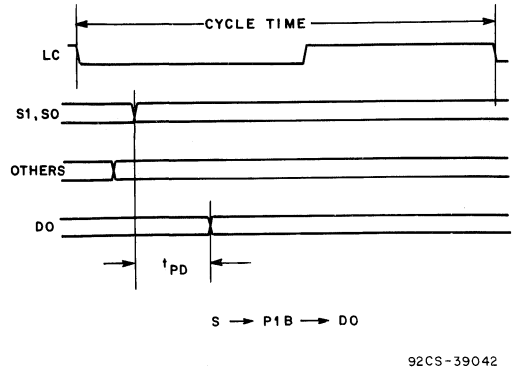


Fig. 7

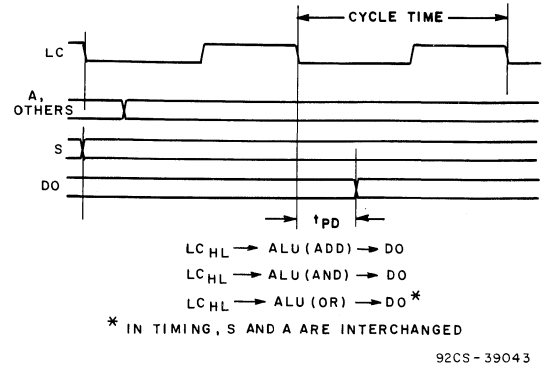


Fig. 8

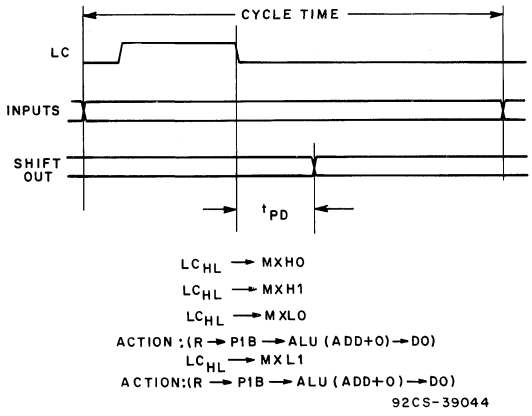


Fig. 9

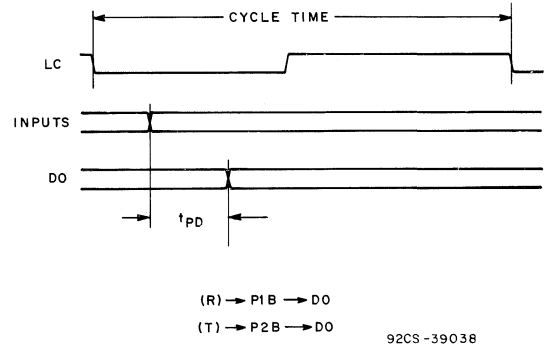


Fig. 10

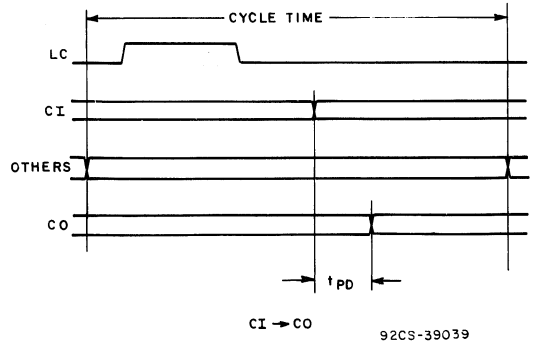


Fig. 11

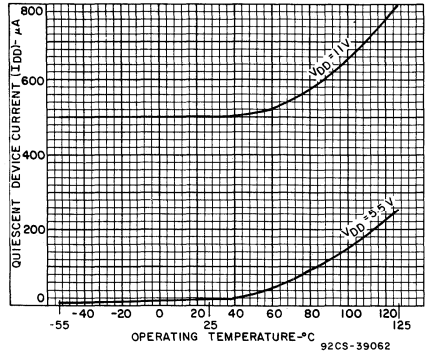


Fig. 12 - Typical quiescent device current as a function of operating temperature.

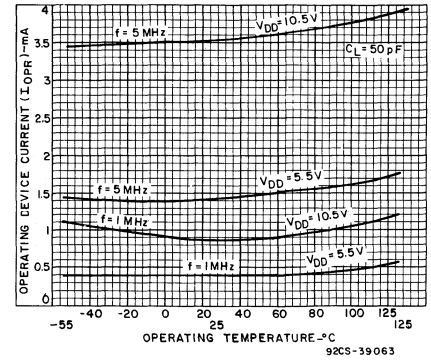


Fig. 13 - Typical operating device current as a function of operating temperature.

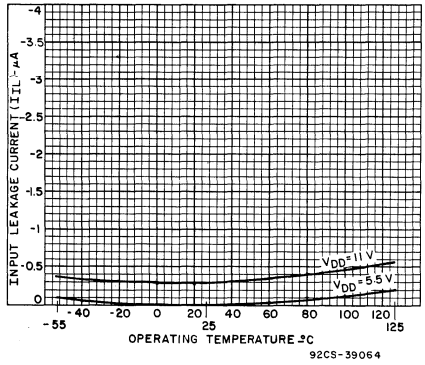


Fig. 14 - Typical input leakage current low as a function of operating temperature.

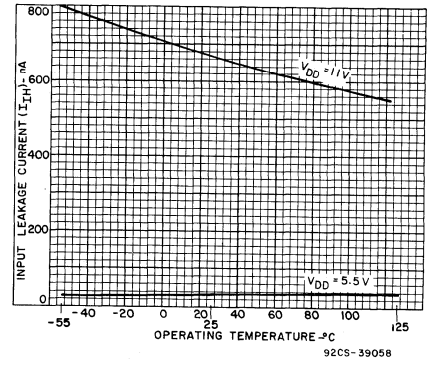


Fig. 15 - Typical input leakage current high as a function of operating temperature.

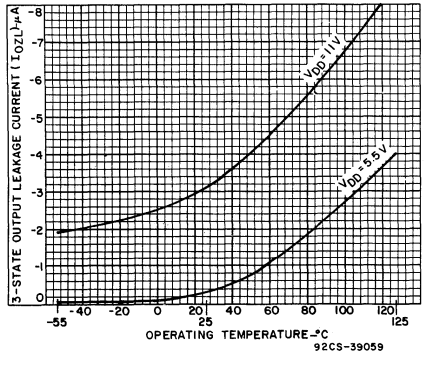


Fig. 16 - Typical 3-state output leakage current as a function of operating temperature.

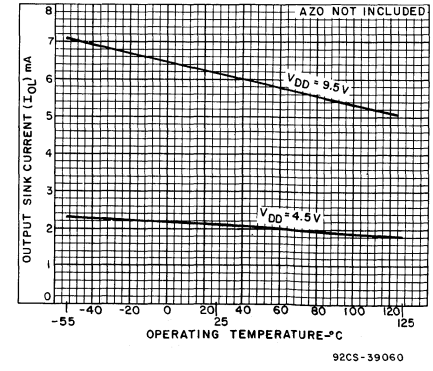


Fig. 17 - Typical output sink current as a function of operating temperature.

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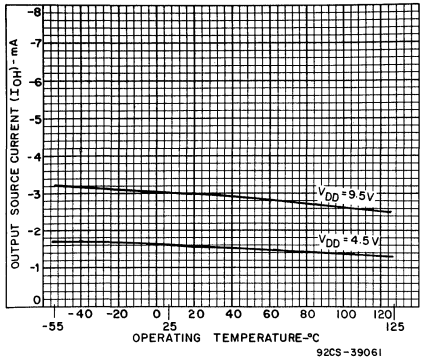


Fig. 18 - Typical output source current as a function of operating temperature.

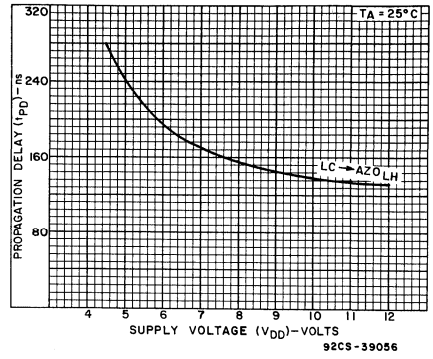


Fig. 19 - Typical propagation delay times as a function of supply voltage.

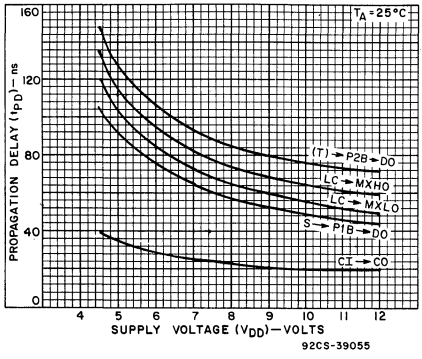


Fig. 20 - Typical propagation delay times as a function of supply voltage.

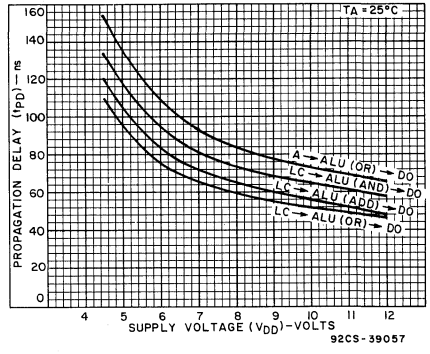


Fig. 21 - Typical propagation delay times as a function of supply voltage.

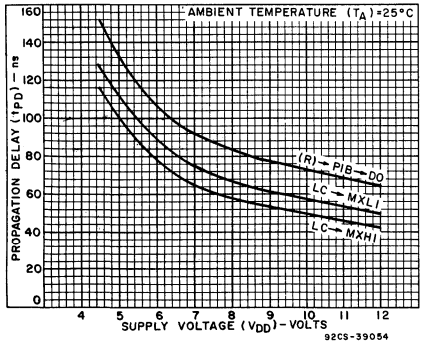


Fig. 22 - Typical propagation delay times as a function supply voltage.

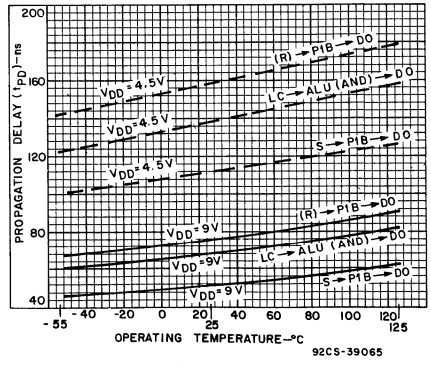


Fig. 23 - Typical propagation delay times as a function of operating temperature.

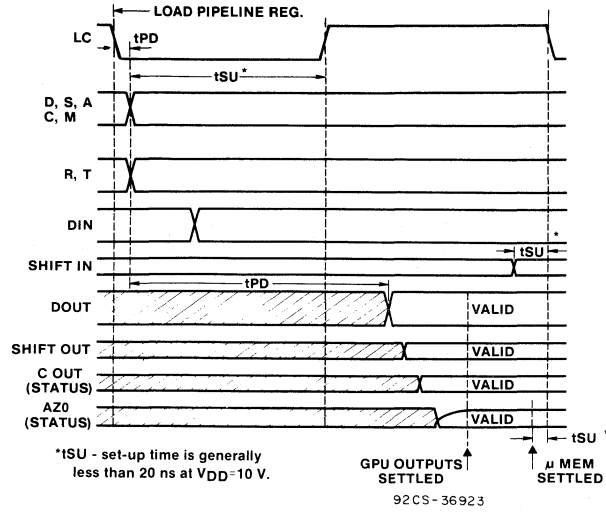
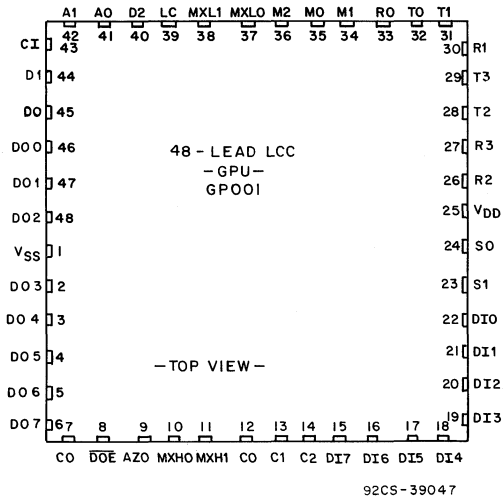
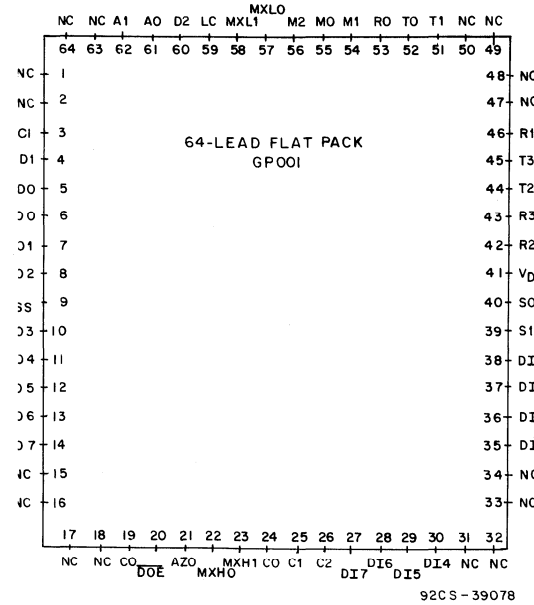


Fig. 24 - Timing diagram of major events in a microcycle.



TERMINAL ASSIGNMENT FOR J PACKAGE (48-CONTACT, LEADLESS CHIP CARRIER)



TERMINAL ASSIGNMENT FOR K PACKAGE (64-LEAD, CERAMIC FLATPACK)

GP001A/1RZ

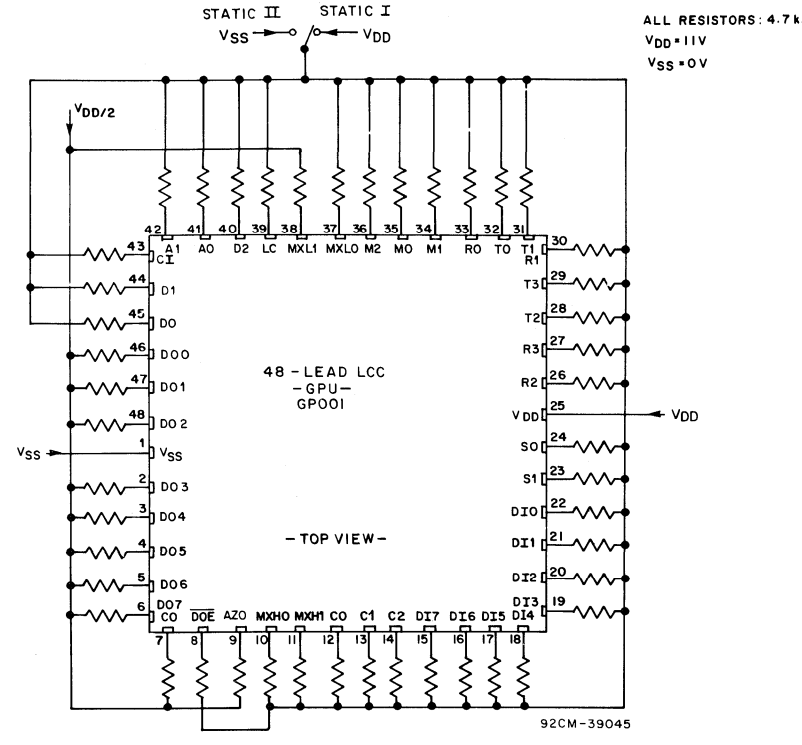


Fig. 25 - 48-Lead LCC static I and II burn-in circuit.

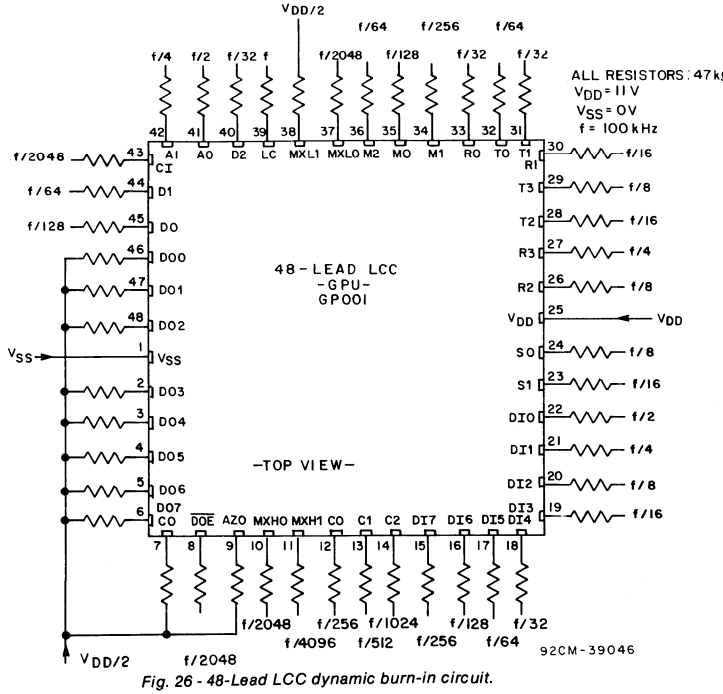


Fig. 26 - 48-Lead LCC dynamic burn-in circuit.

Advance Information/
Preliminary Data

GP301/1RZ, GP302/1RZ

High-Reliability, Radiation-Hardened CMOS 4096-Bit Mask-Programmable Static Read-Only Memories

Features:

- *CMOS/SOS circuitry for low power and high speed*
- *Fully static operation*
- *No minimum clock is required*
- *Single power supply*
- *High noise immunity*
- *Full military temperature-range operation*
- *40-mil center hermetic leadless package for high packing density*
- *Typical, 10-V operation*
- *High-speed access time–typically 60 ns at 10 V, 25°C*
- *Metal-mask programmable*
- *Low power–50 μA typical at 10 V, 25°C*
- *Tri-state outputs*
- *Output latch capability*
- *Pipeline operation*
- *Radiation hardened to 100K rads (Si)*

The GP301/1RZ and GP302/1RZ are fully static 4096-bit metal-mask-programmable CMOS/SOS Read-Only Memories (ROMs), organized as 512 words by 8 bits and 256 words by 16 bits, respectively.

The data are permanently stored in the memory by use of custom-developed pattern masks. These ROMs have a unique feature that makes them suitable for microprogram applications. Output latch operation allows them to hold data while the address inputs are changed.

The GP301/1RZ and GP302/1RZ are supplied in 32-contact hermetic leadless packages (J suffix).

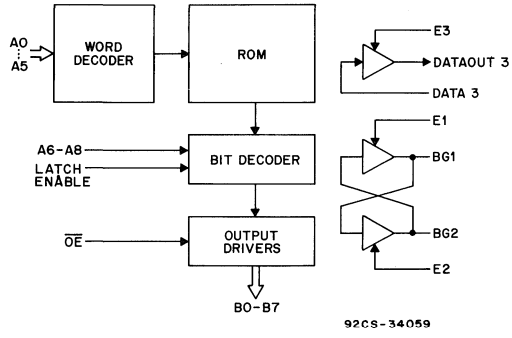


Fig. 1 - GP301 block diagram.

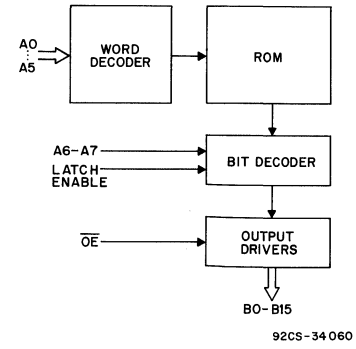


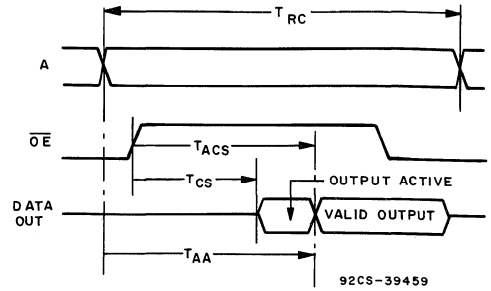
Fig. 2 - GP302 block diagram.

GP301/1RZ, GP302/1RZ

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CONDITIONS			LIMITS								UNITS
					-55°C		+25°C		+125°C		Post† Radiation +25°C		
		V_{DD} (V)	V_{IN} (V)	V_{OUT} (V)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent Device Current	I_{DD}	5	0, 5	—	—	500	—	500	—	1000	—	1000	
		10	0, 10	—	—	1000	—	1000	—	2000	—	2000	
Input Leakage Current, Low	I_{IL}	5	0, 5	—	—	5	—	5	—	10	—	10	μA
High	I_{IH}	10	0, 10	—	—	10	—	10	—	20	—	20	
3-State Output Leakage Current	I_{OZL}	5	0, 5	0, 5	—	8	—	8	—	15	—	15	
	I_{OZH}	10	0, 10	0, 10	—	15	—	15	—	30	—	30	
Output Drive Current (Sink)	I_{DN}	5	0, 5	0.4	1.8	—	1.4	—	1	—	1	—	mA
		10	0, 10	0.5	4.25	—	3.3	—	2.4	—	2.4	—	
Output Drive Current (Source)	I_{DP}	5	0, 5	4.6	0.75	—	0.6	—	0.5	—	0.5	—	
		10	0, 10	9.5	1.95	—	1.5	—	1	—	1	—	

†After 100K rads (Si) total dose.



LEGEND:
T_{RC} - CYCLE TIME (READ)
T_{ACS} - ACCESS TIME FROM CHIP-ENABLE SIGNAL
T_{CS} - DELAY TO ACTIVE
T_{AA} - ACCESS TIME FROM ADDRESS CHANGE

NOTE:
INPUT LEVELS: $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$
TIME MEASUREMENTS ARE TAKEN AT 50% POINT ($V_{DD}/2$)

Fig. 3 - Timing diagram for GP301 and GP302 ROMs.

Advance Information/
Preliminary Data

GP501A/1RZ

High-Reliability, Radiation-Hardened Emulating Controller

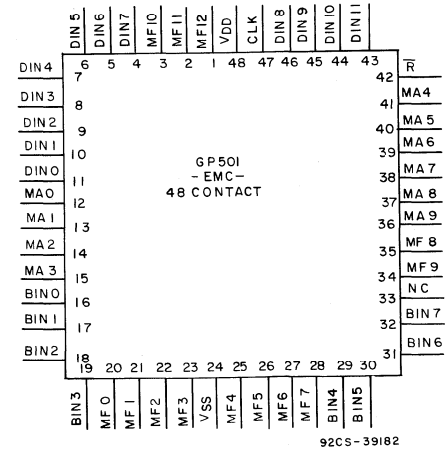
Aerospace Class S Screening

Features:

- *Provides efficient implementation of computer control section combining high speed and efficient micromemory use*
- *13-bit command word*
- *10-bit address generator*
- *Storage registers for bus registers and masks*
- *Full military temperature range operation*
- *40-mil center hermetic leadless package for high packing density*

Radiation Features:

- *Radiation hardened to 100K rads (Si)*
- *Latch-up free under transient radiation*
- *Resistance to upset under transient radiation rate of up to 1 x 10^{10} rads (Si)/sec*



TERMINAL ASSIGNMENT
For J Package
(48-Contact, Leadless Chip Carrier)

The RCA-GP501A/1RZ is an emulating microcontroller (EMC) that has been designed to efficiently implement the entire control section of a computer (when micromemory is added). The EMC has capabilities to support multiple controller configurations, thus increasing speed and memory efficiency.

The GP501A/1RZ is available in a 48-contact leadless chip carrier (J suffix). It may also be supplied in a 64-lead ceramic flat package.

Architecture of the GP501A/1RZ

An extensive set of masking and data manipulation functions exist to provide for various combinations of external inputs to be mapped to the microaddress being generated. These types of functions are required to extract specific operation fields within macroinstructions, suboperation codes, and various combinations of status information.

EMC operations are determined by the microfield and synchronized by the clock. The EMC, shown in Fig. 1, receives data from the bus input and the discrete I/O interface and generates a micromemory address output and certain discrete outputs.

The four stack registers (SR3-SR0) allow linkages between various microsubroutines. The currently active stack register points to the next micromemory location to be executed. The EMC can go to a microsubroutine by pushing the stack and return from a subroutine by popping the stack. If too many levels of subroutine are called, the stack wraps around and the oldest stack register is overwritten with the new stack value. A two-bit Stack Pointer (SP) keeps track of which SR is the currently used register.

The five operations Registers (R4-R0) are dedicated to specific functions such as masking or saving common re-entry points. R0 and R1 are pointers to re-entry points that can be given control directly or conditionally. R2 is a pair of 4-bit mapping registers that can be used to transfer execution to one of 16 micromemory locations depending on other conditions. R3 is a maskable address register that can be loaded from microcode or from the external bus. R4 is an address masking register.

The controller contains a dual timer. This timer is a pair of 16-bit counters that can be set up as inner and outer loop timers. Each timer is set up with a count and a set of branch conditions to be executed when the count runs out. Once started, a counter counts microcycles until terminated, pushed, or finished. The outer loop counter is suspended (pushed) by activation of the inner loop counter. When the inner loop counter runs out, the outer loop counter starts counting on the count at which it was pushed.

The Address Generator is used in determining the next address. The ability exists to mask and Right Justify (RJ) input fields, as needed, by implementing Microcommand 3, the translate command, or Microcommand 2, the map command.

The Control Decode section of the EMC receives microcode input and based upon the bit structure, determines how the next address will be generated. It also determines which discretes and registers to use for the operations. The Control Decode section also indicates the proper stack register and governs the reading and writing of that register. It also starts, stops, resets, and restarts the dual timers.

GP501A/1RZ

An Incrementer receives code from the address generator and, in the normal mode, increments that address for the next microcode instruction. In the two's complement mode it acts as a counter and decrements the count.

The EMC controller has twelve (12) Discrete Inputs that the designer can use to connect various functions from other elements within the architecture that directly effect the flow of microcode. Examples of some of the signals that could be assigned to the discrete inputs are as follows:

- Sign of the ALU output
- Overflow indication
- Carry out
- Indication of all zeros out of ALU
- Completion of shift
- Index register select equals zero
- Completion of load or store multiple
- Multiplier bits for sequential multiply operation
- Changing sign of dividend and sign of division for sequential divide operation
- Interrupts

A four-bit register, loadable by four of the discrete inputs, is provided for machines requiring a Condition Code Register (CCR). The EMC controller is the most efficient location for the CCR when discrete inputs are used for deriving status information. Means are also provided to load and store the contents of the CCR for exchange status requirements.

The Discrete inputs are organized as three (3) groups of four (4) bits each, and the CCR is considered a fourth group.

The discrete interface is shown in Fig. 1. D7-D0 are bidirectional signal pins while D11-D8 are unidirectional inputs having a 4-bit register associated with them. The register bits indicate whether D11-D8 are accepted in true or complement form.

The following comments apply when the controller is used with the bit-slice GPU, GP001. Some features of the EMC facilitate the marriage of the EMC to the GP001, an ALU in the same EPIC series. However, this does not preclude the

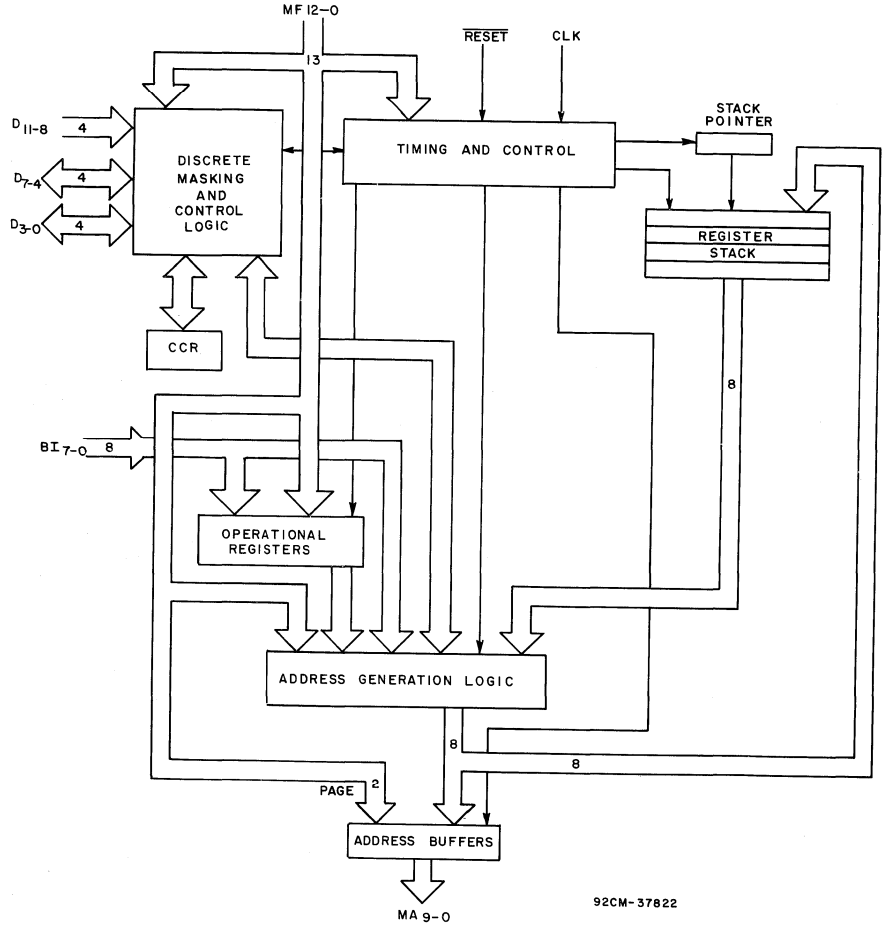


Fig. 1 - Functional block diagram of the GP501.

EMC's efficient use with any other bit-slice ALU.

- The ALU sign and overflow inputs to the controller are time multiplexed to contain the most significant shift input or output when required for the rotate function. Therefore, two pairs of discretes have the ability to pass data in either direction or complete the ALU circular shift macroinstruction.
- The lower four discrete bits (D3-D0) are arranged for connecting the upper and lower shift bits of the GPUs (MXH1-0) and (MXL1-0). Under microcode control D0 connects to D2 and D1 connects to D3, or D2 connects to D0 and D3 connects to D1, or D1 ex-or D0 connects to D2 and D1 connects to D3.

The middle four discrete bits (D7-D4) are primarily used for storing and retrieving status bits. The Condition Code Register (CCR3-CCR0) can be output via D7-D4 or can be loaded via D7-D4. Alternatively, CCR3-CCR0 can be loaded from D11, D10, D1, D0 or D11, D10, D1, D1 XOR D0 or D11, D10, D1 XOR D0, D0.

Fig. 2 shows an application of the GP501 in a typical control section of a computer.

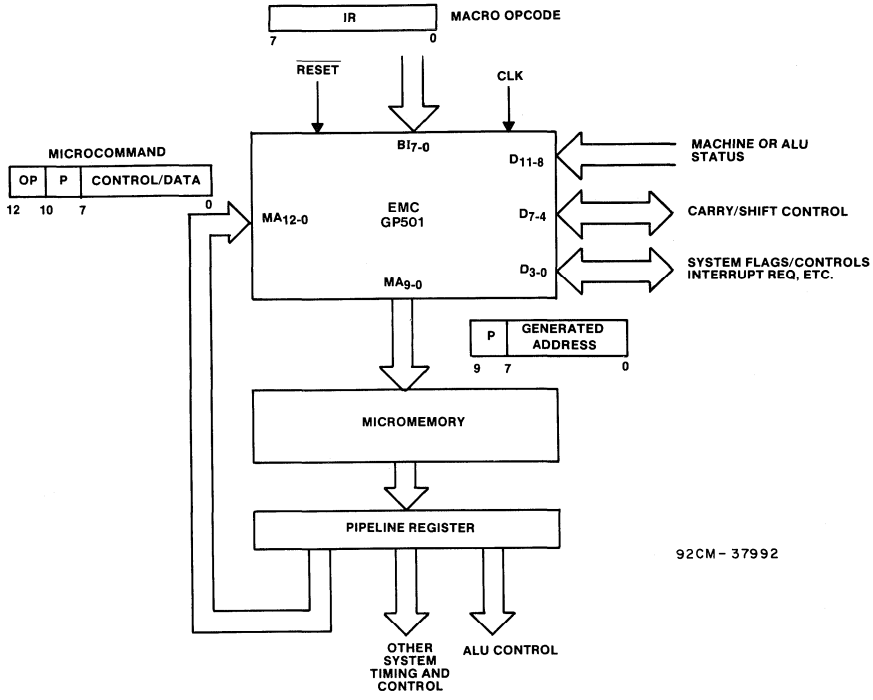


Fig. 2 - Typical application of GP501 in the control section of a computer.

Instruction Set and Operation

The EMC uses eight operation codes to perform various functions (see Table I). The first two codes implement the branch (opcode 0) and branch-and-link (opcode 1) options. Both of these functions are unconditional and, in both cases, the lower 10 bits are the address of the next microinstruction.

However, while the lower 8 bits are solely incremented and loaded into the currently active stack register in opcode 0, in opcode 1, the stack pointer is incremented prior to loading the incremented microcommand into the stack register. The net effect is that the previously active stack register is left pointing to the micromemory location just past the branch-and-link command. Execution continues until a return causes the controller to pick the next address from the previously active stack register.

The control and mask fields in the map command (opcode 2) formulate a new 8-bit address, using some combination of the value present at the bus interface, the value in register R3, or the mapping register R2. This is done according to a table of 16 choices. Immediate mask data is used as a mask for the high nibble of the new address or as a bit-selection map when applied to the low nibble via a right justify function.

The translate command (opcode 3) determines if the currently active stack register is updated or not, using one of 16 control settings. Thus, the new address is combined from the current program counter values at the discrete interface (DI) and/or the content of the CCR. Other control settings apply the masking register R4 or immediate mask values as a bit map using a right justify function.

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The load command (opcode 4) allows the value in the immediate data field to be loaded into one of 16 half registers. The next micromemory address comes from the current stack register and is then incremented.

Two bits, MF5 and MF4, of the conditional discrete setup command (opcode 5) select and examine one of four sets of four signals (the CCR, D8 to 11, D4 to 7 or D0 to 3) from the discrete interface. Bits MF3 to MF0 are a mask that determines which of the selected inputs will be subject to a logical operation (bits MF7 and MF6). If the mask is zero, the current CCR is used as a mask. Bits MF0 to MF7 are all latched for later use. Once the command has set up a discrete operation, the result of the selected logical function is sampled during subsequent operations.

The immediate count instruction (opcode 6) causes the count value to be placed in the holding and masking registers for one of the two counters, and a count of the type specified is initiated. If MF7 is zero, a sequential count begins. Execution continues in normal sequence until the count runs out. At count equals zero, a flag is set and the next instruction is determined by the branch instruction that was set up in the sequential count command.

Table I - The Eight Operation Codes in the 13-Bit Control Word

Command	Control Word MF_{12-0}			Result					Comments
	12-10 Opcode	9-8 Page	7-0 Address, Control, Mask, etc.	Memory Out MA_{9-0}	Stack Register (SR)	Stack Pointer (SP)	Selected Register	Flag	
Unconditional Branch	000	P	Address	P: Address	MA_{7-0} +1	No Change	—	—	—
Unconditional Branch and Link	001	P	Address	P: Address	MA_{7-0} +1	SP + 1	—	—	Currently active SR is not changed.
Map	010	P	Control Mask	P:Formulated Address	MA_{7-0} +1	No Change	—	—	Formulated address from some combination selected by control value of bus in register R2, register R3 and immediate mask.
Translate	011	P	Control Mask	P:Formulated Address	MA_{7-0} +1	No Change	—	—	Formulated address from some combination, selected by control value of current SR value at discrete interface, register R4, immediate mask and CCR. No SR update if C=4-7 and C-F.
Load	100	P	Register Data	P: SR	SR + 1	No Change	Data	—	Active also during Reset.
Conditional Discrete Setup	101	P	E S Mask	P: SR	SR + 1	No Change	—	CD Set	Equation select (E), data source select (S), and mask are recorded. Data source is discrete interface or CCR. Testing via opcode 7.
Immediate Count	110	P	T Branch Count	Branch option selected by branch field	Depends on branch	Depends on branch	—	—	T=0 Sequence T=1 Iterate
Sub-op and Branch	111	P	Branch Sub-op	Branch option selected by branch field	Depends on branch	Depends on branch	—	CD Reset	Sub-op specifies one of several discrete interface operations, counter operations or testing of conditional discrete setups.

In an iterative-type subcommand (MF7-1), the count is also loaded into an available counter. However, the branch condition determined by MF4 to MF7 is taken immediately. The microcode instruction that results from the branch is repeated until the word count runs out, and execution continues sequentially from the repeated microword.

The sub-op and branch command (opcode 7) combines two semi-independent operations. One suboperation specifies a utility function, such as a discrete interface operation or a counter operation. The other is a branch operation that samples a conditional discrete equation, like AND or OR.

Other suboperations include various methods of loading the CCR, while another method features a no-op command. Another sub-op loads register R3 from the bus interface. Meanwhile a different one samples the discrete operation that is set up by opcode 5.

The branch option specifies one of 16 possibilities when no discrete is pending, or one of 32 when coupled with the conditional discrete evaluation feature. Opcode 7 stops sampling the result of opcode 5 execution (the latest discrete operation) and branches according to the branch field in the command. Command 7 allows all microcode sequences emulating a macroinstruction to branch to the fetch routine and load status into the CCR in one single instruction.

For detailed programming information and discussions of instructions, see the following literature:

1. "Emulating Controller (GP501ADL) User's Guide," RCA Solid State Publication, ECG-750.
2. "The GP501-A Flexible and Powerful Microprogram Controller for Emulation in the Control Section of High-Performance Microcomputers," K. Karstad, RCA Solid State Application Note, ICAN-7281.
3. "A Guide to the Emulating Microprogram Controller GP501-With Programming Examples," K. Karstad, RCA Solid State Application Note, ICAN-7259.
4. "A Comparison of EPIC CMOS/SOS Microprogram Controllers GP501 and GP502," K. Karstad, RCA Solid State Application Note, ICAN-7283.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +11 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING FOR D AND K PACKAGE TYPES):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	10.5	V

GP501A/1RZ

PIN FUNCTIONS FOR THE GP501 48-CONTACT LEADLESS CHIP CARRIER

Pin No.	Abbreviation	Name	Function
1	MF12	Input Control Bit	Opcode Bit in Control Word
2	MF11	Input Control Bit	Opcode Bit in Control Word
3	MF10	Input Control Bit	Opcode Bit in Control Word
4	DIN7	Discrete I/O Bit	Used in Conditional Testing and Address Formulation
5	DIN6	Discrete I/O Bit	Used in Conditional Testing and Address Formulation
6	DIN5	Discrete I/O Bit	Used in Conditional Testing and Address Formulation
7	DIN4	Discrete I/O Bit	Used in Conditional Testing and Address Formulation
8	DIN3	Discrete I/O Bit	Used in Conditional Testing and Address Formulation
9	DIN2	Discrete I/O Bit	Used in Conditional Testing and Address Formulation
10	DIN1	Discrete I/O Bit	Used in Conditional Testing and Address Formulation
11	DIN0	Discrete I/O Bit	Used in Conditional Testing and Address Formulation
12	MA0	Memory Address Output	Microprogram Address Bit
13	MA1	Memory Address Output	Microprogram Address Bit
14	MA2	Memory Address Output	Microprogram Address Bit
15	MA3	Memory Address Output	Microprogram Address Bit
16	BIN0	Bus Input Bit	Bit Input for Storage or Address Formulation
17	BIN1	Bus Input Bit	Bit Input for Storage or Address Formulation
18	BIN2	Bus Input Bit	Bit Input for Storage or Address Formulation
19	BIN3	Bus Input Bit	Bit Input for Storage or Address Formulation
20	MF0	Input Control Bit	Control, Data or Address Bit in Control Word
21	MF1	Input Control Bit	Control, Data or Address Bit in Control Word
22	MF2	Input Control Bit	Control, Data or Address Bit in Control Word
23	MF3	Input Control Bit	Control, Data or Address Bit in Control Word
24	V_{SS}	V_{SS}	Minus Supply
25	MF4	Input Control Bit	Control, Data or Address Bit in Control Word
26	MF5	Input Control Bit	Control, Data or Address Bit in Control Word
27	MF6	Input Control Bit	Control, Data or Address Bit in Control Word
28	MF7	Input Control Bit	Control, Data or Address Bit in Control Word
29	BIN4	Bus Input Bit	Bit Input for Storage or Address Formulation
30	BIN5	Bus Input Bit	Bit Input for Storage or Address Formulation
31	BIN6	Bus Input Bit	Bit Input for Storage or Address Formulation
32	BIN7	Bus Input Bit	Bit Input for Storage or Address Formulation
33	N.C.	No Connection	—
34	MF9	Input Control Bit	Page Address Bit in Control Word
35	MF8	Input Control Bit	Page Address Bit in Control Word
36	MA9	Memory Address Output	Microprogram Address Bit
37	MA8	Memory Address Output	Microprogram Address Bit
38	MA7	Memory Address Output	Microprogram Address Bit
39	MA6	Memory Address Output	Microprogram Address Bit
40	MA5	Memory Address Output	Microprogram Address Bit
41	MA4	Memory Address Output	Microprogram Address Bit
42	$\overline{R}$	Reset	Reset Memory Address Output Bits to Zero
43	DIN11	Discrete Input Bit	Used in Conditional Testing and Address Formulation
44	DIN10	Discrete Input Bit	Used in Conditional Testing and Address Formulation
45	DIN9	Discrete Input Bit	Used in Conditional Testing and Address Formulation
46	DIN8	Discrete Input Bit	Used in Conditional Testing and Address Formulation
47	CLK	Clock	For Internal Latching of Data Applied to the MCU
48	V_{DD}	V_{DD}	Plus Supply

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 10 V ± 5%

CHARACTERISTIC		CONDITIONS	LIMITS						UNITS
			-55°C, +25°C		+125°C		Post† Radiation +25°C		
			Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent Device Current	I_{DD}	V_{IN}=0 V or V_{DD}	—	4	—	7	—	7	mA
Operating Device Current	I_{OPR} Note 3	Open Circuit Outputs Cycle Time=200 ns	—	25	—	30	—	30	mA
		Open Circuit Outputs Cycle Time=1000 ns	—	8	—	10	—	10	
Input Leakage Current, Low	I_{IL}	V_{IN}=0, Note 1	—	10	—	20	—	20	μA
Input Leakage Current, High	I_{IH}	V_{IN}=V_{DD}, Note 1	—	10	—	20	—	20	
3-State Output Leakage Current	I_{OZL}	Applied Voltage=0 V, Note 1	—	10	—	20	—	20	
3-State Output Leakage Current	I_{OZH}	Applied Voltage=V_{DD}, Note 1	—	10	—	20	—	20	
Output (Sink) Current	I_{OL}	V_{OUT}=0.5 V	2.5	—	2	—	2	—	mA
Output (Source) Current	I_{OH}	V_{OUT}=V_{DD}-0.5 V	1.5	—	1.4	—	1.4	—	
Output Voltage Low Level	V_{OL}	Note 2	—	0.5	—	0.5	—	0.5	V
Output Voltage High Level	V_{OH}	Note 2	9.5	—	9.5	—	9.5	—	
Input Low Voltage	V_{IL}	V_{OUT}=1 V or 9 V	—	3	—	3	—	3	
Input High Voltage	V_{IH}	V_{OUT}=1 V or 9 V	7	—	7	—	7	—	

†The limits shown are for tests performed within one hour of radiating to 100 K rads (Si).

NOTES:

1. All other inputs (non-measured) are held at opposite logic level.
2. Input levels shall be V_{DD} and V_{SS}. Outputs open.
3. Measured while running the vector set.

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%

CHARACTERISTIC		CONDITIONS	LIMITS						UNITS
			-55°C, +25°C		+125°C		Post† Radiation +25°C		
			Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent Device Current	I_{DD}	V_{IN}=0 V or V_{DD}	—	2	—	3	—	3	mA
Operating Device Current	I_{OPR} Note 3	Open Circuit Outputs Cycle Time=200 ns	—	10	—	12	—	12	mA
		Open Circuit Outputs Cycle Time=1 μs	—	4	—	5	—	5	
Input Leakage Current, Low	I_{IL}	V_{IN}=0, Note 1	—	5	—	10	—	10	μA
Input Leakage Current, High	I_{IH}	V_{IN}=V_{DD}, Note 1	—	5	—	10	—	10	
3-State Output Leakage Current	I_{OZL}	Applied Voltage=0 V, Note 1	—	5	—	10	—	10	
3-State Output Leakage Current	I_{OZH}	Applied Voltage=V_{DD}, Note 1	—	5	—	10	—	10	
Output (Sink) Current	I_{OL}	V_{OUT}=0.4 V	0.9	—	0.7	—	0.7	—	mA
Output (Source) Current	I_{OH}	V_{OUT}=V_{DD}-0.4 V	0.8	—	0.7	—	0.7	—	
Output Voltage Low Level	V_{OL}	Note 2	—	0.5	—	0.5	—	0.5	V
Output Voltage High Level	V_{OH}	Note 2	4.5	—	4.5	—	4.5	—	
Input Low Voltage	V_{IL}	V_{OUT}=0.5 V or 4.5 V	—	1.5	—	1.5	—	1.5	
Input High Voltage	V_{IH}	V_{OUT}=0.5 V or 4.5 V	3.5	—	3.5	—	3.5	—	

†The limits shown are for tests performed within one hour of radiating to 100 K rads (Si).

NOTES:

1. All other inputs (non-measured) are held at opposite logic level.
2. Input levels shall be V_{DD} and V_{SS}. Outputs open.
3. Measured while running the vector set.

GP501A/1RZ

DYNAMIC ELECTRICAL CHARACTERISTIC, V_{DD} = 10 V ± 5%

CHARACTERISTIC*	PROP. DELAY	MAXIMUM LIMITS -55°C +25°C	MAXIMUM LIMITS +125°C	MAXIMUM LIMITS Post† Radiation +25°C	UNITS	Fig.+	Note■
MF(0) → MA		65	80	80		3	
MF(1) → MA		65	80	80		3	
BI(2) → MA		60	75	75		4	1
BI/MF(2) → MA		70	90	90		4	2
BI_{3-0}(2) → MA		50	65	65		5	2
BI_{3-0}/MF(2) → MA		75	95	95		5	
D_{3-0}(3) → MA		35	45	45		6	3
D_{3-0}/MF(3) → MA		65	80	80		7	
MF(3) → MA	t_{PD}	65	80	80	ns	3	4
MF(4) → MA		60	75	75		3	5
MF(5) → MA		60	75	75		3	6
MF(6) → MA		95	120	120		3	7
MF(7) → D_{7-4}		80	100	100		8	8
MF(7) → MA, TRUE		25	30	30		9	9
MF(7) → MA, FALSE		95	120	120		9	10
D0 → D3(7)		25	30	30		10	
$\overline{RESET}$ → MA		50	65	65		11	

†Radiation measurements are made on 2 samples/wafer. The limits shown are for tests performed within one hour of radiating to 100 K rads (Si).

*Number inside bracket refers to opcode being executed.

+Refer to timing diagrams.

■See notes below.

DYNAMIC ELECTRICAL CHARACTERISTIC, V_{DD} = 5 V ± 5%

CHARACTERISTIC*	PROP. DELAY	MAXIMUM LIMITS -55°C +25°C	MAXIMUM LIMITS +125°C	MAXIMUM LIMITS Post† Radiation +25°C	UNITS	Fig.+	Note
MF(0) → MA		120	150	150		3	
MF(1) → MA		120	150	150		3	
BI(2) → MA		100	125	125		4	1
BI/MF(2) → MA		130	160	160		4	
BI_{3-0}(2) → MA		100	125	125		5	2
BI_{3-0}/MF(2) → MA		140	175	175		5	
D_{3-0}(3) → MA		80	100	100		6	3
D_{3-0}/MF(3) → MA		130	160	160		7	
MF(3) → MA	t_{PD}	130	160	160	ns	3	4
MF(4) → MA		130	160	160		3	5
MF(5) → MA		130	160	160		3	6
MF(6) → MA		180	225	225		3	7
MF(7) → D_{7-4}		160	200	200		8	8
MF(7) → MA, TRUE		50	65	65		9	9
MF(7) → MA, FALSE		190	240	240		9	10
D0 → D3(7)		50	70	70		10	
$\overline{RESET}$ → MA		110	140	140		11	

†Radiation measurements are made on 2 samples/wafer. The limits shown are for tests performed within one hour of radiating to 100 K rads (Si).

*Number inside bracket refers to opcode being executed.

+Refer to timing diagrams.

NOTES:

1. Opcode 2 is set up earlier.
2. Opcode 2 is set up earlier. $R2_{3-0}$ is preloaded.
3. Opcode 3 is set up earlier.
4. Preload CCR and $R4_{7-4}$.
5. Load Outer Counter Holding Register.
6. Conditional Discrete Flag is set.
7. Iterative count. Return branch option.
8. Preload CCR.
9. Discrete pending is true.
10. Discrete pending is false.

Timing Diagrams for Various Propagation Delay Paths

Figure numbers are referred to in the Dynamic Electrical Characteristics charts

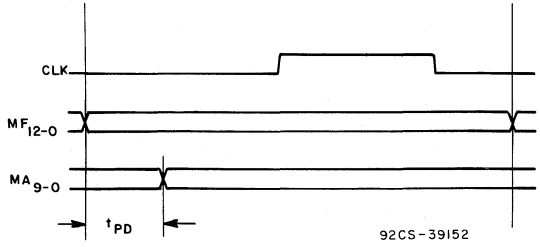


Fig. 3

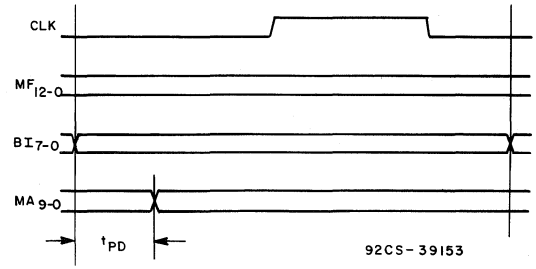


Fig. 4

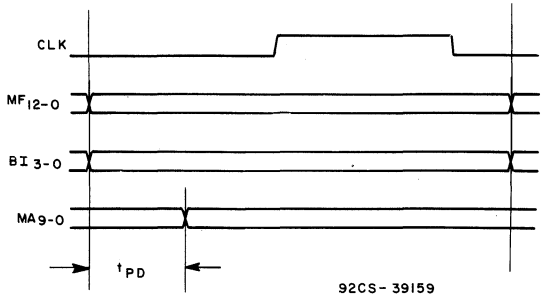


Fig. 5

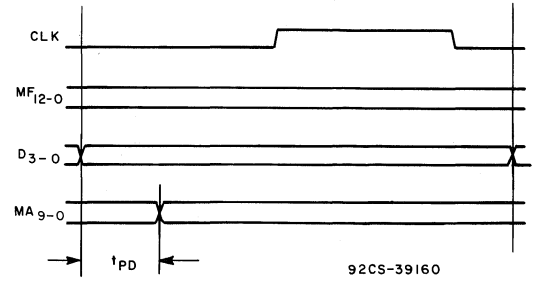


Fig. 6

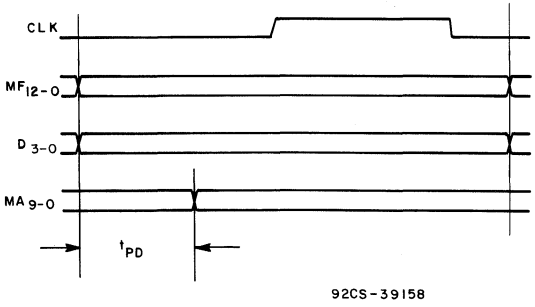


Fig. 7

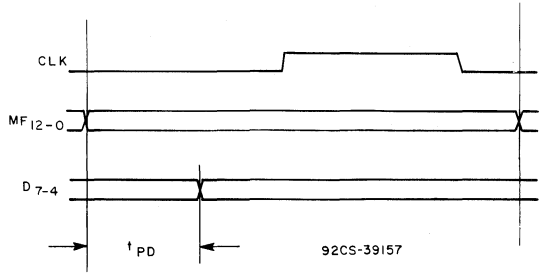


Fig. 8

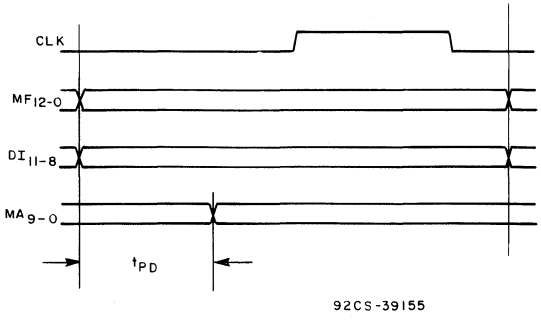


Fig. 9

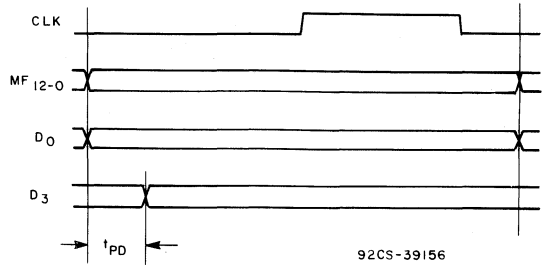


Fig. 10

GP501A/1RZ

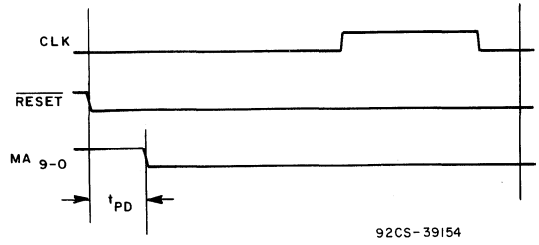


Fig. 11

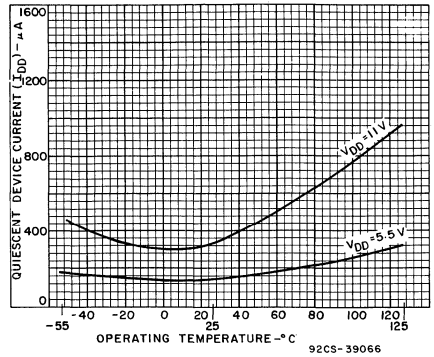


Fig. 12 - Typical quiescent device current as a function of operating temperature.

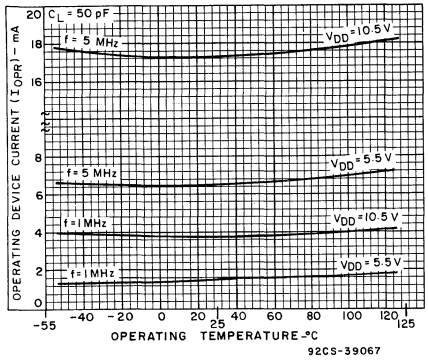


Fig. 13 - Typical operating device current as a function of operating temperature.

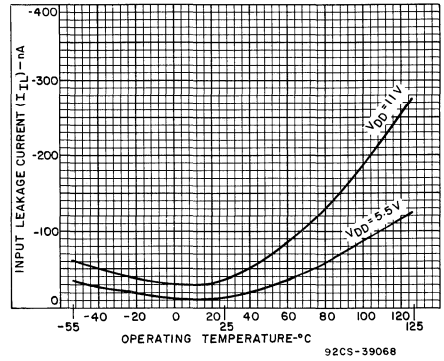


Fig. 14 - Typical input leakage current as a function of operating temperature.

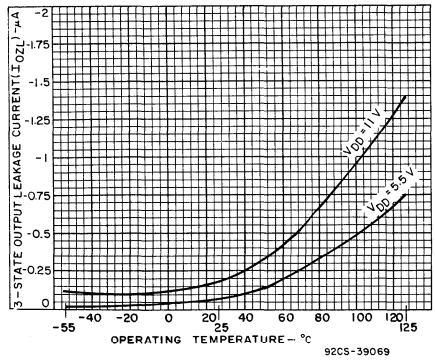


Fig. 15 - Typical 3-state output leakage current as a function of operating temperature.

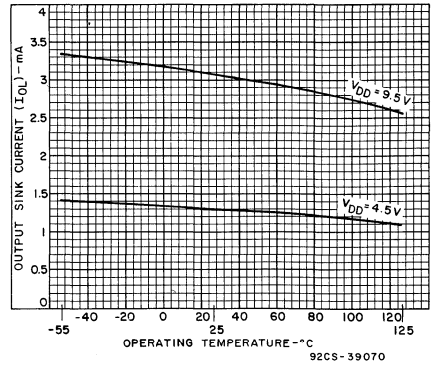


Fig. 16 - Typical output sink current as a function of operating temperature.

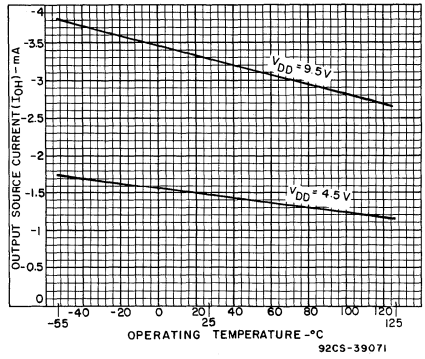


Fig. 17 - Typical output source current as a function of operating temperature.

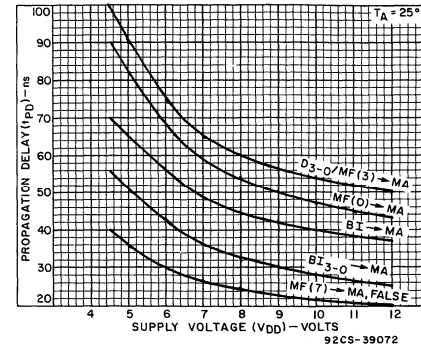


Fig. 18 - Typical propagation delay as a function of supply voltage.

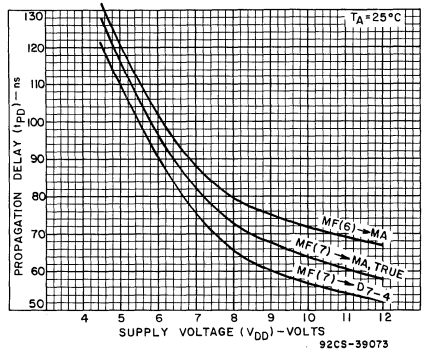


Fig. 19 - Typical propagation delay as a function of supply voltage.

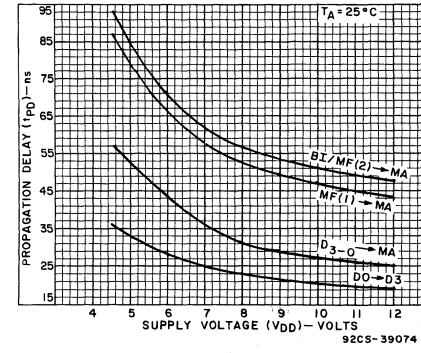


Fig. 20 - Typical propagation delay as a function of supply voltage.

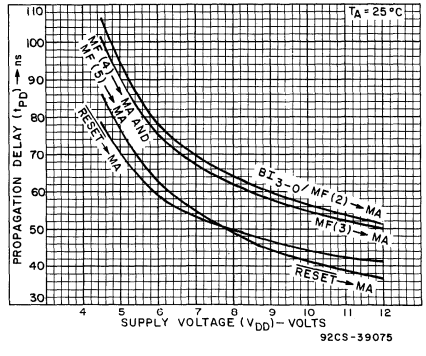


Fig. 21 - Typical propagation delay as a function of supply voltage.

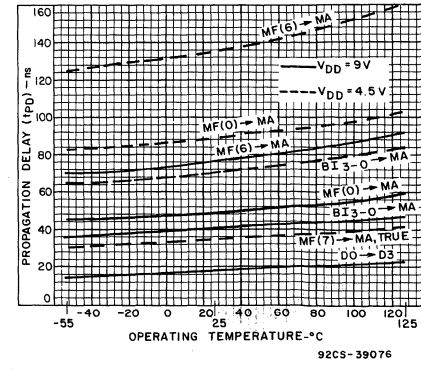


Fig. 22 - Typical propagation delay as a function of operating temperature.

GP501A/1RZ

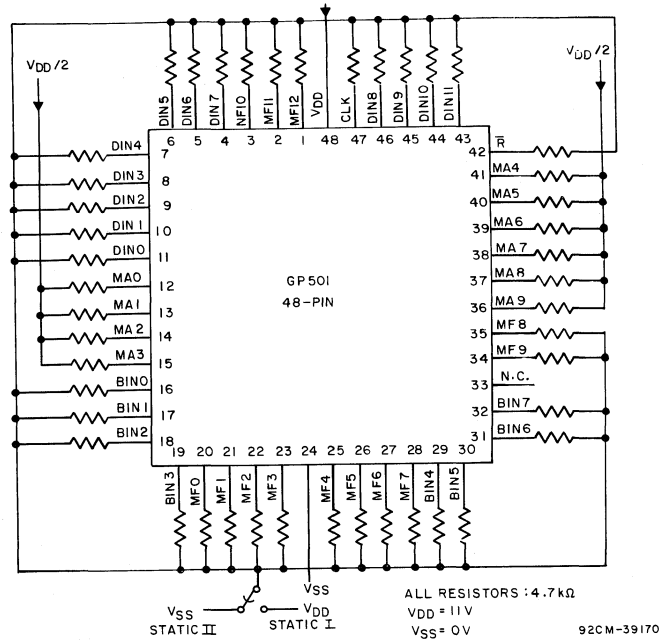


Fig. 23 - Static burn-in circuit for the GP501 48-contact leadless chip carrier.

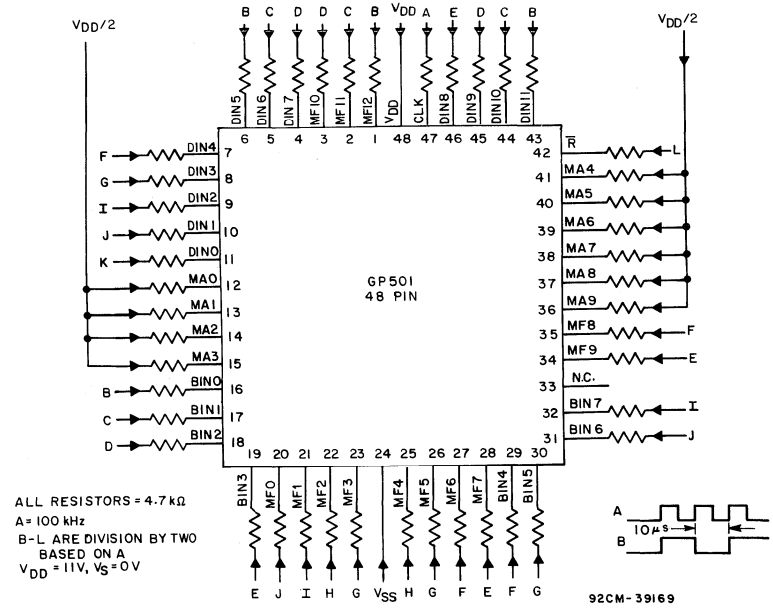


Fig. 24 - Dynamic burn-in circuit for the GP501 48-contact leadless chip carrier.

Advance Information/
Preliminary Data

GP502/1RZ

High-Reliability, Radiation-Hardened Microprogram Sequencer "2910"

Features:

- *CMOS/SOS circuitry for low power and high speed*
- *Fully static operation to 10 MHz*
- *No minimum clock is required*
- *Single power supply*
- *High noise immunity*
- *Full military temperature range operation*
- *40-mil center hermetic leadless package for high packing density*
- *Typical 10-V operation*
- *Tri-state outputs*
- *12 bits wide - 4096 words of N code*
- *Internal 12-bit loop counter for repeating instructions and counting loop iterations*
- *16 powerful microinstructions*
- *Radiation hardened to 100K Rads-(Si)*

The CMOS/SOS GP502 is a 12-bit microprogram sequencer, which provides flexible control typically required in emulation architectures. This device is pin-for-pin (DIC) and functionally compatible with the commerical bipolar AM2910 microprogram sequencer. It is designed to control the stepping through target machine microprograms. In addition it provides conditional branching to any microinstruction within its 4096-microword range.

During each microinstruction, a 12-bit address can be selected by the 16 basic commands from one of the four microprogram address sources. These sources are:

1. μP address register for sequencial operation,
2. Direct input for absolute branching,
3. Contents of register/counter for mapping functions,
4. Top of LIFO (Last-In-First Out) stack for return linkage in microsubroutines.

The 12-bit register/counter (R/C) is controlled by the RLD signal. When RLD is low, the new data is being loaded. The output of R/C is fed to the multiplexer where it becomes available as a source for the next microinstruction address.

Another source of 12-bit address is a microprogram counter (μPC) which includes the 12-bit incrementer and a 12-bit register. The operation depends on the carry-in state. When carry-in is high, the microprogram register is loaded on the next clock cycle with the current microprogram address (Y-outputs) plus one (Y+1). This results in sequencial execution. When the carry-in is low, the microprogram address (Y-out) is passed on to μPC unmodified on the next clock cycle. This means that the same microinstruction may be executed any number of times.

One of the sources available at the multiplexer is a 5-word by 12-bit stack with a built-in stack pointer, which addresses the value presently on the top of the stack. Any time the stack is full, the FULL warning out occurs.

GP502/1RZ

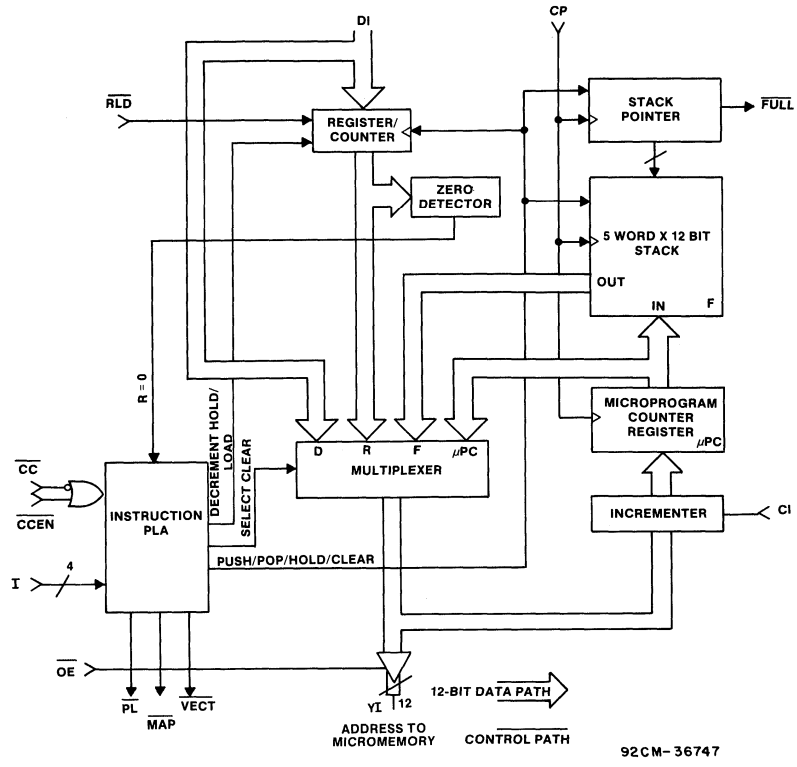


Fig. 1 - Block diagram of CMOS/SOS microprogram sequencer.

PIN ASSIGNMENTS FOR LEADLESS 48-CONTACT PACKAGE

PIN #	I/O	SIGNAL NAME
1	O	Y4
2	I	D4
3	O	Y5
4	I	D5
5	O	$\overline{VECT}$
6	O	$\overline{PL}$
7	O	$\overline{MAP}$
8	I	I3
9	—	—
10	I	I2
11	—	—
12	POS. POT	V_{DD}
13	I	I1
14	—	—
15	I	I0
16	—	—
17	I	$\overline{CCEN}$
18	I	$\overline{CC}$
19	I	$\overline{RLD}$
20	—	—
21	O	$\overline{FULL}$
22	I	D6
23	O	Y6
24	I	D7

PIN #	I/O	SIGNAL NAME
25	O	Y7
26	I	D8
27	O	Y8
28	I	D9
29	O	Y9
30	I	D10
31	O	Y10
32	I	D11
33	O	Y11
34	I	$\overline{OE}$
35	NEG. POT.	V_{SS}
36	I	CP
37	—	—
38	I	CI
39	O	Y0
40	I	D0
41	O	Y1
42	I	D1
43	—	—
44	—	—
45	O	Y2
46	I	D2
47	O	Y3
48	I	D3

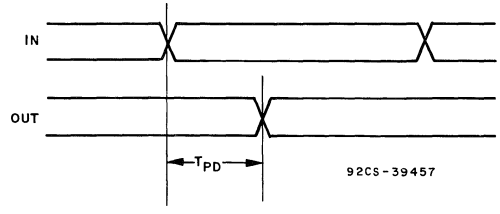
STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			LIMITS								UNITS
				-55°C		+25°C		+125°C		+25°C POST RADIATION		
	V_{DD} (V)	V_{IN} (V)	V_{OUT} (V)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{DD} Quiescent	5	5, 0	—	—	200	—	200	—	500	—	500	μA
	10	10, 0	—	—	500	—	500	—	1000	—	1000	
Input Leakage	5	5, 0	—	—	5	—	5	—	10	—	10	μA
I_{IH}/I_{IL}	10	10, 0	—	—	10	—	10	—	20	—	20	
Tri-state Leakage	5	5, 0	5, 0	—	8	—	8	—	15	—	15	μA
I_{OZH}/I_{OZL}	10	10, 0	10, 0	—	15	—	15	—	30	—	30	
I_{DN}	5	5, 0	0.4	0.6	—	0.5	—	0.36	—	0.36	—	mA
	10	10, 0	0.5	1.9	—	1.5	—	1.1	—	1.1	—	
I_{DP}	5	5, 0	4.6	0.6	—	0.5	—	0.36	—	0.36	—	mA
	10	10, 0	9.5	1.9	—	1.0	—	0.72	—	0.72	—	

DYNAMIC ELECTRICAL CHARACTERISTICS

Input t_r, t_f = 20 ns, C_L = 50 pF, V_{DD} = ± 5%

CHARACTERISTIC	TEST CONDITIONS			LIMITS								UNITS
				-55°C		+25°C		+125°C		+25°C POST RADIATION		
	V_{DD} (V)	V_{IN} (V)	V_{OUT} (V)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dynamic I_{DD}	5	5, 0	—	—	1.0	—	1.0	—	1.2	—	1.2	mA
1.0 MHz	10	10, 0	—	—	2.0		2.0	—	2.5	—	2.5	
Dynamic I_{DD}	5	5, 0	—	—	5.0	—	5.0	—	6.0	—	6.0	mA
5.0 MHz	10	10, 0	—	—	10.0	—	10.0	—	12.0	—	12.0	
T_{PD}	5	V_{IH},	—	—	220	—	220	—	300	—	300	ns
Prop Delay Time	10	V_{IL}	—	—	110	—	110	—	180	—	180	



NOTE: INPUT LEVELS: $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$.
TIME MEASUREMENT IS TAKEN AT 50% POINT ($V_{DD}/2$)

Fig. 2 - Timing diagram.

GP502/1RZ

SIGNAL CLASSIFICATION

NAME	FUNCTION
1. Input Address (D11-D0)	Direct input to R/C and Multiplexer
2. Instruction Bits (I3-I0)	Selects one-of-sixteen instructions for the microprogram sequencer.
3. Carry-In (CI)	Input to Increment for μPC
4. Condition Code ($\overline{CC}$)	Used as test criterion
5. Condition Code Enable ($\overline{CCEN}$)	It enables $\overline{CC}$ signal
6. Register Load ($\overline{RLD}$)	Controls loading of Register/Counter
7. Clock Pulse (CP)	Triggers Register/Counter
8. Output Enable ($\overline{OE}$)	Controls the tri-state outputs of the 12 microprogram address bits (Y11-Y0)
OUTPUTS	
1. Microprogram Address Bits (Y11-Y0)	Address to microprogram memory Y0 = least significant bit, Y11 = most significant bit
2. Map Address Enable ($\overline{MAP}$)	Usually selects Mapping ROM or PLA as direct input source.
3. Pipeline Address Enable ($\overline{PL}$)	Usually selects Pipeline Register as direct input source.
4. Vector Address Enable ($\overline{VECT}$)	Usually selects interrupt Starting Address as direct input source.
5. Full Stack ($\overline{FULL}$)	Indicates that five items are on the stack.

INSTRUCTIONS

I-STATE I3-I0	MNEMONIC	DESCRIPTION
0	JZ	**Jump and Zero,** or Reset
1	CJS	**Conditional Jump-to-Subroutine** via the address provided in the pipeline register.
2	JMAP	**Jump MAP.** This is an unconditional instruction that causes MAP output to be enabled.
3	CJP	**Conditional Jump Pipeline.** Provides a technique for branching.
4	PUSH	**Push/Conditional Load Counter.** It is used primarily for setting up loops in microprogram firmwave.
5	JSRP	**Conditional Jump-to-Subroutine** via the Register/Counter or the contents of the pipeline register.
6	CJV	**Conditional Jump Vector.** This instruction provides one technique for performing interrupt type branching at the microprogram level.
7	JRP	**Conditional Jump** via the contents of Register/Counter or the contents of the pipeline register.
8	RLCT	**Repeat Loop, Counter ≠ Zero.** This instruction makes use of the decrementing capability of the Register/Counter.
9	RPCT	**Repeat Pipeline Register, Counter ≠ Zero.** Similar to instruction #8 except that the branch address comes from the pipeline register rather than the file.
10	CRTN	**Conditional Return-from-Subroutine.** This instruction is used to branch from the subroutine back to the next microinstruction address following the subroutine call.
11	CJPP	**Conditional Jump Pipeline** register address and POP stack. This instruction provides another technique for loop termination and stack maintenance.
12	LDCT	**Load Counter and Continue.** Enables the counter to be loaded with the value at its parallel inputs.
13	LOOP	**Test End-of-Loop.** Provides the capability of conditionally exiting a loop.
14	CONT	**Continue.** Causes the microprogram counter to increment.
15	TWB	**Three-Way Branch.** This instruction provides for testing both a data-depending condition and the counter during one microinstruction and provides for selecting one of the three microinstruction addresses as the next microinstruction to be performed.

GP503/1RZ

Advance Information/
Preliminary Data

High-Reliability, Radiation-Hardened 8-Bit by 8-Bit Multiplier

Features:
- *CMOS/SOS circuitry for low power drain and high speed*
- *Fully static operation*
- *No minimum clock-speed is required*
- *Single power supply*
- *High noise immunity*
- *Full military temperature-range operation*
- *40-mil center hermetic leadless package for high packaging density*
- *Typical 10-V operation*
- *8-bit by 8-bit multiplication requiring no additional logic*
- *Expandable to greater bit lengths*
- *Completely asynchronous operation*
- *Input operands may be latched*
- *Typical multiply time: 150 ns for 8 bits at 10 V*
- *Radiation hardened to 100k rads (Si)*

The RCA GP503/1RZ module is an asynchronous 8-bit by 8-bit expandable 2's complement multiplier that may be used in applications where high-speed, low-power digital multiplication is required. Expansion features make it possible to design a multiplier for operands of almost any bit length by using more than one GP503/1RZ device.

The GP503/1RZ is a CMOS/SOS integrated circuit that is usable in a wide variety of logic configurations in aerospace, military, and precision industrial equipment.

The input/output signals of this device can be classified by function as: data (a,b,A,B,CI,c,CO), controls (La, Lb, M1, M2, EN1, EN2) and power (V_{DD}, V_{SS}).

The two 8-bit operands (multiplicands and multipliers) are applied to pins bin, b0, b1 through b7 and ain, a0, a1 through a7, respectively, and their product (c=a·b) appears as outputs c0, c1 through c15. A third 8-bit word may be applied to expansion inputs B0, B1 through B7 to implement the arithmetic function c=a·b+B.

When the input latch control signals (La, Lb) are at a high level, the respective input data is latched and will remain stable until a negative transition of the latch control occurs, at which time new data may be introduced.

Four carry-in signals (CI1, CI2 through CI4) and four carry-out signals (CO1, CO2 through CO4) are provided to link GP503/1RZ's with each other in an array.

There are 4 modes of operation for the GP503/1RZ multiplier. Mode is determined by mode control bits M1 and M2.

When mode control bits M1 and M2 are low, the GP503/1RZ will operate in the Solo Slice mode in which the adders act as a 9th-bit extension of the 8-bit adders. The carry-in signals are internally generated and the CI pins must be electrically free to float. The value of c15 appears on the CO4/c15 pin. The ain and bin are both set to zero. The carry-out signals CO are used to provide sign extension by connecting CO1 to A1 and A2, CO2 to A3 and A4 and CO3 to A5 and A6.

In the Most Significant Slice mode, mode control M1=High and M2=Low. This mode is the same as the Solo Slice mode except that the carry-in input values CI are used as the carry-in values to the four adder stages. The value of c15 appears on the CO4/c15 pin. Inputs ain and bin are tied to the most significant bit inputs (a7 and b7, respectively, of the next less significant multiplier in an array).

Mode control setting M1=Low and M2=High places the GP503/1RZ into the Least Significant Slice mode. In this mode the adders are transparent, leaving each adder stage as an 8-bit adder. The carry-in signals are internally generated. The value of CO4 appears on the CO4/c15 pin. Inputs ain and bin are both set to zero. Inputs A0, A1 through A6 are connected to output pins c0, c1 through c6 of the next more significant multiplier in an array. If mode controls M1=High and M2=High, the multiplier will be in the Middle Slice mode. This mode is the same as the Least Significant Slice mode, except for carry-in signals which are used as the carry-in values to the adder stages. Inputs ain and bin are connected in the same way as in the Most Significant Slice mode.

EN1 and EN2 signals control the state of the output drivers independently or are gated with M1 and M2, respectively. Output drivers c0, c1 through c6 are enabled when EN1=High or when M1=High. Output pin CO4/c15 will be c15 value when M2=Low and EN2=High. When M2=High, CO4 value will appear at CO4/c15 output pin independently of EN2 value. If EN2=High, output drivers c8, c9 through c14 are enabled.

GP503/1RZ multipliers can be used as functional multipliers in three ways: solo (8-bit by 8-bit), concatenation (8n-bit by 8-bit), and cascading and concatenation (8n-bit by 8m-bit). By concatenating a number of GP503/1RZ multipliers, the length of the multiplicand (b-operand) can be increased in increments of 8 bits, thus implementing 16-bit by 8-bit multiplication, 24-bit by 8-bit multiplication, and so on. Concatenated arrays of GP503/1RZ multipliers can be combined by cascading, which increases the length of the multiplier (a-operands) in increments of 8 bits.

A 16-bit by 16-bit multiplier can be constructed by cascading two 16-bit by 8-bit multiplier arrays each consisting of two concatenated GP503/1RZ multipliers.

The GP503/1RZ is supplied in a 64-pin hermetic leadless package (J suffix).

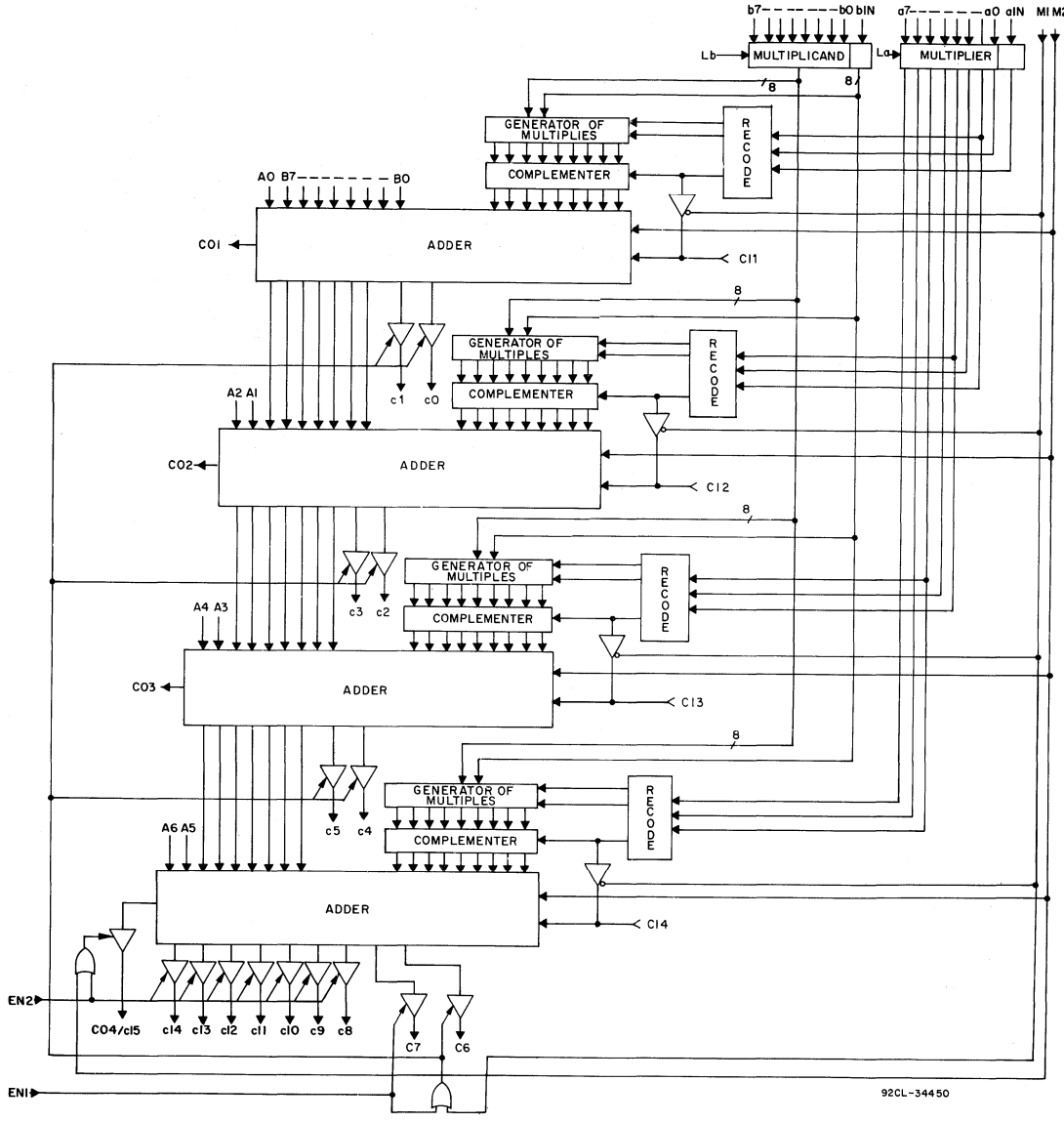


Fig. 1 - GP503/1RZ 8-bit by 8-bit multiplier.

GP503/1RZ

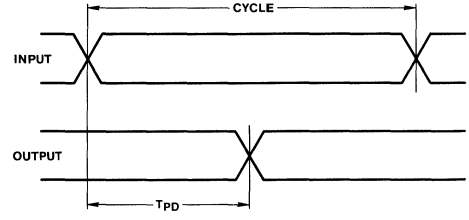
STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			LIMITS								UNITS
				-55°C		+25°C		+125°C		+25°C Post Radiation		
	V_{DD} (V)	V_I (V)	V_O (V)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent Device Current, I_{DD}	5	5, 0		—	500	—	500	—	1000	—	1000	μA
	10	10, 0		—	1000	—	1000	—	2000	—	2000	
Input Leakage Current, I_{IH}/I_{IL}	5	5, 0		—	5	—	5	—	10	—	10	
	10	10, 0		—	10	—	10	—	20	—	20	
Tri-State Output Leakage Current, I_{OZH}/I_{OZL}	5	5, 0	5, 0	—	8	—	8	—	—	—	—	
	10	10, 0	0, 0	—	15	—	15	—	—	—	—	
Output Drive Current (Sink), I_{DN1}	5	5, 0	0.4	0.6	—	0.5	—	0.36	—	0.36	—	mA
	10	10, 0	0.5	1.4	—	1.1	—	0.79	—	0.79	—	
Output Drive Current (Source), I_{DP1}	5	5, 0	4.6	0.6	—	0.5	—	0.36	—	0.36	—	
	10	10, 0	9.5	1.4	—	1.1	—	0.79	—	0.79	—	
Output Drive Current (Sink), I_{DN2}	5	5, 0	0.4	0.12	—	0.1	—	0.08	—	0.08	—	
	10	10, 0	0.5	0.19	—	0.15	—	0.11	—	0.11	—	
Output Drive Current (Source), I_{DP2}	5	5, 0	4.6	0.12	—	0.1	—	0.08	—	0.08	—	
	10	10, 0	9.5	0.19	—	0.15	—	0.11	—	0.11	—	

DYNAMIC ELECTRICAL CHARACTERISTICS

Input t_r,t_f = 20 ns, C_L = 50 pF, V_{DD} = ±5%

CHARACTERISTIC	TEST CONDITIONS			LIMITS								UNITS
				-55°C		+25°C		+125°C		+25°C Post Radiation		
	V_{DD} (V)	V_I (V)	V_O (V)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dynamic I_{DD}, 1 MHz	5	5, 0		—	—	—	2.5	—	3	—	3	mA
	10	10, 0		—	—	—	5	—	6	—	6	
Dynamic I_{DD}, 5 MHz	5	5, 0		—	—	—	12	—	14	—	14	
	10	10, 0		—	—	—	25	—	30	—	30	
Propagation Delay Time, T_{PD}	5	V_{IH},		—	300	—	300	—	420	—	420	ns
	10	V_{IL}		—	160	—	160	—	220	—	220	



NOTE:
INPUT LEVELS: $V_{IH} = V_{DD}$; $V_{IL} = V_{SS}$.
TIMING MEASUREMENTS ARE TAKEN AT 50% POINT ($V_{DD}/2$).

92CS-39507

Fig. 2 - Timing diagram.

GP503/1RZ

Pin/Signal Assignment

Pin No.	Mnemonic	I/O	Description
1	CO2	O	Carry out bit 2
2	A3	I	Bit 3 of A expansion inputs
3	A4	I	Bit 4 of A expansion inputs
4	a4	I	Bit 4 of multiplier inputs
5	a5	I	Bit 5 of multiplier inputs
6	CO3	O	Carry out bit 3
7	A5	I	Bit 5 of A expansion inputs
8	A6	I	MSB of A expansion inputs
9	a6	I	Bit 6 of multiplier inputs
10	a7	I	MSB of multiplier inputs
11	V_{SS}	—	Negative end of power supply
12	La	I	Multiplier input latch control
13	CO4/c15	O	Carry out Bit 4/MSB of product output
14	M2	I	Mode control 2 product output
15	EN2	I	Enable/disable control 2 product output
16	c14	O	Bit 14 product output
17	c13	O	Bit 13 product output
18	c12	O	Bit 12 product output
19	c11	O	Bit 11 product output
20	c10	O	Bit 10 product output
21	c9	O	Bit 9 product output
22	c8	O	Bit 8 product output
23	EN1	I	Enable/disable control 1
24	M1	I	Mode control 1
25	CI4	I	Carry input bit 4
26	c7	O	Bit 7 product output
27	c6	O	Bit 6 product output
28	CI3	I	Carry input bit 3
29	c5	O	Bit 5 product output
30	c4	O	Bit 4 product output
31	CI2	I	Carry input bit 2
32	c3	O	Bit 3 product output
33	c2	O	Bit 2 product output
34	CI1	I	Carry input bit 1
35	c1	O	Bit 1 product output
36	c0	O	LSB product output
37	V_{DD}	—	Positive end of P.S.
38	bin	I	Expansion input for multiplicand
39	B0	I	LSB of B expansion inputs
40	b0	I	LSB of multiplicand inputs
41	B1	I	Bit 1 of B expansion inputs
42	b1	I	Bit 1 of multiplicand inputs
43	B2	I	Bit 2 of B expansion inputs
44	b2	I	Bit 2 of multiplicand inputs
45	B3	I	Bit 3 of B expansion inputs
46	b3	I	Bit 3 of multiplicand inputs
47	B4	I	Bit 4 of B expansion inputs
48	b4	I	Bit 4 of multiplicand inputs
49	B5	I	Bit 5 of B expansion inputs
50	b5	I	Bit 5 of multiplicand inputs
51	B6	I	Bit 6 of B expansion inputs
52	b6	I	Bit 6 of multiplicand inputs
53	B7	I	MSB of B expansion inputs
54	b7	I	MSB of multiplicand inputs
55	Lb	I	Multiplicand input latch control
56	ain	I	Expansion input for multiplier
57	A0	I	LSB of A expansion input
58	a0	I	LSB of multiplier inputs
59	a1	I	Bit 1 of multiplier inputs
60	CO1	O	Carry output bit 1
61	A1	I	Bit 1 of A expansion inputs
62	A2	I	Bit 2 of A expansion inputs
63	a2	I	Bit 2 of multiplier inputs
64	a3	I	Bit 3 of multiplier inputs

GP503/1RZ

EFFECTS OF THE MODE BITS, M

M1	M2	GP503 MODE	CARRY-IN SIGNALS	9TH BIT SLICE OF ADDER	CO4/c15
L	L	SOLO	INTERNAL	ACTIVE	EN2 = L: HIGH Z EN2 = H: c15
L	H	LEAST SIGNIFICANT SLICE	INTERNAL	TRANSPARENT	CO4
H	L	MOST SIGNIFICANT SLICE	CI_I	ACTIVE	EN2 = L: HIGH Z EN2 = H: c15
H	H	MIDDLE SLICE	CI_I	TRANSPARENT	CO4

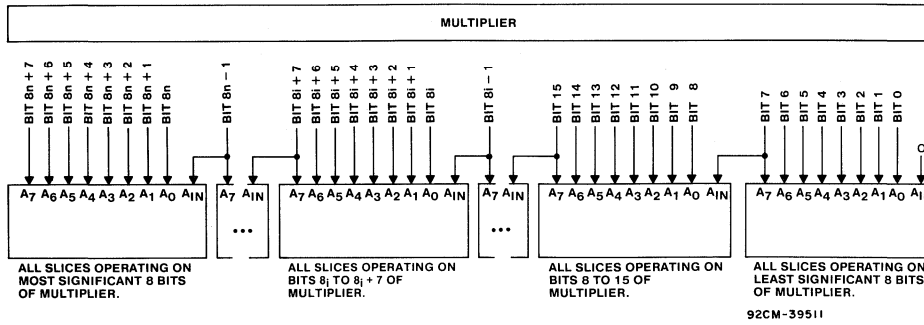


Fig. 3 - Connections of the Data Input pins a_7, a_6, . . ., a_0, a_{IN}.

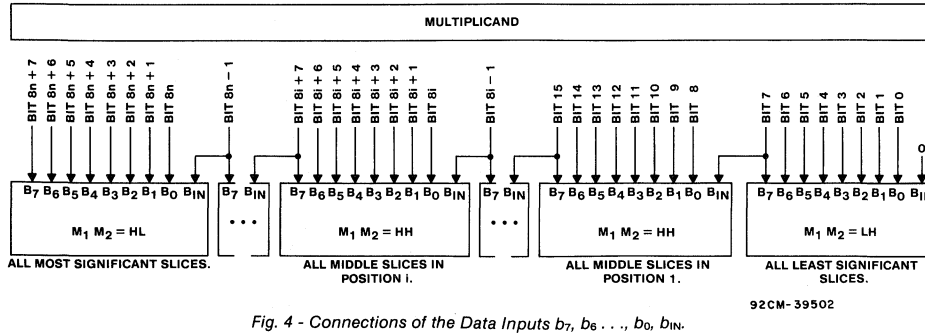


Fig. 4 - Connections of the Data Inputs b_7, b_6 . . ., b_0, b_{IN}.

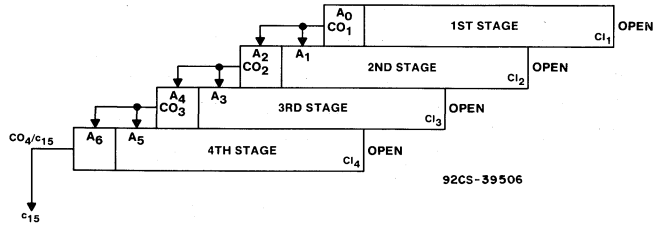


Fig. 5 - Carry-in and Carry-out connections in a solo 8-bit by 8-bit multiplier.

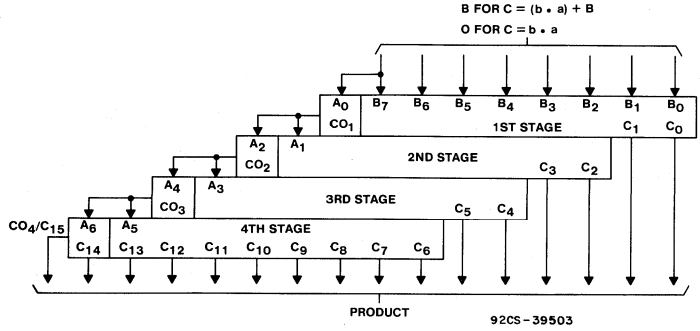


Fig. 6 - Connection of A, B and c pins in a solo 8-bit by 8-bit multiplier.

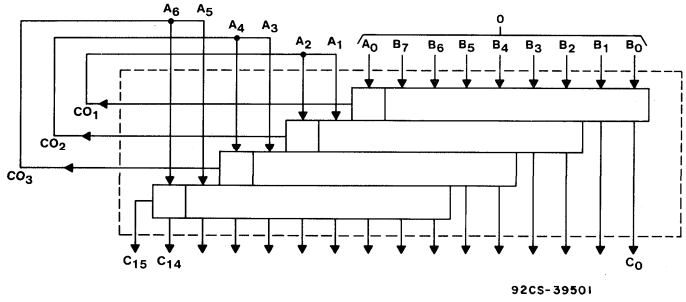


Fig. 7 - GP503 as a solo 8-bit by 8-bit multiplier.

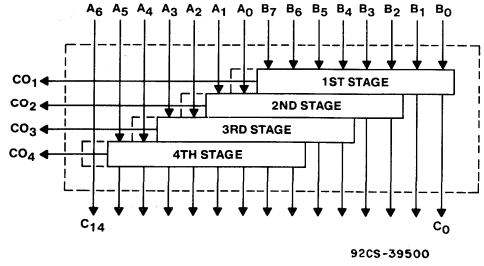


Fig. 8 - GP503 multiplier in "least significant slice" mode (M_1M_2=LH).

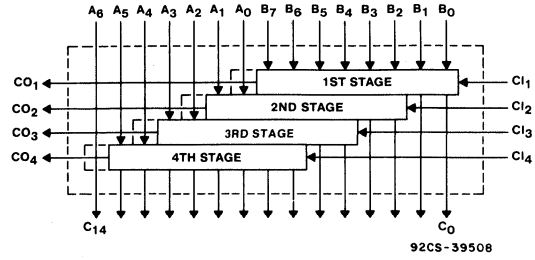


Fig. 9 - GP503 multiplier in "middle slice" mode (M_1M_2=HH).

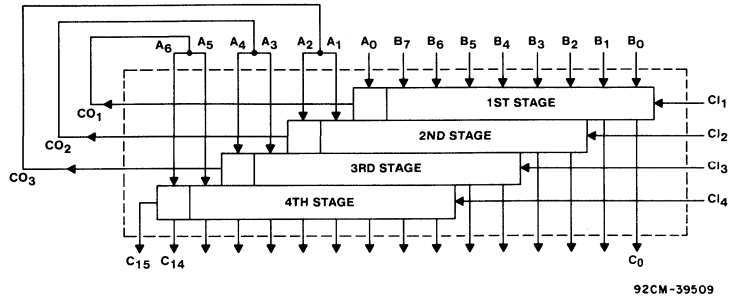


Fig. 10 - GP503 multiplier in "most significant slice" mode (M_1M_2=HL).

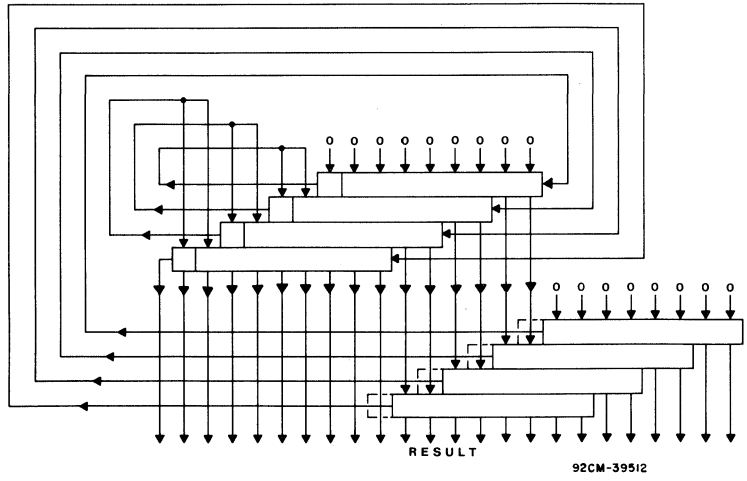


Fig. 11 - Array of two concatenated GP503 multipliers forming a 16-bit by 8-bit multiplier.

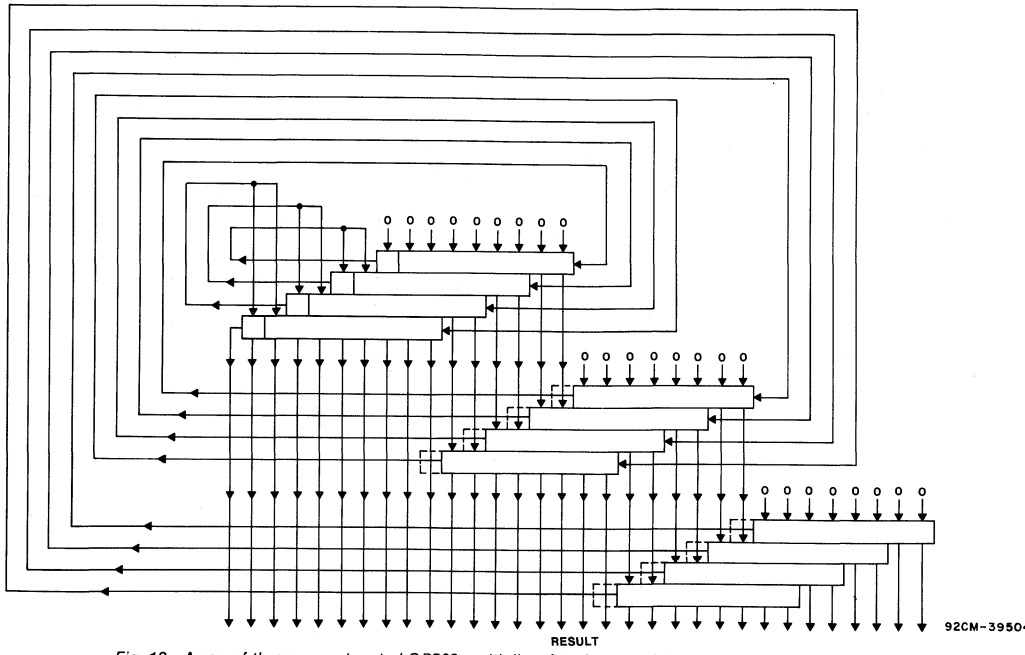


Fig. 12 - Array of three concatenated GP503 multipliers forming a 24-bit by 8-bit multiplier.

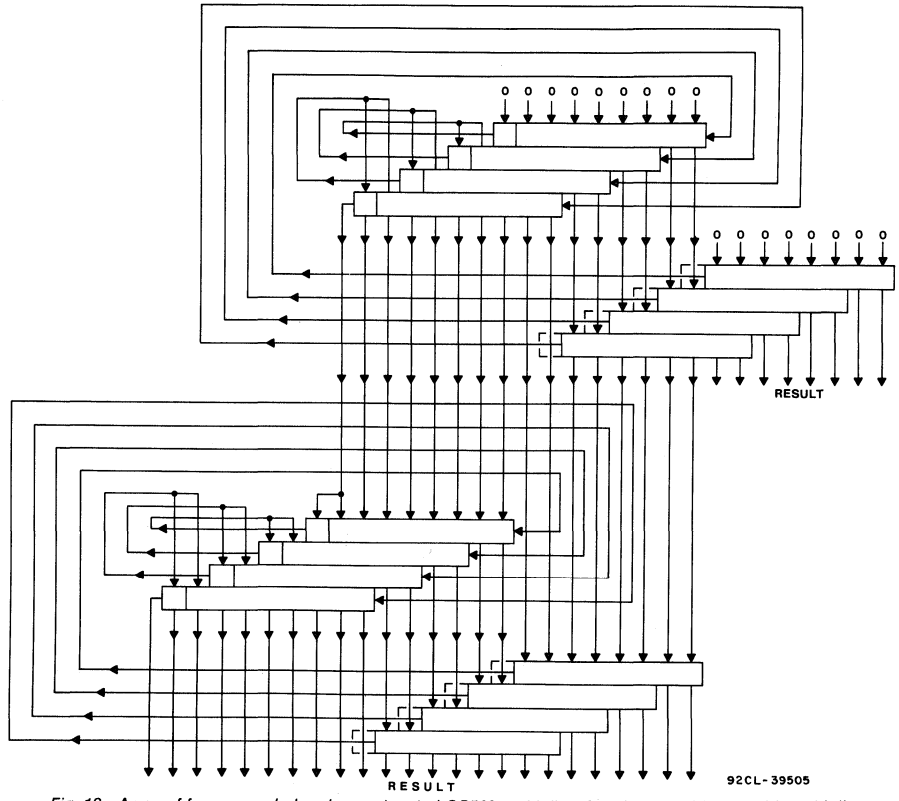


Fig. 13 - Array of four cascaded and concatenated GP503 multipliers forming a 16-bit by 16-bit multiplier.

GP503/1RZ

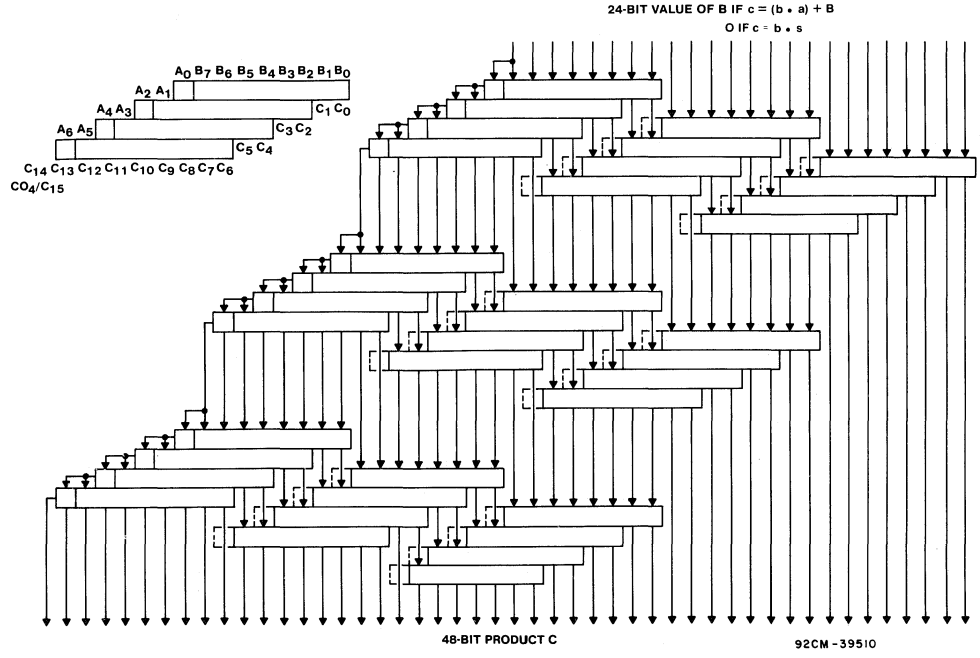


Fig. 14 - Connections of A, B and c pins in 24-bit by 24-bit multiplier array.

High-Reliability Semicustom ICs

RCA High-Reliability Semicustom Capabilities

RCA high-reliability semicustom integrated circuits include both gate arrays and standard cells that are processed and screened to MIL-STD-883 modified Class S and B requirements.

RCA has high-reliability capabilities in:

- Gate Arrays (Automated)
  - PA40000 (3-micron, bulk silicon-gate, CMOS)
  - PA50000 (3-micron, double-level-metal, silicon-gate, CMOS)
  - PA60000 (4-micron, silicon-gate, radiation-hardened, CMOS/SOS)
- PaCMOS Standard-Cell Families
  - CMOS/SOS (3-micron, silicon-gate, radiation-hardened, CMOS/SOS)
  - CMOS II (3-micron, bulk silicon-gate, CMOS)
  - CMOS IID (3-micron, double-level-metal, bulk silicon-gate CMOS)
  - CMOS III (2-micron, double-level-metal, bulk silicon-gate CMOS)

The semicustom designs are fully supported by the following design automation software:

MIMIC - Logic simulation and fault analysis plus user-definable behavioral modeling with the industry's most extensive hazard analysis.

MP2D - Automated placement and routing of interconnections for PaCMOS Standard Cells.

AUA & MERLYN - Automatic placement and routing of interconnections for Gate Arrays with utilization capability exceeding 90 per cent.

SCOAP - Controllability/observability test analysis

AFTER - Test program generation

CONCERT - Connectivity check and parasitic capacitance and resistance extraction of interconnects for both single- and double-level metal.

Accessible from Daisy Systems, Valid Logic, and Mentor Graphics workstations.

Hardware support includes:

- CALMA editors
- ARTCON databases
- MEBES - produced mask generation

Special radiation-hardened semicustom circuits are fabricated using the RCA radiation-hardening CMOS silicon-on-sapphire technology. This CMOS/SOS technology provides exceptional tolerance for withstanding transient radiation, total-dose radiation, and single-event-upset (SEU).

The basic radiation tolerance of CMOS/SOS comes about because the n- and p-transistors are isolated from each other by the insulating sapphire substrate, as shown in Fig. 1. Conventional bulk-silicon-substrate devices are isolated only by electrically fragile pn junctions. The isolation of the transistors on the non-conductive sapphire substrate makes SOS technology inherently resistive to latchup.

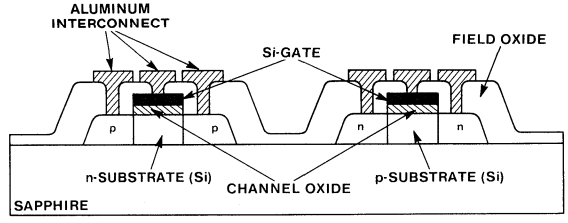


Fig. 1 - Cross-sectional view of CMOS/SOS structure showing the sapphire substrate insulating the n- and p-transistors from each other.

Automated Design System

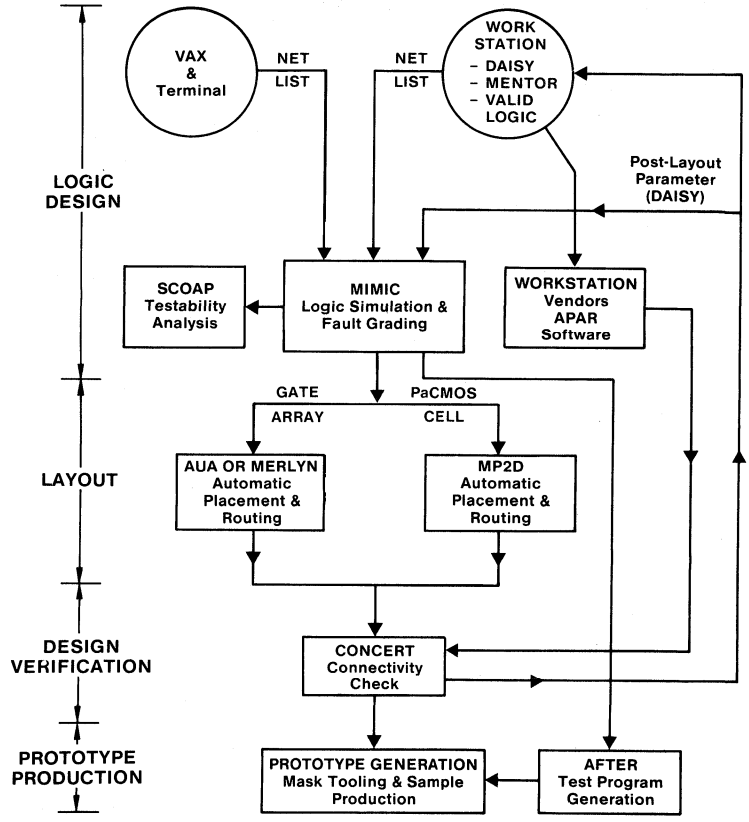


Fig. 2 - Relationship of MIMIC and supporting programs used for the automated design of LSI Semicustom circuits.

Gate Arrays

Gate arrays are a proven high-reliability, low-cost solution to semicustom LSI circuit design. Because gate arrays use standard chips customized by one or four personalization masks, design turnaround time is short and the correction of potential system-integration errors or design change is easily accomplished. Both gate arrays and PaCMOS standard cells interface directly with RCA CD4000-series, CDP6805-series, and CDP1800-series CMOS devices as well as with QMOS and p- and n-type MOS circuits. Gate arrays rival the speed of bipolar devices and offer the additional inherent CMOS advantages of low power dissipation, high noise immunity, and wide supply-voltage operating range. The PA60000 series of gate arrays uses the CMOS/SOS technology and has the advantage of high-speed high latchup resistivity, and high radiation tolerance. Operated with a supply voltage of 5 volts, it has a typical gate delay of only 2 nanoseconds. Gate arrays do not require process experience to implement and the three available customer entry levels provide a flexible relationship between cost and customer involvement.

An RCA gate array is a CMOS LSI chip consisting of p devices, n devices, and tunnels in a repetitive ordered structure on either a silicon or a sapphire substrate. All device nodes (gates, drains, and sources) are accessible. Gate arrays are available for both double-level and single-level metallization.

In double-level-metal gate arrays, a sequence of four "personalization" masks (contact, first metal, via, and second metal) defines the interconnect pattern that implements the required logic function. In single-level-metal gate arrays a single personalization metal mask defines the logic function.

Each gate consists of two p and two n devices and is equivalent to a two-input gate. For purposes of estimating array size for a given application, the list given in Table I is helpful. Although some small number of gates may be inaccessible because of interconnect restrictions, the RCA automatic design process permits utilization of 80% of the total gates available for any one application with single-level metal and often as high as 95% with double-level metal.

As gate count and design complexities increase, manual intervention to complete what otherwise would be a fully automated layout becomes costly and time consuming.

As a desirable cost-saving alternative RCA has developed very sophisticated automated placement and routing techniques. As a result, design systems with manual intervention are no longer required.

Table I. Examples of Logic Functions Available with Gate Arrays

Logic Function	Number of Gates Required
Inverter	1
2-Input NAND	1
2-Input NOR	1
4-Input NAND	2
4-Input NOR	2
(A+B) (C+D) = X	2
R & S Flip-Flop	2
$R_1R_2S_1S_2$ Flip-Flop	3
Static Shift Register (S/R)	5
Static S/R with Low Set	6
Static S/R with High Reset	6
Static S/R with High Set & Reset	8

With RCA's Automated Design System, artwork is generated automatically from RCA's extensive library of logic cells. Once a semicustom circuit is designed, a design audit is conducted. The audit includes the recreation of the network description from artwork and resimulation with actual resistive and capacitive parasitics taken into account. RCA has one of the industry's most advanced and comprehensive design audit system that gives the user the confidence that the design will work the first time.

Most RCA logic macros (predefined logic structures or cells) are common for both gate arrays and for PaCMOS standard cells. The design process for both gate arrays and standard cells is essentially common.

Whenever the RCA Automated Design System has been used for gate array LSI circuits, it has proved to be very effective. For complex random logic applications it has provided 100 per cent connectivity. With RCA's gate arrays, significant savings can be achieved because of the assurance that the arrays will fit into the smallest practical die size.

Table II. Basic Characteristics of the PA40000, PA50000, and PA60000 Series of Gate Arrays

Library	Technology	Typical Gate Delay at 5 V (ns)	Operating Voltage Range (V)	Total Number of Gates	Total Number of Pads
PA40000	3-micron Single-Level Metal, Bulk Si-Gate CMOS	2.5	3-6	650 850 1000 1200	74 86 94 102
PA50000	3-micron Double-Level Metal, Bulk Si-Gate CMOS	2.5	3-6	900 1400 2200 3200 4200 6000	74 92 114 138 156 180
PA60000	4-micron Single-Level Metal, Si-Gate CMOS/SOS	2	3-10	650 1200	74 102

Note: For 2-input NAND gate operated at 5 volts; fanout = 2, local interconnect.

Gate Arrays

Table III. Static Electrical Characteristics of the PA40000 and PA60000 Series of Gate Arrays.

Specified at V_{DD} -V_{SS} = 5 V

CHARACTERISTIC		CONDITIONS			LIMITS				UNITS
					-55°C-+125°C				
		V_{OUT}	V_{IN}	V_{DD}	PA40000		PA60000		
		(V)	(V)	(V)	Min.	Max.	Min.	Max.	
Low-Level Input Voltage,	V_{IL}	0, 5		5	—	1.5	—	1.5	V
High-Level Input Voltage,	V_{IH}	0, 5		5	3.5	—	3.5	—	
Low-Level Output Voltage, ($I_{OUT} \leq 1\ \mu A$),	V_{OL}		0, 5	5	—	0.05	—	0.05	
High-Level Output Voltage,	V_{OH}		0, 5	5	4.95	—	4.95	—	
Output Low Drive (Sink) Current,	I_{OL}	0.4	0, 5	5	0.8	—	0.65	—	mA
Low Z					1.8	—	1.25	—	
Output High Drive (Source) Current,	I_{OH}	4.6	0, 5	5	0.48	—	0.50	—	
Low Z					1.6	—	1.20	—	

Functions on Array Periphery

To provide longer delays and active pull-up resistors, high-impedance cells are placed strategically along the periphery of the PA40000 and PA60000 gate arrays. In order to source and sink TTL levels of current or to drive off-chip capacitive loads at high speed, low-impedance cells are also provided along each side of the array.

RCA's PA60000 series of gate arrays has as an additional periphery feature a special spark gap and gated diode circuit to protect against a static discharge. An n device and a p device are also associated with each pad and can be used as an input inverter, an output inverter, or as a transmission gate.

PaCMOS Standard Cells

PaCMOS, an acronym for Programmable Automated Cell CMOS, is an RCA computer-automated design approach to LSI. It is based on a group of standard building blocks, called standard cells, that can be automatically chosen, placed, and interconnected by means of computer programs to provide an LSI circuit design.

RCA has a large and expanding library of previously designed, verified, and life-tested standard cells available in three technologies: CMOS II, CMOS IID, and CMOS/SOS. The major characteristics of these three cell families are given in Table IV. As an aid in selecting appropriate cells, a Standard Cell Notebook is available. In this Notebook, all of the logic cells are fully characterized and in the form of data sheets. The data sheet provides the name and function of the cell, the logic configuration, the Boolean equation, the truth table, and the worst/best case dynamic performance data.

By using the Standard Cell Notebook, the designer can match the desired circuit configuration with the available standard cells and generate an input net list. Each multi-port standard cell is characterized by its input and output pin connections. Pin connections are accessible for inter-connect wiring at both the top and the bottom of each cell. Sophisticated algorithms automatically select the most appropriate I/O connections to minimize wire length and area and to produce a densely packed, efficient layout. Pin swapping on logically equivalent inputs, for example the inputs to a NAND gate, is accomplished algorithmically to handle tough problems that if done normally would require maze routers and other approaches. This structured computerized layout also simplifies the checking of both interconnection and design rules. Because each individual cell has been previously verified, only the computer-generated interconnections must be checked. The connectivity certifier, CONCERT, performs this task automatically.

PaCMOS Standard Cells

Table IV. Major Characteristics of the PaCMOS Standard Cell Families

	Single-Level Metal CMOS II	Double-Level Metal CMOS IID	Double-Level Metal CMOS III	Single-Level Metal CMOS/SOS
Gates - maximum number	4500+	5000+	10000	3500
Operating Voltage Range - volts	3-6	3-6	3-6	3-10
Stage Delay[a] - nanoseconds	2.3	2.3	1.5	2.0
Cell Height - mils	5.5	5.5	3.0	4.2
Pin Spacing - mils	0.42	0.42	0.30	0.56
Channel Length - microns	2.6[b]	2.6[b]	2.0	4.0
Cell Density - sq. mils/trans.	3	3	1.8	3
Chip Density - sq. mils/trans.	9	9	4	9

[a] For 2-input NAND gate operated at 5 volts; fanout = 2, no interconnect.

[b] Effective channel length.

PaCMOS Sub-Chip RAM

Now available in RCA's CMOS IID double-level-metal standard cell library is a new software-compilable, variable-size RAM "sub-chip." The designer can specify up to four of these modules per design, each having a total storage size ranging from 4 x 4 bits to 1 K bits with word lengths to 32 bits. From 4 to 128 addressable words may be specified in increments of four. With this sub-chip RAM, individual RAMs of up to 1024 bits may be designed. A RAM size of 32 words by 32 bits would meet this limit. A 128-word by 32-bit configuration would be accommodated by four such 32 x 32 modules. A memory configuration is shown in Fig. 3. The typical read access cycle time for 1-K RAM versions is in the order of 60 nanoseconds. Listed in Table V are a few examples of user-defined, software-compilable RAM cell sizes available using the specified guidelines.

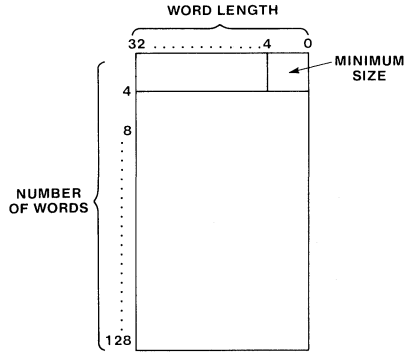


Fig. 3 - Memory configuration for variable-size RAM sub-chip.

Added Options

In addition to the standard cells, PaCMOS can accommodate other sub-chip options. Future enhancements to the system, such as ROMs, PLAs, register stacks, and core processors, which have been remotely designed by conventional techniques, can be automatically connected while the rest of the host design is computer generated. The net effect of incorporating the sub-chip option into the standard cell layout is to combine the high density and performance optimization of handcrafted designs with the low-cost quick turnaround capabilities provided by the standard cell automatic layout program.

Comparison of Standard Cells and Gate Arrays

PaCMOS standard cells and gate arrays offer attractive trade-offs between development time and cost, size and functionality.

Standard cells are offered as libraries of functional logic blocks or cells that are automatically positioned and routed (interconnected) by computer to achieve optimum die size. As a result, standard cell circuits have a smaller die size than equivalent gate array circuits. A further advantage is that reduced interconnect delay leads to higher-speed performance. In addition, the availability of more complex PaCMOS cells such as RAMs and analog circuits increases design flexibility.

Gate array circuits, on the other hand, have a faster development time and slightly lower development costs because users need only pay for the mask levels needed to interconnect prefabricated transistors.

In volume production, however, PaCMOS standard cell designs can achieve significant cost advantages over gate array designs.

Table V. Examples of RAM Cell Sizes Available with the CMOS IID Sub-chip

Words	x	Bits	
4	x	4	(minimum words and word length)
4	x	5	
8	x	4	
128	x	8	(maximum possible number of words)
64	x	16	
32	x	32	(maximum possible word length)

Comparison of Standard Cells and Gate Arrays

Fig. 4 compares the relative cost of automated designs using gate arrays, PaCMOS standard cells, and fully custom LSI circuits. The curves indicate that production quantities starting between 25,000 and 100,000 are required for an economical fully custom design. Standard cells are more economical for quantities as low as 1000 units of production depending upon the logic complexity.

Fig. 5 is a graph showing the relationship of cost and device complexity for both PaCMOS II and gate array designs. This figure is based on a 40-pin DIP package, a standard-cell design, and the production cost of 10,000 units. The costs are normalized; a 3000-gate device equals 1.0. For the gate-array design an 80-per cent utilization rate is assumed.

Fig. 6 is a bar chart showing the relative advantages of CMOS devices, gate arrays, PaCMOS standard cells and custom circuit designs. The data for this bar chart were taken from the May 13, 1985 issue of EE Times.

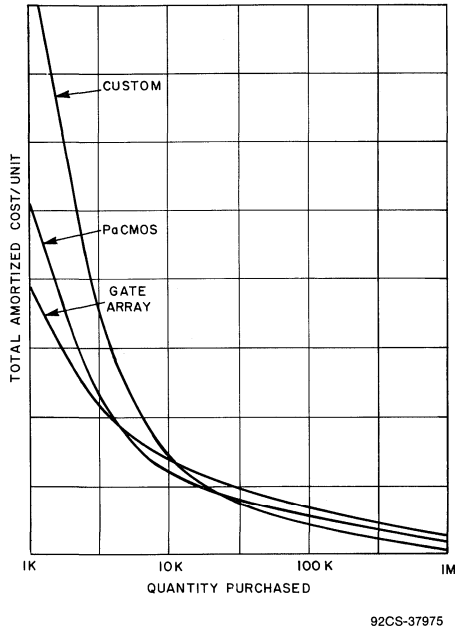


Fig. 4 - Comparison of relative costs of automated designs using PaCMOS standard cells, gate arrays, or fully customized LSI circuits.

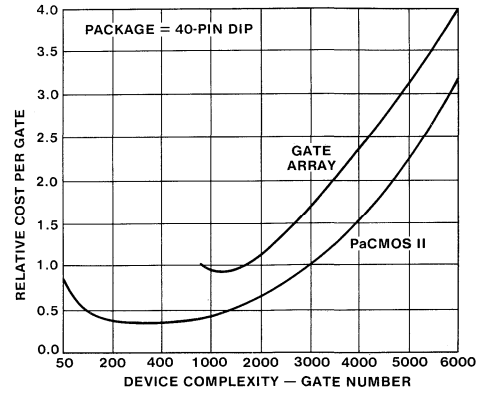


Fig. 5 - Relationship of cost and device complexity for both PaCMOS standard cell and gate array designs. Based on design and production cost of 10,000 units. Normalized - cost of 3000-gate standard-cell device equals 1.0.

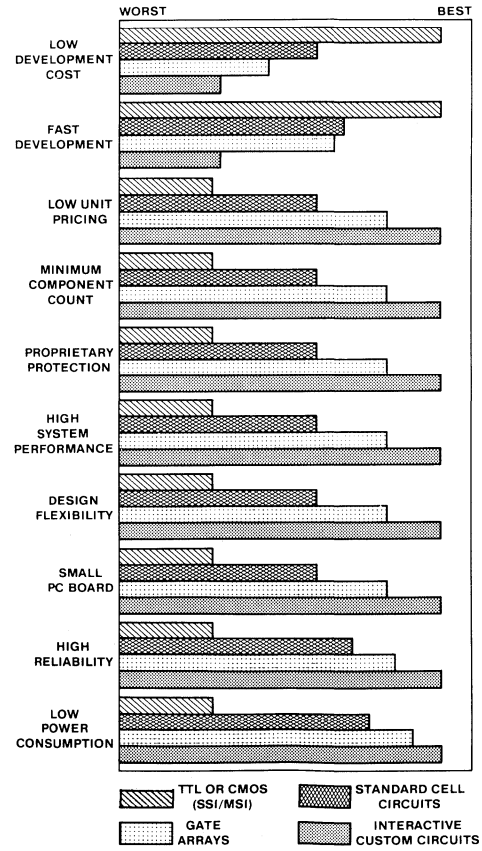


Fig. 6 - Relative advantages of CMOS devices, gate arrays, PaCMOS standard cells, and fully custom LSI circuit designs. (Data from EE times, May 13, 1985).

High-Reliability Power Devices

High-Reliability Power Products

Solid-state devices classified as high-reliability types have come to be primarily associated with military and aerospace applications. In many ways, this association is misleading because the commerical equipment market is probably the largest user of high-reliability products, but not necessarily by that label. Military and aerospace agencies, however, have been largely responsible for establishment of comprehensive published reliability specifications and standards which have been accepted by the solid-state industry. MIL standards dominate the procedures used to specify high-reliability solid-state devices and represent a common reference point frequently used by commerical users to define their requirements.

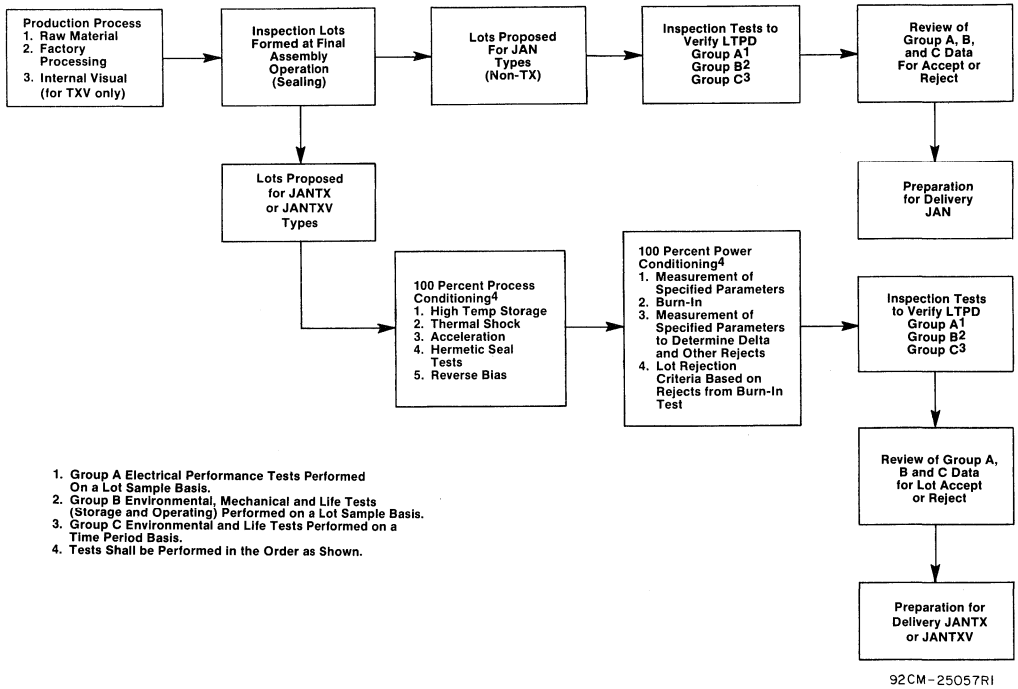
Military and aerospace requirements for high-reliability solid-state devices are extremely large and diverse, not only in terms of performance, operating conditions, and reliability, but also in terms of logistics and procurement. As a result of these requirements, the military services have jointly developed specifications and standards under which most military end-use solid-state devices are procured. To simplify procurement, logistics, and the development of reliability data, MIL specs are not issued for the full spectrum of devices manufactured: rather, they are restricted to those devices for which significant need is demonstrated and are specified so that the device can have as wide applicability as possible. Although the limits for operating conditions may exceed those required for some applications, they simplify procurement and assure a supply of devices for the majority of military equipment. These standards also cover a wide range of requirements for the manufacturer on such things as:

(a) The procedure and requirements for a manufacturer to become certified to manufacture MIL-spec parts.
(b) The requirements for qualifying parts.
(c) Product-assurance provisions in such areas as quality control, inspection procedures, personnel training, cleanliness, failure analysis, and documentation.
(d) Test methods and procedures.
(e) Marking and identification of product.
(f) Preservation and packing.

JAN, JANTX, and JANTXV Solid-State Power Devices

The major military specification used for the procurement of standard solid-state devices by the military is MIL-S-19500, which covers the devices such as discrete transistors, thyristors, and diodes.

MIL-S-19500 is the specification for the familiar "JAN" type solid state devices. Detailed electrical specifications are prepared as needed by the three military services and coordinated by the Defense Electronic Supply Center (DESC).



Order of procedure diagram for JAN, JANTX, and JANTXV solid-state devices.

JAN, JANTX, and JANTXV Devices

Levels of reliability are defined by MIL-S-19500. JAN types receive Group A, Group B, and Group C lot sampling only, and are the least expensive. JANTX types receive 100 percent process conditioning, and power conditioning, and are subjected to lot rejection based on delta parameter criteria in addition to Group A, Group B, and Group C lot sampling. JANTXV types are subjected to 100 percent (JTXV) internal visual inspection in addition to all of the JANTX tests in accordance with MIL-STD-750 test methods and MIL-S-19500.

DESC publishes "QPL-19500", a Qualified Products List of all types and suppliers approved to produce and brand devices in accordance with MIL-S-19500.

The following tables list approved "QPL" types and types that are process of testing preliminary to QPL approval by DESC, respectively.

Custom high reliability selections of RCA Power devices can also be supplied with similar process and power conditioning tests and delta criteria.

QPL Approved Types

RCA is presently qualified on the following devices. Prices and delivery quotations may be obtained from your local sales representative.

Bipolar Power Transistors

Types	MIL-S 19500/	Package	Polarity	P_T (W)	I_C (A)	V_{CEO} (V)	h_{FE} Min.	h_{FE} I_C (A)	f_T (MHz)
2N3439, 2N3440	368	TO-39	N-P-N	0.8	1	350	40	0.02	15
2N3584, 2N3585	384	TO-66	N-P-N	35	2	300	25	1	15
2N3879	526	TO-66	N-P-N	35	7	75	20	4	40
2N5038, 2N5039	439	TO-204AA	N-P-N	140	20	90	20	12	60
2N5302, 2N5303	456	TO-204AA	N-P-N	200	30	80	15	15	2
2N5415S, 2N5416S	485	TO-39	P-N-P	0.75	1	300	30	0.05	15
2N5671, 2N5672	488	TO-204AA	N-P-N	140	30	120	20	20	50
2N6032, 2N6033	528	TO-204AE	N-P-N	140	50	120	10	50	50
2N6211-2N6213	461	TO-66	P-N-P	35	2	350	30	1	20
2N6283, 2N6284	504	TO-204AA	N-P-N	175	20	100	1250	10	8
2N6306, 2N6308	498	TO-204AA	N-P-N	125	8	350	15	3	5
2N6383-2N6385	523	TO-204AA	N-P-N	100	10	80	1000	5	20
2N6546	525	TO-204AA	N-P-N	175	15	300	12	5	60
2N6648-2N6650	527	TO-204AA	P-N-P	85	10	80	1000	5	20
2N6671, 2N6673	536	TO-204AA	N-P-N	150	10	400	10	5	15
2N6674, 2N6675	537	TO-204AA*	N-P-N	175	20	400	8	10	15
2N6676, 2N6678	538	TO-204AA	N-P-N	175	20	400	8	10	15

Power MOSFETs

N-Channel Types	MIL-S 19500/	Package	Channel	P_T (W)	I_D (A)	$V_{BR(DSS)}$ (V)	$r_{DS(on)}$ Ω
2N6764	543A	TO-204AE	N	150	38	100	0.055
2N6766	543A	TO-204AE	N	150	30	200	0.085
2N6756	542A	TO-204AA	N	75	14	100	0.18
2N6758	542A	TO-204AA	N	75	9	200	0.4
2N6760	542A	TO-204AA	N	75	5.5	400	1
2N6762	542A	TO-204AA	N	75	4.5	500	1.5
2N6788	555	TO-205AF	N	20	6	100	0.3
2N6796	557	TO-205AF	N	25	8	100	0.18

SCR's

Types	MIL-S 19500/	Package	V_{DRM} (V)	$I_{T(RMS)}$ (A)	V_{GT} (V)	I_{GT} (mA)	dv/dt (V/μs)
2N682	108	TO-48	50	25	3	35	20
2N683	108	TO-48	100	25	3	35	20
2N685	108	TO-48	200	25	3	35	20
2N686	108	TO-48	250	25	3	35	20
2N687	108	TO-48	300	25	3	35	20
2N688	108	TO-48	400	25	3	35	20
2N690	108	TO-48	600	25	3	35	20

JAN, JANTX, and JANTXV Devices

Types Planned for 1986 QPL Approval

RCA plans to request authorization to qualify the following types for QPL listing and presently anticipates completion of the required test procedures by the date noted below.

Power MOSFETs

N-Channel Types	MIL-S 19500/	Package	Channel	P_T (W)	I_D (A)	$V_{BR(DSS)}$ (V)	$r_{DS(on)}$ Ω	Anticipated Approval Date
2N6782	556	TO-205AF	N	15	3.5	100	0.6	1/86
2N6768	543A	TO-204AA	N	150	14	400	0.3	3/86
2N6770	543A	TO-204AA	N	150	12	500	0.4	3/86
2N6784	XXX	TO-205AF	N	15	2.25	200	1.50	3/86
2N6786	XXX	TO-205AF	N	15	1.25	400	3.60	3/86
2N6790	555	TO-205AF	N	20	3.50	200	.80	3/86
2N6792	555	TO-205AF	N	20	2.00	400	1.80	3/86
2N6794	555	TO-205AF	N	20	1.50	500	3.00	3/86
2N6798	557	TO-205AF	N	25	5.50	100	0.40	3/86
2N6800	557	TO-205AF	N	25	3.0	400	1.00	3/86
2N6802	557	TO-205AF	N	25	2.5	500	1.50	3/86
P-Channel Types	**MIL-S 19500/**	**Package**	**Channel**	**P_T (W)**	**I_D (A)**	**$V_{BR(DSS)}$ (V)**	**$r_{DS(on)}$ Ω**	**Anticipated Approval Date**
2N6895	565	TO-205AF	P	8.33	-1.5	100	3.65	3/86
2N6896	565	TO-204AA	P	60	-6	100	0.6	3/86
2N6897	565	TO-204AA	P	100	-12	100	0.3	3/86
2N6898	565	TO-204AE	P	150	-25	100	0.2	3/86
N-Channel Logic-Level Types	**MIL-S 19500/**	**Package**	**Channel**	**P_T (W)**	**I_D (A)**	**$V_{BR(DSS)}$ (V)**	**$r_{DS(on)}$ Ω**	**Anticipated Approval Date**
2N6901	566	TO-205AF	N	8.33	-1.5	100	1.4	3/86
2N6902	566	TO-204AA	N	75	-12	100	0.2	3/86
2N6903	566	TO-205AF	N	8.33	-1.5	200	3.65	3/86
2N6904	566	TO-204AA	N	75	-8	200	0.65	3/86

Added Value Screening

RCA Added Value Screening for Power MOSFETs, Transistors, Thyristors, and Chips

Many solid-state devices not yet covered by military specifications, because they are too new, offer the most recent technological advances or have special performance characteristics which offer advantages to the designer of high-reliability equipment. RCA cooperates with the users of such devices in establishment of high-reliability specifications patterned after MIL standards, which allow these designs to be approved for use in military and aerospace systems, as well as commercial equipment.

Most procurements of solid-state devices for military systems are made by the equipment contractor from the MIL-STD parts list as awards are received for electronic equipment. Some military and aerospace programs, because of their size, duration, or special requirements (Minuteman and Peacekepper are two examples), require that special specifications and process methods, or even special production lines, be established and tailored to the particular functional, reliability, and economic needs of the program. RCA Solid State Division has frequently used the resources of its laboratories, production, facilities, and expert technical staff to contribute to the success of such programs.

All RCA high-reliability solid-state power devices are processed in accordance with provisions of MIL-S-19500. The desired screening test sequence can be chosen from the models shown in Table III.

Class S devices provide wafer lot control traceability from wafer diffusion through screening.

Class S chips also provide wafer lot control traceability from wafer diffusion through screening. A sample of 22 devices taken from this lot is assembled in a suitable package. The assembled sample devices are subjected to the Class S screening sequence in the table below. Class S chips are released for shipment when the assembled sample devices successfully pass the screen.

Group B and Group C tests will be performed when requested in accordance with MIL-S-19500.

ADDED VALUE HIGH-RELIABILITY SCREENING

SCREEN	MIL-STD-750 METHOD	CONDITION	CLASS S REQUIREMENTS	CLASS V REQUIREMENTS	CLASS X REQUIREMENTS
1. Internal Visual	2072	For transistors.	100%	100%	—
2. High Temp Life (LTPD) (stabilization bake)	1032	24 hrs min at max rated storage temp.	100%	100%	100%
3. Thermal shock (temp cycling)	1051	No dwell is required at 25° C. Test condition C, 20 cycles, t (extremes) > 10 min.	100%	100%	100%
4. Constant acceleration 1/	2006	Y_1 direction at 20,000 G min except at 10,000 G min for devices with power rating of > 10 watts at T_C = 25° C. The 1 min hold time requirement shall not apply.	100%	100%	100%

Added Value Screening

ADDED VALUE HIGH-RELIABILITY SCREENING (Continued)

SCREEN	MIL-STD-750 METHOD	CONDITION	CLASS S REQUIREMENTS	CLASS V REQUIREMENTS	CLASS X REQUIREMENTS
5. Hermetic Seal Fine 1/	1071	Test condition G or H, max leak rate = $5x10^{-8}$ atm cc/s except $5x10^{-7}$ atm cc/s for devices with internal cavity > 0.3 cc.	Optional if done in screen 14.	100% 4/	100% 4/
Gross		Test condition A, C, D, E, or F.	Optional	100% 4/	100% 4/
6. Serialization		See 3.7.9.	100%		
7. Interim Electrical Parameters		As specified.	100% (Read and record)		
8. High Temp Reverse Bias (HTRB)		48 hrs min at T_A = 150° C (min) and minimum applied voltage as follows:			
Burn-in (for transistors)	1039	Transistors - 80% (min) of rated V_{CB} (bipolar), $V_{GS(FET)}$, or $V_{DS(FET)}$ as applicable. Test condition A.	100%	100%	100%
9. Interim electrical and delta parameters		As specified but including all delta parameters as a minimum. Leakage current shall be measured on each device before any other test is made.	100% (Measure all specified parameters within 16 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 11.)	100% (Measure all specified parameters within 24 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 11.)	100% (Measure all specified parameters within 24 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 11.)

Added Value Screening

ADDED VALUE HIGH-RELIABILITY SCREENING (Continued)

SCREEN	MIL-STD-750 METHOD	CONDITION	CLASS S REQUIREMENTS	CLASS V REQUIREMENTS	CLASS X REQUIREMENTS
10. Power Burn-In		As specified.	100%	100%	100%
Burn-In (Transistors)		Transistors. Test condition B.	240 hrs (min)	160 hrs (min)	160 hrs (min)
Burn-In (Thyristors) 3/	1040	Thyristors.	240 hrs (min)	96 hrs (min)	96 hrs (min)
11. Final Electrical Test		As specified.	100%	100%	100%
Interim Electrical		All interim and delta parameter measurements must be completed within 96 hrs after removal from burn-in conditions.	Interim electrical and delta parameters as a minimum. (Read and record.)	Interim electrical and delta parameters as a minimum. (Read and record.)	Interim electrical and delta parameters as a minimum. (Read and record.)
Other Electrical Parameters			Group A, sub-groups 2 and 3.	Group A, sub-groups 2 and 3.	Group A, sub-roups 2 and 3.
12. Hermetic Seal	1071	(Same as 5 on previous page) 2/	100%	Optional 4/	Optional 4/
Fine 1/					
Gross					
13. Radiography	2076	2/	100%	—	—
14. External Visual Examination	2071	To be performed after complete marking.	100%	—	—

*1/ Omit fine leak seal test and constant acceleration test for double plug, non-internal cavity diode construction.
*2/ The radiographic and seal screens for JANS may be performed in any order following final electrical test. Glass diodes shall not be painted until after seal tests. When hermetic seal testing is performed in screen 5 it does not have to be performed again in screen 12 for double plug, non-internal cavity diode construction.
*3/ Reverse-blocking test shall replace power burn-in for power rectifiers at $\geq$ 10 amp rating at $T_C \geq 100°$ C and all thyristors.
4/ Fine and gross seal leak test for JANTX and JANTXV shall be performed in either block 5 or block 12.

Radiation-Resistant Power Transistors

RCA offers a variety of bipolar silicon power transistors in which special design and processing techniques are used to assure continued functional performance after exposure to specified dosages of neutron and gamma radiation.

The following types are recommended for those applications where radiation tolerance is a critical factor. Radiation tolerance is not covered by present slash (/) specifications. Device capabilities and system requirements are generally limited to a custom specification basis.

Types	Package	Polarity	P_T (W)	h_{FE} Min.	h_{FE} I_C(A)	V_{CEO} (V)
2N3879	TO-66	N-P-N	35	20	4	75
2N5038	TO-204AA	N-P-N	140	20	12	90
2N5320	TO-39	N-P-N	10	10	1	75
2N5322	TO-39	P-N-P	10	10	1	75
2N5672	TO-204AA	N-P-N	140	20	20	120
2N6248	TO-204AA	P-N-P	125	5	10	100
2N6480	Radial	N-P-N	87	20	12	100
2N6673	TO-204AA	N-P-N	150	10	5	400
2N6688	TO-204AA	N-P-N	200	15	20	200
TA9107 (Dev. Type)	Radial	N-P-N	87	50	8	80

For all types except TA9107,
Gamma Intensity (RAD(Si/s) = 1×10^7
Neutron Fluence (N/cm^2) = 5×10^{13}

For TA9107,
Gamma Intensity (RAD(Si)/s) = 1×10^8
Neutron Fluence (N/cm^2) = 1×10^{14}

See Application Note AN-6320 for Data

Neutron-Radiation Compensation

In RCA radiation-resistant power transistors, the base width is made as narrow as possible (consistent with other design objectives) to achieve a minimum base transit time so that a maximum number of minority carriers can complete the journey through the base. The narrower base width thus compensates for the major cause of failure in transistors exposed to neutron radiation, the reduction in minority-carrier lifetime and the corresponding decrease in transistor current gain. The voltage-supporting region in the collector is also made as narrow as feasible and is heavily doped. In this way, the series-resistance path is made as low as possible to compensate for the rise in collector series resistance and the resulting higher saturation voltage caused by exposure of the transistor to neutron radiation.

The problem of increased leakage currents is solved by use of epitaxial-planar transistors. The initial leakage in these transistors is so small that even the higher levels caused by neutron bombardment are unlikely to cause failure.

Because the narrower base width and reduced collector resistivity used to improve transistor radiation resistance are contradictory to the design requirement for high-voltage, high-energy transistors, designers should adjust circuits to require the minimum possible emitter-to-collector voltage-breakdown capability. In addition, ratings for transistors should be specified in accordance with the way in which the devices are to be used. (i.e., V_{CE} or V_{CEV}, and never V_{CEO}). The circuit design should also provide high-energy protection for the transistor.

Gamma-Radiation Compensation

The gamma dose rate at which the onset of secondary photocurrent occurs depends strongly on the geometry of the transistor emitter. The secondary photocurrent is initiated when a portion of the emitter-base junction becomes forward-biased because of the voltage drop across the lateral base resistance under the emitter. In RCA radiation-resistant transistors, the distance from the base contact to the farthest point of the base under the emitter is reduced to the minimum possible value to achieve a substantial increase in the gamma threshold level at which the secondary photocurrent starts.

Design Example

The RCA developmental transistor TA9107 is an excellent example of the radiation-resistance capability that can be achieved through the use of effective design techniques. This transistor can operate satisfactorily after exposure to neutron fluence levels of 1×10^{14} neutrons/cm^2 and can withstand a gamma dose rate of 1×10^8 rads (Si)/second before the onset of secondary photocurrent.

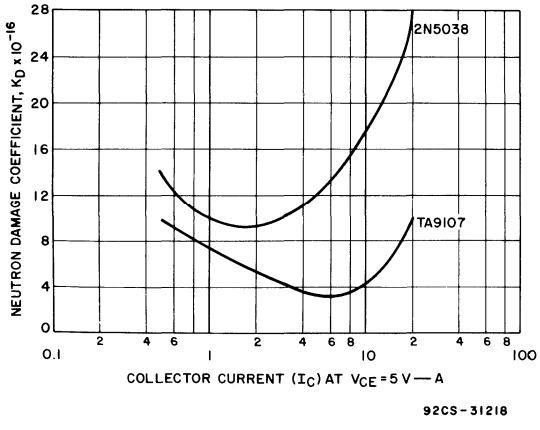
The TA9107 has a collector-to-emitter voltage rating V_{CER} of 100 volts and a post-radiation current capability of 10 amperes. The width of the collector-to-base depletion region is only 0.7 mil, the doping concentration in the collector is 1×10^{15} atoms/cm^2, and the width of the base is only about 8000 angstroms. The TA9107 employs a unique emitter design in which 32 emitter sites are interconnected by an expanded metallization system so that the maximum distance from the base contact to the center of the emitter is only 2 mils.

Aluminum metallization 50,000 angstroms thick is used in the TA9107 to assure uniform current distribution in the emitter. A gold eutectic bond is used for collector mounting.

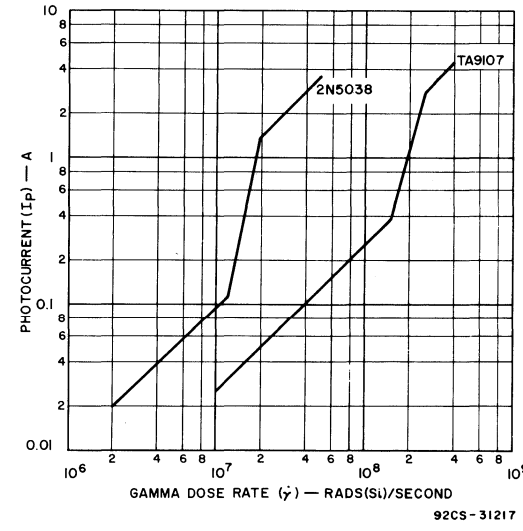
Radiation-Resistant Power Transistors

TA9107 Capability

Characteristic	Pre-Radiation	Post-Radiation (5×10^{13}N/cm^2)
V_{CEO}	80 V	80 V
V_{CBO}	100 V	100 V
V_{EBO}	5.5 V	5.5 V
h_{FE} at $I_C = 5A$, $V_{CE} = 2V$	80	10
V_{CE}(sat) at $I_C = 8A$, $h_{FE} = 5$	0.5 V	2.0 V
V_{BE}(sat) at $I_C = 8A$, $h_{FE} = 5$	1.35 V	1.5 V
$I_{S/b}$ at 75V for 100 μs	60 W	60 W
$E_{S/b}$ L P 125 μH	0.3 mj	0.3 mj
Primary Photocurrent = 250 mA typ. at 1×10^8 rad (Si)/second		
Onset of Secondary Photocurrent occurs typically at 1.5×10^8 rad(Si)/second		



Neutron damage coefficient (at 1 mev) as a function of collector current for the TA9107 and 2N5038 radiation-hardened power transistors.



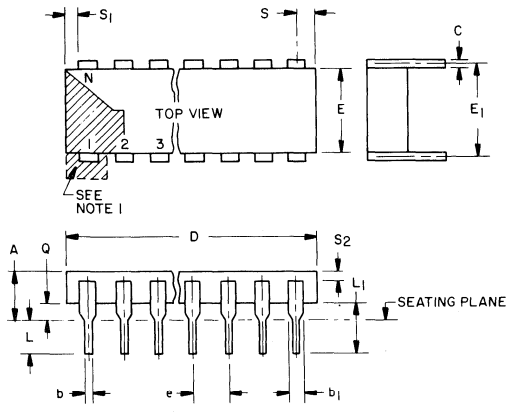
Photocurrent as a function of gamma dose rate for the TA9107 and 2N5038 radiation-hardened power transistors.

Dimensional Outlines

Dual-In-Line Side-Brazed Ceramic Packages

For CD4000-, CDP1800-, and CA3000-Series High-Reliability ICs

D SUFFIX



Notes:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be 0.023 in. (0.58 mm) for corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is 0.100 in. (2.54 mm) between centerlines. Each pin centerline shall be located within ±0.010 in. (0.25 mm) of its exact longitudinal position relative to pins 1 and N.
6. Applies to all four corners.
7. E_1 shall be measured at the centerline of the leads.
8. All leads — Increase maximum limit by 0.003 in. (0.08 mm) measured at the center of the flat, when lead finish A is applied.
9. N is the maximum quantity of lead positions.
10. Dimension S_1 shall be measured from the edge of the furthest extension of the metal pad or the lead.

14-Lead
MIL-M-38510 Case Outline D-1

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.200	—	5.08	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	0.785	—	19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5, 9
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	14		14		9
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6, 10
S_2	0.005	—	0.13	—	

92CS-39718

16-Lead
MIL-M-38510 Case Outline D-2

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.200	—	5.08	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	0.840	—	21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	16		16		9
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6, 10
S_2	0.005	—	0.13	—	

92CM-31408R2

Dual-In-Line Side-Brazed Ceramic Packages

For CD4000-, CDP1800-, and CA3000-Series High-Reliability ICs

18-Lead
MIL-M-38510 Case Outline D-6

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.200	—	5.08	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	0.960	—	24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	18		18		9
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6, 10
S_2	0.005	—	0.13	—	

92CM-31406R2

22-Lead
MIL-M-38510 Case Outline D-7

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.225	—	5.72	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	1.160	—	29.46	4
E	0.350	0.410	8.89	11.41	4
E_1	0.390	0.420	9.91	10.67	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	22		22		9
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6, 10
S_2	0.005	—	0.13	—	

92CM-31410R2

24-Lead
MIL-M-38510 Case Outline D-3

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.225	—	5.72	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	24		24		9
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6, 10
S_2	0.005	—	0.13	—	

92CM-31409R2

28-Lead

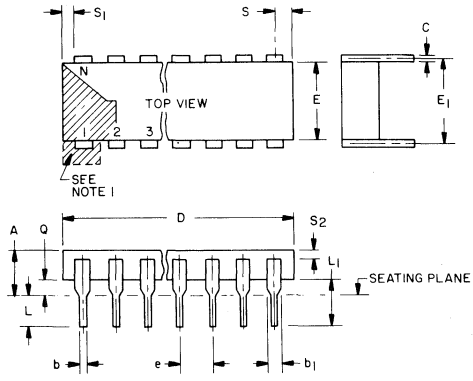
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.225	—	5.72	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	1.490	—	37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	28		28		9
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6, 10
S_2	0.005	—	0.13	—	

92CS-39719

Dual-In-Line Side-Brazed Ceramic Packages

For CD4000-, CDP1800-, and CA3000-Series High-Reliability ICs

D SUFFIX



Notes:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be 0.023 in. (0.58 mm) for corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is 0.100 in. (2.54 mm) between centerlines. Each pin centerline shall be located within ±0.010 in. (0.25 mm) of its exact longitudinal position relative to pins 1 and N.
6. Applies to all four corners.
7. E_1 shall be measured at the centerline of the leads.
8. All leads — increase maximum limit by 0.003 in. (0.08 mm) measured at the center of the flat, when lead finish A is applied.
9. N is the maximum quantity of lead positions.
10. Dimension S_1 shall be measured from the edge of the furthest extension of the metal pad or the lead.

40-Lead
MIL-M-38510 Case Outline D-5

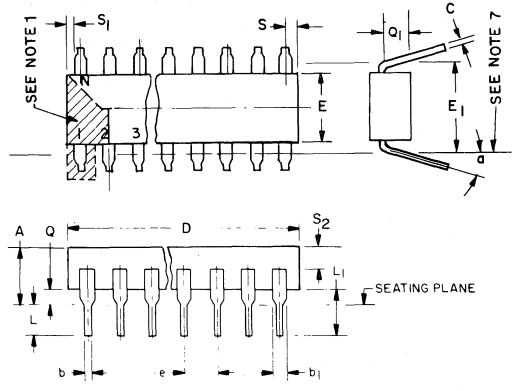
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.225	—	5.72	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	2.096	—	53.24	4
E	0.510	0.620	12.95	15.74	4
E_1	0.520	0.630	13.21	16.00	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	40		40		9
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6, 10
S_2	0.005	—	0.13	—	

92CM-31407R2

Dual-In-Line Frit-Seal Ceramic (CERDIP) Packages

For CD4000-, CD54HC/HCT-, and CA3000-Series High-Reliability ICs

F SUFFIX



Notes:

1. Index area; a notch or a pin one identification mark shall be adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be 0.023 in. (0.58 mm) for corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is 0.100 in. (2.54 mm) between centerlines. Each pin centerline shall be located within ±0.010 in. (0.25 mm) of its exact longitudinal position relative to pins 1 and N.
6. Applies to all four corners.
7. Lead center when α is 0. E_1 shall be measured at the centerline of the leads.
8. All leads — Increase maximum limit by 0.003 in. (0.08 mm) measured at the center of the flat, when lead finish A is applied.
9. N is maximum quantity of lead positions.

18-Lead
MIL-M-38510 Case Outline D-6

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.200	—	5.08	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	0.960	—	24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	18		18		9
Q	0.015	0.060	0.38	1.52	3
Q_1	0.020	—	0.51	—	
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
S_2	0.005	—	0.13	—	
α	0°	15	0°	15	

92CS-39723

20-Lead
MIL-M-38510 Case Outline D-8

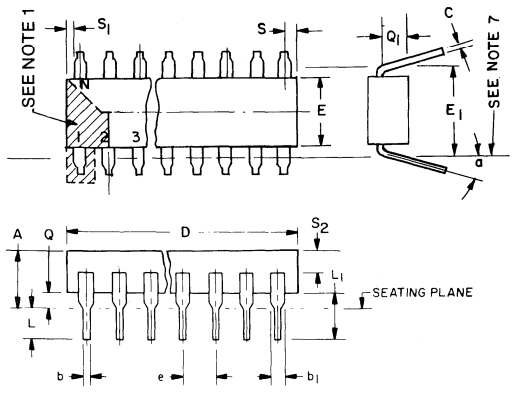
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.200	—	5.08	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	20		20		9
Q	0.015	0.060	0.38	1.52	3
Q_1	0.020	—	0.51	—	
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
S_2	0.005	—	0.13	—	
α	0°	15	0°	15	

92CS-39724

Dual-In-Line Frit-Seal Ceramic (CERDIP) Packages

For CD4000-, CD54HC/HCT-, and CA3000-Series High-Reliability ICs

F SUFFIX



Notes:

1. Index area; a notch or a pin one identification mark shall be adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be 0.023 in. (0.58 mm) for corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is 0.100 in. (2.54 mm) between centerlines. Each pin centerline shall be located within ±0.010 in. (0.25 mm) of its exact longitudinal position relative to pins 1 and N.
6. Applies to all four corners.
7. Lead center when α is 0. E_1 shall be measured at the centerline of the leads.
8. All leads — increase maximum limit by 0.003 in. (0.08 mm) measured at the center of the flat, when lead finish A is applied.
9. N is maximum quantity of lead positions.

14-Lead
MIL-M-38510 Case Outline D-1

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.200	—	5.08	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	0.785	—	19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	14		14		9
Q	0.015	0.060	0.38	1.52	3
Q_1	0.020	—	0.51	—	
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
S_2	0.005	—	0.13	—	
α	0°	15	0°	15	

92CM-31405R2

16-Lead
MIL-M-38510 Case Outline D-2

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.200	—	5.08	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	0.840	—	21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	16		16		9
Q	0.015	0.060	0.38	1.52	3
Q_1	0.020	—	0.51	—	
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
S_2	0.005	—	0.13	—	
α	0°	15	0°	15	

92CM-31404R2

Dual-In-Line Frit-Seal Ceramic (CERDIP) Packages

For CD4000-, CD54HC/HCT-, and CA3000-Series High-Reliability ICs

F SUFFIX

22-Lead
MIL-M-38510 Case Outline D-7

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.225	—	5.72	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	1.260	—	32.00	4
E	0.350	0.390	8.89	9.91	4
E_1	0.390	0.420	9.91	10.67	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	22		22		9
Q	0.015	0.075	0.38	1.91	3
Q_1	0.020	—	0.51	—	
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
S_2	0.005	—	0.13	—	
α	0°	15	0°	15	

92CS-39720

24-Lead
MIL-M-38510 Case Outline D-3

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.225	—	5.72	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	
L_1	0.150	—	3.81	—	
N	24		24		9
Q	0.015	0.075	0.38	1.91	3
Q_1	0.020	—	0.51	—	
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
S_2	0.005	—	0.13	—	
α	0°	15	0°	15	

92CM-31403R2

28-Lead
MIL-M-38510 Case Outline D-2

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.225	—	5.72	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	1.490	—	37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	
L_1	0.150	—	3.81	—	
N	28		28		9
Q	0.015	0.075	0.38	1.91	3
Q_1	0.020	—	0.51	—	
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
S_2	0.005	—	0.13	—	
α	0°	15	0°	15	

92CS-39721

40-Lead
MIL-M-38510 Case Outline D-5

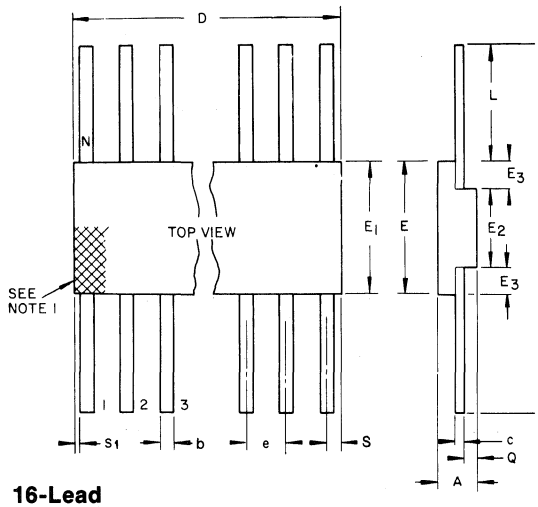
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.225	—	5.72	
b	0.014	0.023	0.36	0.58	8
b_1	0.030	0.070	0.76	1.78	2, 8
c	0.008	0.015	0.20	0.38	8
D	—	2.096	—	53.24	4
E	0.510	0.620	12.95	15.74	4
E_1	0.520	0.630	13.21	16.00	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L_1	0.150	—	3.81	—	
N	40		40		9
Q	0.015	0.060	0.38	1.52	3
Q_1	0.020	—	0.51	—	
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
S_2	0.005	—	0.13	—	
α	0°	15	0°	15	

92CS-39722

Ceramic Flat Packs

For CD4000- and CA3000-Series High-Reliability ICs

K SUFFIX



16-Lead
MIL-M-38510 Case Outline F-5
(Case Designator Z, U)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.045	0.100	1.14	2.54	11
b	0.015	0.019	0.25	0.48	5
c	0.003	0.006	0.08	0.15	5
D	—	0.440	—	11.18	3
E	0.245	0.285	6.22	7.24	
E_1	—	0.305	—	7.75	3
E_2	0.130	—	3.30	—	
E_3	0.030	—	0.76	—	
e	0.050 BSC		1.27 BSC		4
L	0.250	0.370	6.35	9.40	
Q	0.010	0.040	0.250	1.02	2
S	—	0.045	—	1.14	7
S_1	0.005	—	0.13	—	7, 9
N	16		16		6

92CS-24786R4

14-Lead
MIL-M-38510 Case Outline F-2
(Case Designator Y)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.045	0.100	1.14	2.54	11
b	0.010	0.019	0.25	0.48	5
c	0.003	0.006	0.08	0.15	5
D	—	0.390	—	9.91	3
E	0.235	0.260	5.97	6.60	
E_1	—	0.280	—	7.11	3
E_2	0.125	—	3.18	—	
E_3	0.030	—	0.76	—	
e	0.050 BSC		1.27 BSC		4
L	0.250	0.370	6.35	9.40	
Q	0.010	0.040	0.250	1.02	2
S	—	0.045	—	1.14	7
S_1	0.005	—	0.13	—	7, 8
N	14		14		6

92CS-24772R4

For Memory/Microprocessors
24-Lead

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.080	0.115	2.03	2.92	
b	0.015	0.019	0.38	0.48	5
c	0.004	0.007	0.10	0.18	5
D	—	0.640	—	16.26	3
E	0.360	0.420	9.14	10.67	
E_1	—	0.440	—	11.18	3
E_2	0.180	—	4.57	—	
E_3	0.030	—	0.76	—	
e	0.050 BSC		1.27 BSC		4
L	0.250	0.370	6.35	9.40	
Q	0.010	0.040	0.250	1.02	2
S	—	0.045	—	1.14	7
S_1	0.005	—	0.13	—	7, 10
N	24		24		6

92CS-39725

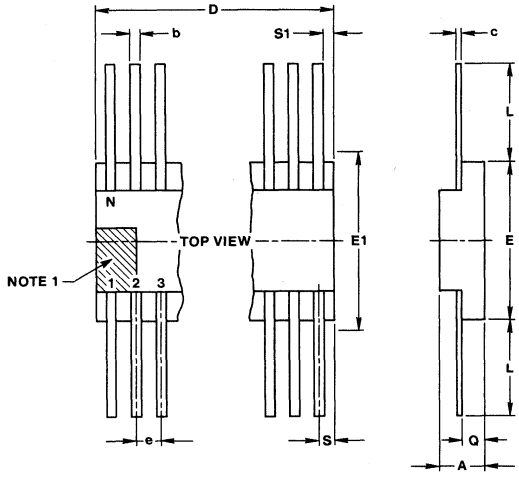
Notes:

1. Index area; a notch or pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. Dimension Q shall be measured at the point of exit of the lead from the body. The minimum Q dimension shall be 0.0085 in. (0.22 mm) when lead finish A is applied.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. The basic pin spacing is 0.050 in. (1.25 mm) between centerlines. Each pin centerline shall be located within ±0.005 in. (0.13 mm) of its exact longitudinal position relative to pins 1 and N.
5. All leads — increase maximum limit by 0.003 in. (0.08 mm) measured at the center of the flat, when lead finish A is applied.
6. N is maximum quantity of lead positions.
7. Applies to all four corners.
8. Dimension S_1 may be 0 in. (0 mm) if lead numbers 1, 7, 8, and 14 bend toward the cavity of the package within one lead width from the point of the entry of the lead into the body or if the leads are brazed to the metallized ceramic body.
9. Dimension S_1 may be 0 in. (0 mm) if lead numbers 1, 8, 9, and 16 bend toward the cavity of the package within one lead width from the point of the entry of the lead into the body or if the leads are brazed to the metallized ceramic body.
10. Dimension S may be 0 in. (0 mm) if lead numbers 1, 12, 13, and 24 bend toward the cavity of the package within one lead width from the point of the entry of the lead into the body or if the leads are brazed to the metallized ceramic body.
11. Maximum dimension allowed per MIL-M-38510 detailed specifications for CMOS.

Ceramic Flat Packs

For CD4000- and CA3000-Series High-Reliability ICs

K SUFFIX



24-Lead

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.075	0.110	1.91	2.79	
b	0.018	0.022	0.46	0.56	3
c	0.004	0.007	0.10	0.18	3
D	—	0.740	—	18.80	
E	0.600	0.660	15.24	16.76	
E_1	—	0.680	—	17.27	4
e	0.050 BSC		1.27 BSC		5
L	0.250	0.370	6.35	9.40	6
Q	0.030	0.060	0.76	1.52	7
S	—	0.100	—	2.54	8
S_1	0	—	0	—	8, 9
N	24		24		2

92CS-39748

28-Lead

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.075	0.110	1.91	2.79	
b	0.018	0.022	0.46	0.56	3
c	0.004	0.007	0.10	0.18	3
D	—	0.740	—	18.80	
E	0.600	0.660	15.24	16.76	
E_1	—	0.680	—	17.27	4
e	0.050 BSC		1.27 BSC		5
L	0.250	0.370	6.35	9.40	6
Q	0.030	0.060	0.76	1.52	7
S	—	0.045	—	1.14	8
S_1	0	—	0	—	8, 9
N	28		28		2

92CS-39726

42-Lead

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.120	—	3.05	
b	0.018	0.022	0.46	0.56	3
c	0.006	0.010	0.152	0.254	3
D	1.050	1.070	26.67	27.18	
E	0.630	0.650	16.00	16.51	
E_1	—	0.670	—	17.02	4
e	0.050 BSC		1.27 BSC		5
L	0.320	0.440	8.13	11.18	6
Q	0.040	0.070	1.02	1.78	7
S	—	0.045	—	1.14	8
S_1	0	—	0	—	8, 9
N	42		42		2

92CS-39727

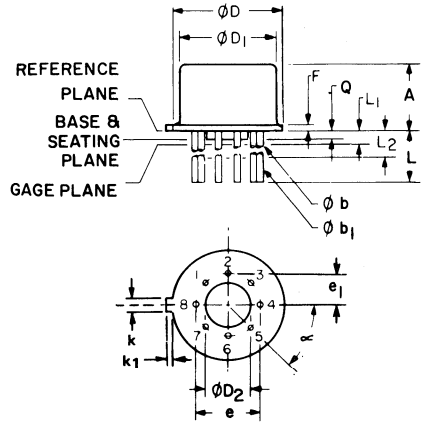
Notes:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. Total number of lead positions. Lead marked "N" is lead of highest pin number.
3. Increase maximum limit by 0.003 in. (0.08 mm) when leads are solder coated.
4. Lead thickness to be measured outside this zone.
5. Basic Spacing between Lead Centerlines. Each lead centerline is located within 0.005 in. (0.13 mm) of its True Position relative to lead number one and lead marked "N" (highest pin number).
6. Measured from the ceramic body.
7. Measured at the point of the exit of the lead from the ceramic body. Reduce minimum limit by 0.0015 in. (0.04 mm) when leads are solder coated.
8. Applies to all corner leads.
9. Dimension S_1 shall be measured from the edge of the furthest extension of the metal pad or the lead.

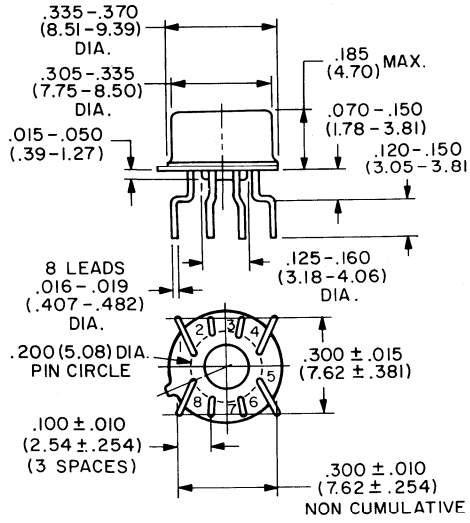
TO-5 Style Packages

For CA3000-Series High-Reliability ICs

T SUFFIX



S SUFFIX
8-Lead TO-5 with Dual-In-Line Formed Leads (DIL-CAN)



92CS-20296R3

8-Lead
MIL-M-38510 Case Outline A-1

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1, 5
ϕb_1	0.016	0.021	0.41	0.53	1, 5
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.120	0.160	3.05	4.06	
e	0.200 BSC		5.08 BSC		3
e_1	0.100 BSC		2.54 BSC		3
F	—	0.040	—	1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1	0	0.050	0	1.27	1
L_2	0.250	—	1	6.35	1
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

92CS-24774R1

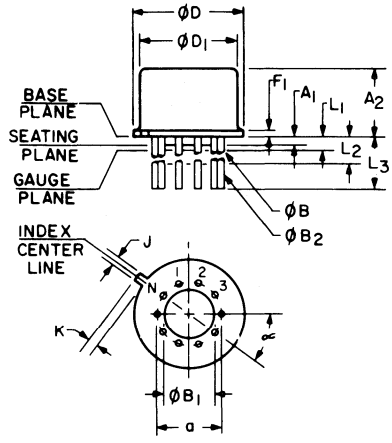
Notes:

1. (All leads) ϕb applies between L_1 and L_2; ϕb_1 applies between L_2 and 0.500 in. (12.70 mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500 in. (12.70 mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019 in. (0.48 mm) measure in gauging plane 0.054 in. (1.37 mm) +0.001 in. (0.03 mm) — 0 in. (0 mm) below the base plane of the product shall be within 0.007 in. (0.18 mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gauge.
5. All leads — increase maximum limit by 0.003 in. (0.08 mm) when lead finish A is applied.

TO-5 Style Packages

For CA3000-Series High-Reliability ICs

T SUFFIX

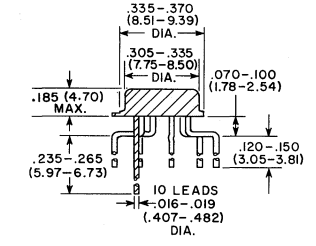


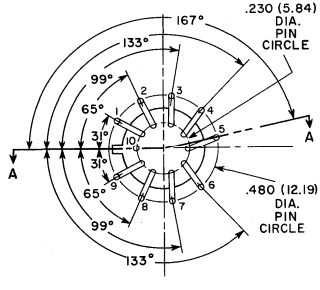
10-Lead
JEDEC Outline MO-006-AF

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
a	0.230 TP		5.84 TP		2
A_1	0	0	0	0	
A_2	0.165	0.185	4.19	4.70	
ϕB	0.016	0.019	0.407	0.482	3
ϕB_1	0	0	0	0	
ϕB_2	0.016	0.021	0.407	0.533	3
ϕD	0.335	0.370	8.51	9.39	
ϕD_1	0.305	0.335	7.75	8.50	
F_1	0.020	0.040	0.51	1.01	
j	0.028	0.034	0.712	0.863	
k	0.029	0.045	0.74	1.14	4
L_1	0	0.050	0	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	36° TP		36° TP		
N	10		10		6
N_1	1		1		5

92CS-15835

V SUFFIX
10-Lead TO-5 with Formed Leads Radially Arranged





92CS-14638R2

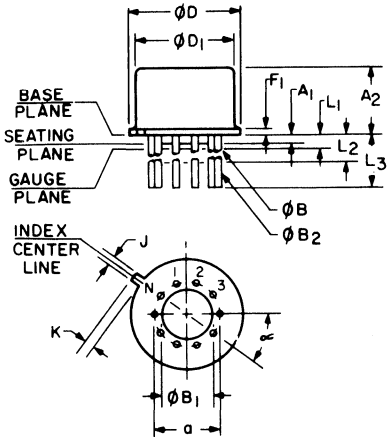
Notes:

1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007 in. (0.178 mm) radius of True Position (TP) at maximum material condition.
3. ϕB applies between L_1 and L_2; ϕB_2 applies between L_2 and 0.500 in. (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500 in. (12.70 mm).
4. Measure from Max. ϕD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

TO-5 Style Packages

For CA3000-Series High-Reliability ICs

T SUFFIX



Notes:

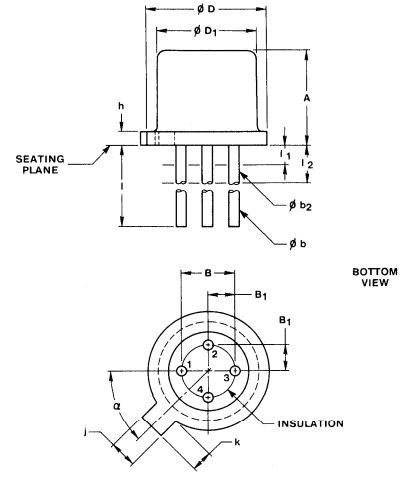
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007 in. (0.178 mm) radius of True Position (TP) at maximum material condition.
3. ϕB applies between L_1 and L_2; ϕB_2 applies between L_2 and 0.500 in. (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500 in. (12.70 mm).
4. Measure from Max. ϕD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

12-Lead
JEDEC Outline MO-006-AG

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
a	0.230 TP		5.84 TP		2
A_1	0	0	0	0	
A_2	0.165	0.185	4.19	4.70	
ϕB	0.016	0.019	0.407	0.482	3
ϕB_1	0	0	0	0	
ϕB_2	0.016	0.021	0.407	0.533	3
ϕD	0.335	0.370	8.51	9.39	
ϕD_1	0.305	0.335	7.75	8.50	
F_1	0.020	0.040	0.51	1.01	
j	0.028	0.034	0.712	0.863	
k	0.029	0.045	0.74	1.14	4
L_1	0	0.050	0	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	30° TP		30° TP		
N	12		12		6
N_1	1		1		5

92CS-19774

JEDEC TO-72 Package
For High-Reliability MOSFETs



Notes:

1. (Four leads). Maximum number leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.
2. (All leads) ϕb_2 applies between l_1 and l_2; ϕb applies between l_2 and 0.500 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.500 in. (12.70 mm) from seating plane.
3. Measured from maximum diameter of the product.
4. Leads having maximum diameter 0.019 in. (0.483 mm) measured in gauging plane 0.054 in. (1.37 mm) + 0.001 in. (0.025 mm) — 0 in. (0 mm) below the seating plane of the product shall be within 0.007 in. (0.178 mm) of their true position relative to a maximum width tab.
5. The product may be measured by direct methods or by gauge.
6. Tab centerline.

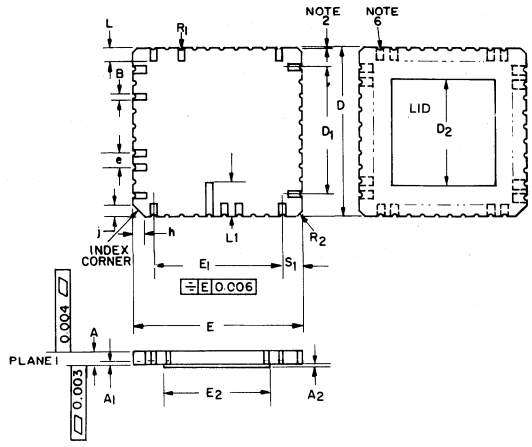
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.210	4.32	5.33	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 TP		2.54 TP		4
e_1	0.050 TP		1.27 TP		4
h	—	0.030	—	0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500	—	12.70	—	2
l_1	—	0.050	—	1.27	2
l_2	0.250	—	6.35	—	2
α	45° TP		45° TP		4, 6

92CS-39728

Leadless-Chip-Carrier Packages

40-Mil Center-to-Center Terminals

(J) SUFFIX



Notes:

1. Metallized corner castellations permissible.
2. Burr permissible on outside edges within dimensions shown.
3. N is the maximum quantity of terminal positions. Refer to terminal numbering convention.
4. Terminals to be centered about notches within ±0.002 in. (0.050 mm).
5. Terminal spacing tolerance is non-cumulative within tolerance limitations of indicated areas.
6. Terminal metallization of edges and opposite side optional.
7. Terminal extended on plane 1 for electrical/optical orientation/handling purposes.
8. Controlling dimension: inch.

24-Terminal Square
JEDEC MS009-AC

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.045	0.075	1.15	1.90	
A_1	0.015	0.030	0.39	0.76	6
A_2	0.010	0.035	0.26	0.88	
B	0.017	0.023	0.432	0.584	4
D	0.345	0.360	8.77	9.14	2
D_1	0.195	0.205	4.96	5.20	
D_2	0.310	0.330	7.88	8.38	
E	0.345	0.360	8.77	9.14	2
E_1	0.195	0.205	4.96	5.20	
E_2	0.310	0.330	7.88	8.38	
e	0.037	0.043	0.940	1.092	
h	0.028 BSC		0.71 BSC		
j	0.028 BSC		0.71 BSC		
L	0.033	0.047	0.84	1.19	
L_1	0.077	0.093	1.96	2.36	7
N	24		24		3
R_1	0.0075 REF		0.19 REF		
R_2	0.0075 REF		0.19 REF		1
S_1	0.070	0.085	1.78	2.15	

92CM-39442

32-Terminal Square
JEDEC MS009-AD

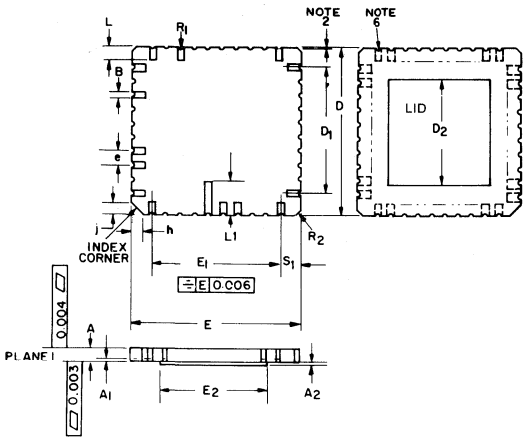
SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.045	0.075	1.15	1.90	
A_1	0.015	0.030	0.39	0.76	6
A_2	0.010	0.035	0.26	0.88	
B	0.017	0.023	0.432	0.584	4
D	0.415	0.430	10.55	10.92	2
D_1	0.275	0.285	6.99	7.23	
D_2	0.370	0.400	9.40	10.16	
E	0.415	0.430	10.55	10.92	2
E_1	0.275	0.285	6.99	7.23	
E_2	0.370	0.400	9.40	10.16	
e	0.037	0.043	0.940	1.092	
h	0.028 BSC		0.71 BSC		
j	0.028 BSC		0.71 BSC		
L	0.033	0.047	0.84	1.19	
L_1	0.077	0.093	1.96	2.36	7
N	32		32		3
R_1	0.0075 REF		0.19 REF		
R_2	0.0075 REF		0.19 REF		1
S_1	0.065	0.080	1.66	2.03	

92CM-34414

Leadless-Chip-Carrier Packages

40-Mil Center-to-Center Terminals

(J) SUFFIX



Notes:

1. Metallized corner castellations permissible.
2. Burr permissible on outside edges within dimensions shown.
3. N is the maximum quantity of terminal positions. Refer to terminal numbering convention.
4. Terminals to be centered about notches within ±0.002 in. (0.050 mm).
5. Terminal spacing tolerance is non-cumulative within tolerance limitations of indicated areas.
6. Terminal metallization of edges and opposite side optional.
7. Terminal extended on plane 1 for electrical/optical orientation/handling purposes.
8. Controlling dimension: inch.

48-Terminal Square
JEDEC MS009-AF

SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.045	0.090	1.15	2.28	
A_1	0.015	0.030	0.39	0.76	6
A_2	0.010	0.035	0.26	0.88	
B	0.017	0.023	0.432	0.584	4
D	0.554	0.572	14.08	14.52	2
D_1	0.435	0.445	11.05	11.30	
D_2	0.500	0.535	12.70	13.58	
E	0.554	0.572	14.08	14.52	2
E_1	0.435	0.445	11.05	11.30	
E_2	0.500	0.535	12.70	13.58	
e	0.037	0.043	0.940	1.092	
h	0.028 BSC		0.71 BSC		
j	0.028 BSC		0.71 BSC		
L	0.033	0.047	0.84	1.19	
L_1	0.077	0.093	1.96	2.36	7
N	48		48		3
R_1	0.0075 REF		0.19 REF		
R_2	0.0075 REF		0.19 REF		1
S_1	0.055	0.070	1.40	1.77	

92CM-34409

64-Terminal Square
JEDEC MS009-AG

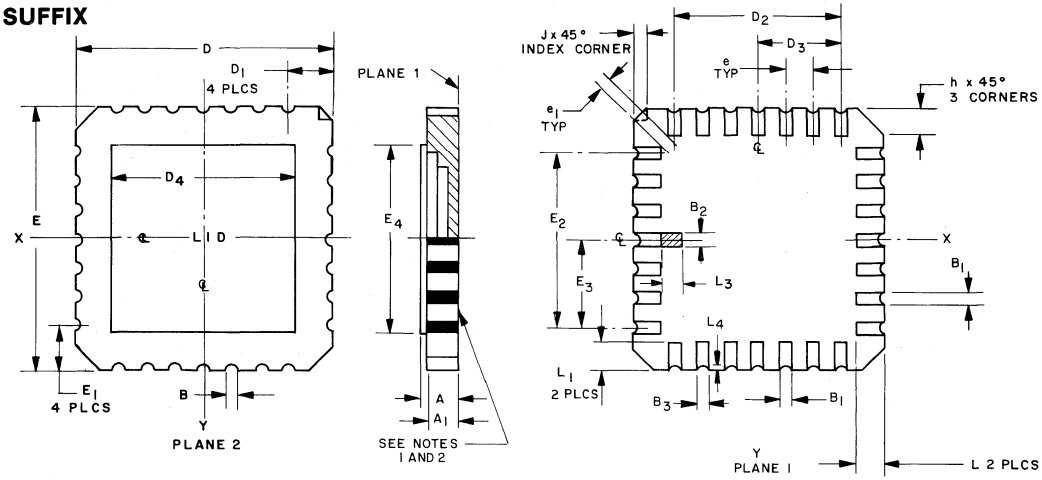
SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.045	0.090	1.15	2.28	
A_1	0.015	0.030	0.39	0.76	6
A_2	0.010	0.035	0.26	0.88	
B	0.017	0.023	0.432	0.584	4
D	0.712	0.733	18.09	18.61	2
D_1	0.594	0.606	15.09	15.39	
D_2	0.600	0.625	15.24	15.87	
E	0.712	0.733	18.09	18.61	2
E_1	0.594	0.606	15.09	15.39	
E_2	0.600	0.625	15.24	15.87	
e	0.037	0.043	0.940	1.092	
h	0.028 BSC		0.71 BSC		
j	0.028 BSC		0.71 BSC		
L	0.033	0.047	0.84	1.19	
L_1	0.077	0.093	1.96	2.36	7
N	64		64		3
R_1	0.0075 REF		0.19 REF		
R_2	0.0075 REF		0.19 REF		1
S_1	0.055	0.070	1.40	1.77	

92CM-34413

Leadless-Chip-Carrier Packages

50-Mil Center-to-Center Terminals

J SUFFIX



Multilayer Construction

92CM-35363R1

MIL-M-38510 Leadless Types C2 and C4 (Generic-Industry Type C)

20-TERMINAL SQUARE
0.350" x 0.350"

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.064	0.100	1.63	2.54	7
A_1	0.054	0.088	1.37	2.24	
B	—	—	—	—	
B_1	0.022	0.028	0.56	0.71	2
B_2	0.022	0.055	0.56	1.40	6
B_3	0.006	0.022	0.15	0.56	9, 10
D	0.342	0.358	8.69	9.09	
D_1	0.075 REF		1.91 REF		
D_2	0.200 REF		5.08 REF		
D_3	0.100 REF		2.54 REF		
D_4	—	0.358	—	9.09	5
E	0.342	0.358	8.69	9.09	
E_1	0.075 REF		1.91 REF		
E_2	0.200 REF		5.08 REF		
E_3	0.100 REF		1.91 REF		
E_4	—	0.358	—	9.09	5
e	0.050 BSC		1.27 BSC		
e_1	0.015	—	0.38	—	3
h	0.040 REF		1.02 REF		
j	0.020 REF		0.508 REF		
L	0.045	0.055	1.14	1.40	
L_1	0.045	0.055	1.14	1.40	
L_3	0.032	0.052	0.81	1.32	6
L_4	0.003	0.015	0.08	0.38	9, 10
N	20		20		4
ND	5		5		4
NE	5		5		4

92CS-39443

28-TERMINAL SQUARE
0.450" x 0.450"

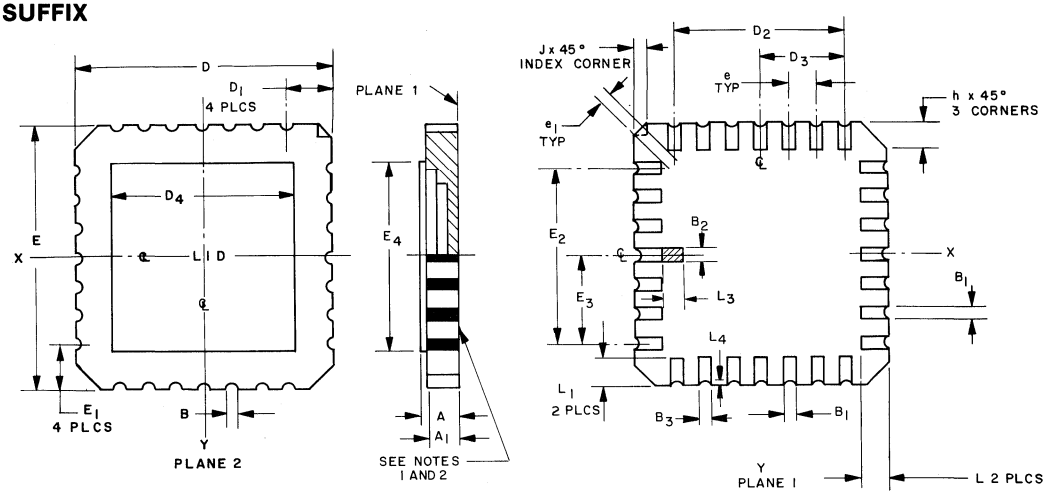
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.064	0.100	1.63	2.54	7
A_1	0.054	0.088	1.37	2.24	
B	—	—	—	—	
B_1	0.022	0.028	0.56	0.71	2
B_2	0.022	0.055	0.56	1.40	6
B_3	0.006	0.022	0.15	0.56	9, 10
D	0.442	0.460	11.23	11.68	
D_1	0.075 REF		1.91 REF		
D_2	0.300 REF		7.62 REF		
D_3	0.150 REF		3.81 REF		
D_4	—	0.460	—	11.68	5
E	0.442	0.460	11.23	11.68	
E_1	0.075 REF		1.91 REF		
E_2	0.300 REF		7.62 REF		
E_3	0.150 REF		3.81 REF		
E_4	—	0.460	—	11.68	5
e	0.050 BSC		1.27 BSC		
e_1	0.015	—	0.38	—	3
h	0.040 REF		1.02 REF		
j	0.020 REF		0.508 REF		
L	0.045	0.055	1.14	1.40	
L_1	0.045	0.055	1.14	1.40	
L_3	0.032	0.052	0.81	1.32	6
L_4	0.003	0.015	0.08	0.38	9, 10
N	28		28		4
ND	7		7		4
NE	7		7		4

92CS-39444

Leadless-Chip-Carrier Packages

50-Mil Center-to-Center Terminals

J SUFFIX



Multilayer Construction

92CM-35363R1

MIL-M-38510 Leadless Type C5 (Generic-Industry Type C)

44-TERMINAL SQUARE CHIP CARRIER, 0.650" x 0.650"

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.064	0.120	1.63	3.05	7
A_1	0.054	0.088	1.37	2.24	
B	0.033	0.039	0.84	0.99	
B_1	0.022	0.028	0.56	0.71	2
B_2	0.022	0.055	0.56	1.40	6
B_3	0.006	0.022	0.15	0.56	9, 10
D	0.640	0.662	16.26	16.81	
D_1	0.075 REF		1.91 REF		
D_2	0.500 REF		12.70 REF		
D_3	0.250 REF		6.35 REF		
D_4	—	0.662	—	16.81	5
E	0.640	0.662	16.26	16.81	
E_1	0.075 REF		1.91 REF		
E_2	0.500 REF		12.70 REF		
E_3	0.250 REF		6.35 REF		
E_4	—	0.662	—	16.81	5
e	0.050 BSC		1.27 BSC		
e_1	0.015	—	0.38	—	3
h	0.040 REF		1.02 REF		
j	0.020 REF		0.508 REF		
L	0.045	0.055	1.14	1.40	
L_1	0.045	0.055	1.14	1.40	
L_3	0.032	0.052	0.81	1.32	6
L_4	0.003	0.015	0.08	0.38	9, 10
N	44		44		4
ND	11		11		4
NE	11		11		4

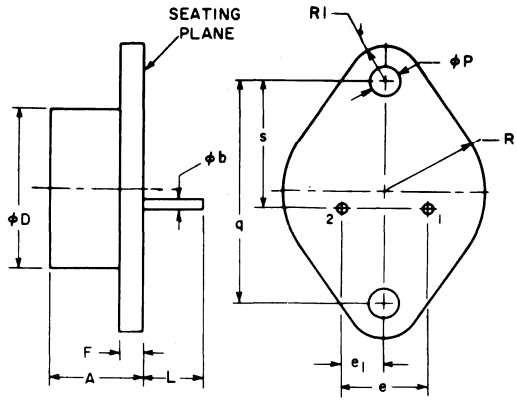
92CS-39445

Notes:

1. Metallized castellations are connected to plane 1 terminals and extend toward plane 2 across at least two layers of the multilayer construction or completely across if plane 2 is metallized. N is measured on plane 1 (see note 2).
2. Electrical connection is required on plane 1. Metallization is optional on plane 2. However, if plane 2 is metallized it must be electrically connected.
3. A minimum clearance of 0.015 in. (0.381 mm) shall be maintained between adjacent terminals.
4. N is the maximum quantity of terminal positions. ND and NE are the numbers of terminals along the sides of length D and E, respectively.
5. A minimum clearance or 0.015 in. (0.38 mm) shall be maintained between a metal lid and other metal features (e.g., plane 2 terminals, metallized castellations, etc.). The lid shall not extend beyond the edges of the body.
6. The index features for No. 1 terminal identification, optional orientation or handling purposes shall be within the shaded area shown on plane 1.
7. Dimension A controls the overall package thickness.
8. Controlling dimension: inch.
9. Dimensions B_3 minimum, L_4 (min.) and the appropriately derived castellation length define an unobstructed 3-dimensional space traversing all the ceramic layers in which a castellation was designed. Dimensions B_3 maximum and L_4 (max.) define the maximum width and depth of the castellation at any point on its surface.
10. Castellations are required on bottom two layers.

Power Device Packages

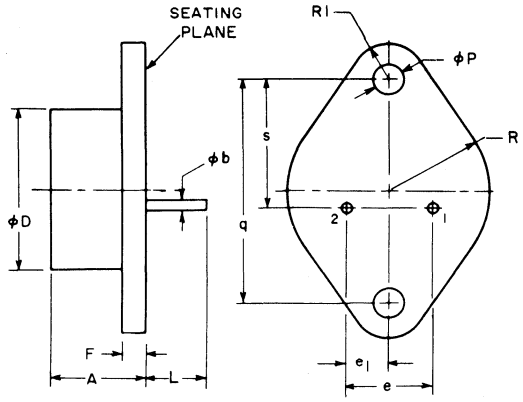
JEDEC TO-204AA



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.4	11.4	
φb	0.038	0.043	0.966	1.092	
φD	—	0.875	—	22.22	
e	0.420	0.440	10.67	11.17	
e_1	0.205	0.225	5.21	5.71	
F	—	0.135	—	3.42	
L	0.312	—	7.93	—	
φP	0.151	0.161	3.84	4.08	
q	1.187 BSC		30.15 BSC		
R	—	0.525	—	13.33	
R_1	—	0.188	—	4.77	
s	0.655	0.675	16.64	17.14	

92CS-37249R1

JEDEC TO-204AE

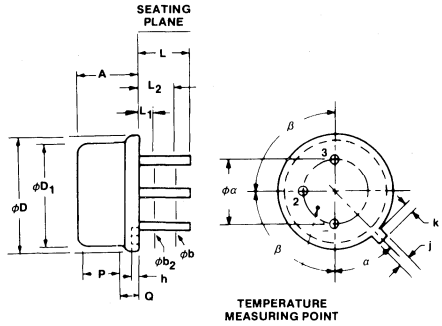


SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.4	11.4	
φb	0.057	0.063	1.45	1.60	
$φD_2$	—	0.875	—	22.22	
e	0.420	0.440	10.67	11.17	
e_1	0.205	0.225	5.21	5.71	
F	0.060	0.135	1.53	3.42	
L	0.440	0.480	11.18	12.19	
φP	0.151	0.161	3.84	4.08	
q	1.187 BSC		30.15 BSC		
R	0.495	0.525	12.58	13.33	
R_1	0.131	0.188	3.33	4.77	
s	0.655	0.675	16.64	17.14	

92CS-36443R2

Power Device Packages

JEDEC TO-205AF



TERMINAL CONNECTIONS
Lead No. 1 - Source
Lead No. 2 - Gate
Lead No. 3 - Drain (connected to case)

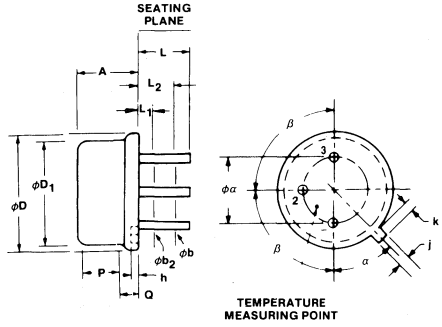
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	0.200 BSC		5.08 BSC		4
A	0.160	0.180	4.07	4.57	
ϕb	0.016	0.021	0.41	0.53	5
ϕb_2	0.016	0.019	0.41	0.48	5
ϕD	0.340	0.370	8.64	9.39	
ϕD_1	0.315	0.355	8.01	9.01	2
h	0.009	0.041	0.23	1.04	
j	0.028	0.034	0.72	0.86	
k	0.029	0.045	0.74	1.14	1
L	0.500	0.750	12.70	19.05	5
L_1	—	0.050	—	1.27	5
L_2	0.250	—	6.35	—	5
P	0.070	—	1.78	—	2
Q	—	0.050	—	1.27	3
α	45° NOMINAL				
β	90° NOMINAL				

92CS-38248R1

Notes:

1. Dimension k measured from ϕD maximum.
2. ϕD_1 shall not vary more than 0.010 in Zone P. This zone controlled for automatic handling.
3. Details of outline in this zone optional.
4. Leads at gauge plane 0.054-0.055 below seating plane shall be within 0.007 radius of positional tolerance at MMC relative to tab at MMC. Device may be measured by direct methods or by gauge and gauging procedure described on JEDEC gauge drawing GS-1.
5. ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and L minimum. Diameter is uncontrolled in L_1 and beyond L minimum.

TO-39



TERMINAL CONNECTIONS
Lead No. 1 - Emitter
Lead No. 2 - Base
Lead No. 3 - Collector (connected to case)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	0.200 BSC		5.08 BSC		4
A	0.240	0.260	6.10	6.60	
ϕb	0.016	0.021	0.41	0.53	5
ϕb_2	0.016	0.019	0.41	0.48	5
ϕD	0.335	0.370	8.51	9.39	
ϕD_1	0.305	0.335	7.75	8.50	2
h	0.009	0.041	0.23	1.04	
j	0.028	0.034	0.72	0.86	
k	0.029	0.045	0.74	1.14	1
L	0.500	0.750	12.70	19.05	5
L_1	—	0.050	—	1.27	5
L_2	0.250	—	6.35	—	5
P	0.100	—	2.54	—	2
Q	—	0.050	—	1.27	3
α	45° NOMINAL				
β	90° NOMINAL				

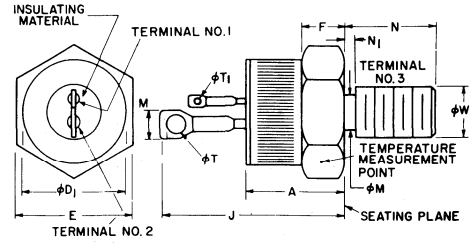
92CS-39772

Notes:

1. Dimension k measured from ϕD maximum.
2. ϕD_1 shall not vary more than 0.010 in Zone P. This zone controlled for automatic handling.
3. Details of outline in this zone optional.
4. Leads at gauge plane 0.054-0.055 below seating plane shall be within 0.007 radius of positional tolerance at MMC relative to tab at MMC. Device may be measured by direct methods or by gauge and gauging procedure described on JEDEC gauge drawing GS-1.
5. ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and L minimum. Diameter is uncontrolled in L_1 and beyond L minimum.

Power Device Packages

TO-48



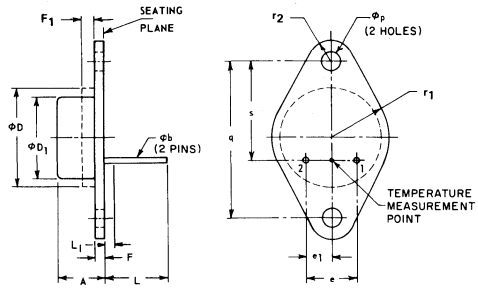
Notes:

1. øW is pitch diameter of coated threads. REF: Screw-Thread Standards for Federal Services, Handbook H28, Part I. Recommended Torque: 35 in.lbf (0.4 kg f-m). Maximum Torque: 50 in-lbf (0.57 kgf-m)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.330	0.505	9.4	12.8	
øD1	—	0.544	—	13.81	
E	0.544	0.562	13.82	14.28	
F	0.113	0.200	2.87	5.08	
J	0.950	1.100	24.13	27.94	
øM	0.220	0.249	5.59	6.32	
M	0.215	0.225	5.46	5.71	
N	0.422	0.453	10.72	11.50	
N1	—	0.090	—	2.28	
øT1	0.058	0.068	1.47	1.73	
øT	0.138	0.148	3.50	3.75	
øW	¼-28	UNF-2A	¼-28	UNF-2A	1

92CS-15208R5

TO-66



Maximum Torque: 12 1bf in. (0.14 kgf m)

Notes:

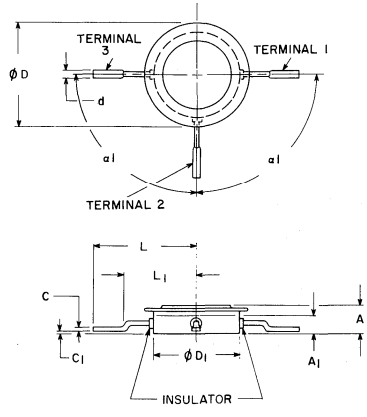
1. Body contour is optional within zone defined by øD and F_2.
2. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gauge is not used, measurements will be made at seating plane.
3. øb applies between L_1 and L. Diameter is uncontrolled in L_1.

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.340	6.35	8.63	
øb	0.028	0.034	0.712	0.863	
øD	—	0.620	—	15.74	1
øD1	0.470	0.500	11.94	12.70	
e	0.190	0.210	4.83	5.33	2
e1	0.093	0.107	2.37	2.71	2
F	0.050	0.075	1.27	1.90	
F1	—	0.050	—	1.27	1
L	0.360	0.500	9.15	12.70	
L1	—	0.050	—	1.27	3
øp	0.142	0.152	3.607	3.860	
q	0.958	0.962	24.334	24.434	
R	—	0.350	—	8.89	
R1	0.115	0.145	2.93	3.68	
s	0.570	0.590	14.48	14.98	

92CM-34147

4. The seating plane of header shall be flat within 0.001 in. (0.025 mm) concave to 0.004 in. (0.10 mm) convex inside a 0.520 in. (13.21 mm) diameter circle on the center of the header and flat within 0.001 in. (0.025 mm) concave to 0.006 in. (0.15 mm) convex overall.

RADIAL PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.200	—	5.08	
A1	—	0.125	—	3.17	1
C	0.015	0.019	0.38	0.48	
C1	—	0.015	—	0.38	
øD	—	0.710	—	18.03	
øD1	0.615	0.690	15.62	17.52	1
d	0.042	0.046	1.06	1.16	
L	—	0.705	—	17.90	
L1	—	0.510	—	12.95	
α1	90° ± 2°		90° ± 2°		

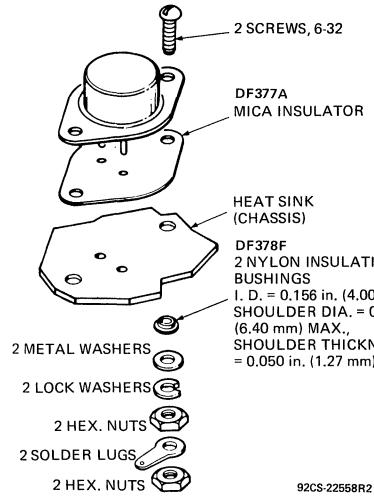
92CS- 20224

Notes:

1. CONTROLLED AREA OF THE DIAMETER DOES NOT INCLUDE THE BRAZED AREA AROUND THE CERAMIC AND TERMINAL 2.

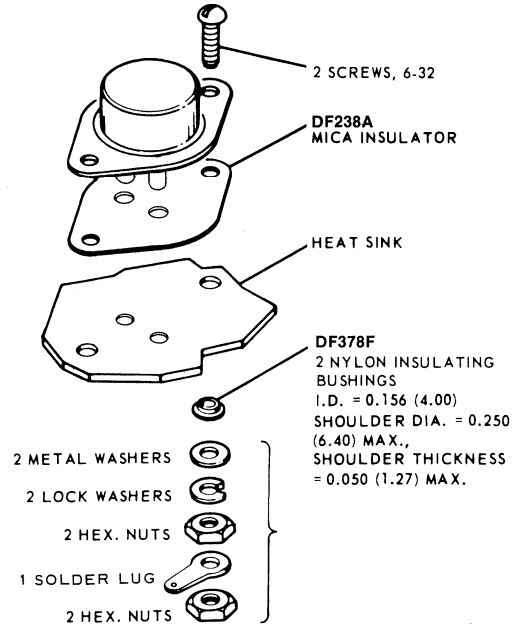
Power Devices Mounting Hardware

JEDEC TO-204AA

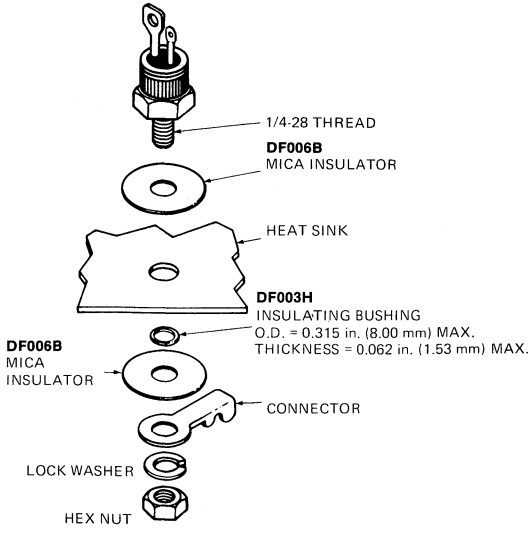


NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING FLANGE IS 12 in.-lbs. (0.14 kgf m).

JEDEC TO-204AE

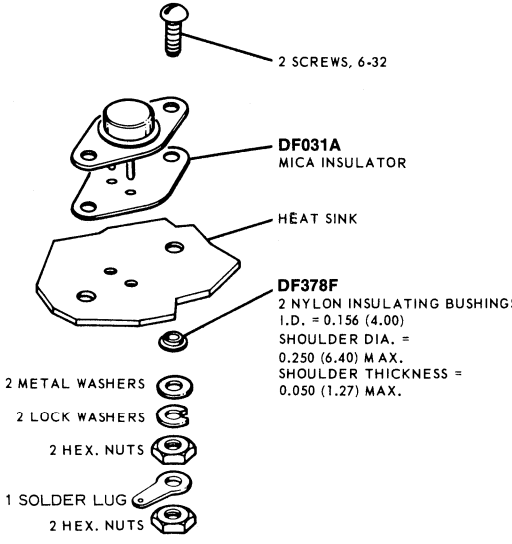


TO-48



Maximum torque: 50 in.-lb (0.58 kgf-m) 92CS-22640R2

TO-66



Note: Maximum torque applied to mounting flange is 12 in.-lb. (0.14 kgfm) 92CS-22560R5

Application Notes

Index to Application Notes

Operating Considerations for RCA Solid-State Devices

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid-state devices.

The ratings included in RCA Solid-State Devices data bulletins are based on the Absolute-Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

> Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid-state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces. For specific information on voltage creepage, the user should consult references such as the JEDEC Standard No. 7 "Suggested Standard on Thyristors," and JEDEC Standard RS282 "Standards for Silicon Rectifier Diodes and Stacks".

The metal shells of some solid-state devices operate at the collector voltage and for some rectifiers and thyristors at the anode voltage. Similarly, the TO-5-style package often used for integrated circuits usually has the substrate or most negative supply voltage connected to the case. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device and result in destruction and/or possible shattering of the enclosure.

TRANSISTORS AND THYRISTORS WITH MOUNTING FLANGES

The mounting flanges of JEDEC-type packages such as the TO-3 or TO-66 often serve as the collector or anode terminal. In such cases, for the electrical connection, but more importantly for conduction of the heat generated, it is essential that the mounting flange be securely fastened to the heat sink, which may be the equipment chassis. Soldering is the preferred method for mounting. The package may be soldered to the heat sink by use of lead-tin solder, however a solder with a lower melting point than the 95/5 lead/tin solder used for assembly should be used. The soldering process should be carefully controlled to prevent permanent damage to the device. Devices which cannot be soldered can be installed in commercially available sockets. Electrical connections may also be made by soldering directly to the terminal pins. Such connections may be soldered to the pins close to the pin seals provided care is taken to conduct excessive heat away from the seals; otherwise the heat of the soldering operation could crack the pin seals and damage the device.

During operation, the mounting-flange temperature is higher than the ambient temperature by an amount which depends on the heat sink used. The heat sink must have sufficient thermal capacity to assure that the heat dissipated in the heat sink itself does not raise the device mounting-flange temperature above the rated value. The heat sink or chassis may be connected to either the positive or negative supply.

In many applications the chassis is connected to the voltage-supply terminal. If the recommended mounting hardware shown in the data bulletin for the specific solid-state device is not available, it is necessary to use either an anodized aluminum insulator having high thermal conductivity or a mica insulator between the mounting-flange and the chassis. If an insulating aluminum washer is required, it should be drilled or punched to provide the two mounting holes for the terminal pins. The burrs should then be removed from the washer and the washer anodized. To

insure that the anodized insulating layer is not destroyed during mounting, it is necessary to remove the burrs from the holes in the chassis.

It is also important that an insulating bushing, such as glass-filled nylon, be used between each mounting bolt and the chassis to prevent a short circuit. However, the insulating bushing should not exhibit shrinkage or softening under the operating temperatures encountered. Otherwise the thermal resistance at the interface between device and heat sink may increase as a result of decreasing pressure.

PLASTIC POWER TRANSISTORS AND THYRISTORS

RCA power transistors and thyristors (SCRs and triacs) in molded-epoxy-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations. The following paragraphs provide guidelines for handling and mounting of these plastic-package devices, recommend forming of leads to meet specific mounting requirements, and describe various mounting arrangements, thermal considerations, and cleaning methods. This information is intended to augment the data on electrical characteristics, safe operating area, and performance capabilities in the technical bulletin for each type of plastic-package transistor or thyristor.

Lead-Forming Techniques

The leads of the RCA VERSAWATT and VERSATAB in-line plastic packages can be formed to a custom shape, provided they are not indiscriminately twisted or bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping.

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. When the use of a properly designed fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case.

When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least ⅛ inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

The leads of the TO-220AB VERSAWATT and TO-202 VERSATAB in-line packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should be devised.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed. The maximum soldering temperature, however, must not exceed 235° C. The soldering instrument must be at least 1/8 inch from the device and must not be applied for more than 10 seconds. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

The leads of RCA molded-plastic packages are not designed to be reshaped. However, simple bending of the leads is permitted to change them from a standard vertical to a standard horizontal configuration, or conversely. Bending of the leads in this manner is restricted to three 90-degree bends; repeated bendings should be avoided.

Mounting

TO-220. Recommended mounting arrangements and suggested hardware for the VERSAWATT package are given in the data bulletins for specific devices and in RCA Application Note AN-4124. When the package is fastened to a heat sink, a rectangular washer (RCA Part No. NR231A) is recommended to minimize distortion of the mounting flange. Excessive distortion of the flange could cause damage to the package. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch.

Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is specified. Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body. The material used for such a spacer or spacer-isolating bushing should, of course, be carefully selected to avoid "cold flow" and consequent reduction in mounting force. Suggested materials for these bushings are diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided. Damage to the device can also result from the use of a non-flat mounting surface. This surface should be flat within 0.002 inch from the mounting hole to either side of the TO-220 device.

Modification of the flange can also result in flange distortion and should not be attempted. The package may be soldered to the heat sink by use of lead-tin solder, however this solder should have a lower melting point than the 95/5 lead/tin solder used for assembly. The soldering process should be carefully controlled to prevent permanent damage to the device.

The TO-220AA plastic package can be mounted in commercially available TO-66 sockets, such as UID Electronics Corp. Socket No. PTD-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. DC74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:

1. Use appropriate hardware.
2. Always fasten the package to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.
4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings to prevent hot-creep problems. Such bushings should be made of diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate.

TO-3. The high power-handling capability of the TO-3 package requires the use of very large silicon die. Large die are susceptible to damage when the TO-3 package is fastened to a non-flat surface, or when unequal torque is applied during mounting.

When mounting a TO-3 device, the following precautions must be observed to avoid internal damage to the device:

1. The mounting surface should be flat within 0.007 inch.
2. **Both** mounting screws should be tightened lightly to 2 inch-pounds **first**, and then to no more than 12 inch-pounds.
3. The use of impact wrenches is not recommended.
4. Care should be exercised with thermal greases to avoid an increase in viscosity and the formation of lumps as a result of excessive exposure to air prior to application. These conditions will place additional stress on the device during mounting.

Thermal Considerations

The maximum allowable power dissipation in a solid-state device is limited by the junction temperature. An important factor in assuring that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid-state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data for the device. Thermal considerations require that a free flow of air around the device is always present and that the power dissipation be maintained below the level which would cause the junction temperature to rise above the maximum rating. However, when the device is mounted on a heat sink, care must be taken to assure that all portions of the thermal circuit are considered.

To assure efficient heat transfer from case to heat sink when mounting RCA molded-plastic solid-state power devices, the following special precautions should be observed:

1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept as small as possible.
3. Holes should be drilled or punched clean with no burrs or ridges, and chamfered to a maximum radius of 0.010 inch.
4. The mounting surface should be flat within 0.002 inch/inch.
5. Thermal grease (Dow Corning 340 or equivalent) should always be used on both sides of the insulating washer if one is employed.
   Note: Silicone-oil fluids that come into direct physical contact with silicone-molded transistors may react chemically with and cause damage to the packages. These silicone oils are commonly formulated into thermal-grease heat-transfer compounds. Selection of these greases is therefore critical and based on the bleed rate of the oil from the grease. For example, in mounting arrangements that employ an insulating washer, a thermal-grease heat-sink compound, such as Dow Corning No. 340 or equivalent, for which the bleed rate does not exceed 0.5 per cent after 24 hours of 200° C is recommended for use on both sides of the insulating washer.
6. Thin insulating washers should be used. (Thickness of factory-supplied mica washers ranges from 2 to 4 mils).
7. A lock washer or torque washer, made of material having sufficient creep strength, should be used to prevent degradation of heat sink efficiency during life.

Cleaning After Mounting

A wide variety of chemicals and solvents is available for fluxing, degreasing, and flux removal. Care must be exercised in the selection of materials, such that from a reliability standpoint, there is no adverse effect on component life. A major contributor, effecting device reliability, is the chemical reaction of chloride with the aluminum metallization of the die. Eventually this etching process will result in electrical open circuits. The mechanism is defined as Electrolytic Metal Attack (EMA) and is accelerated in a moisture environment. Cleaning and fluxing compounds free of chloride will therefore maximize device life. Chloride is defined as the dissociated ion, which is soluble in water, as contrasted to the water insoluble organic chlorine of compounds such as perchloroethylene and trichloroethane. It is, of course, impractical to evaluate the long-term effect on semiconductor life of all chemicals which are marketed under a variety of brand names.

The choice of fluxes for electronic applications should be restricted to rosin types, R, RMA and RA and water soluble organic acid, OA, formulations. Inorganic acid fluxes should not be used as they can attack the internal metallization of the semiconductor. As stated above, it is further recommended, where applicable, that non-halide type fluxes be used for improved device reliability. Some examples of acceptable fluxes are:

A. Rosin Types (RA)
   Alpha 711
   Alpha 809 foam flux
   Alpha 811 foam flux
   Alpha 815 foam flux
   Alpha TL33M halide free
B. Water soluble organic acid (OA) types, halide free
   Blackstone 1452
   Kenco 183
   Alpha 260HF and 265HF

Since circuit boards can fall into several categories, such as single sided, double sided with plated-through holes and densely populated multilayer types, it must be stressed that the manufacturer's recommendation be considered when choosing the proper flux for the process being used.

Flux cleaning and/or degreasing is necessary to assure that the final soldered assembly is free of contaminating soils. The choice of the cleaning system is relative to the soil being removed. Water-based cleaners are generally used to remove polar soils, such as rosin activators, organic acid residues, and finger salts. Solvent cleaners are chosen for removal of organic (non-polar) contaminants, which include rosins, oils, and greases. Cleaning methods can incorporate immersion (with or without ultrasonics), brushing, and spraying. The choice of cleaner should be based on affinity for the contaminant, ability to thoroughly wet the parts, and compatibility with components. It should also be safe to use.

Solvent cleaners are generally divided into two classes: chlorinated and fluorinated. These can be used for cleaning rosin-activated (RA) fluxes. The chlorinated solvents are more aggressive and care must be taken to assure there is no damage to components or substrate. This type solvent should not be used with silicone-encapsulated transistors as the solvent will tend to dissolve the plastic. The use of chlorinated solvents must be closely monitored because of a breakdown to form acid components in the presence of moisture. The solvent should be checked regularly and discarded when acid levels exceed manufacturer's guidelines. Fluorinated solvents are normally blends of trifluorotrichloroethane with other solvents, such as: methanol,

ethanol, isopropanol, acetone, methylene chloride, or chloroform. These solvents can be purchased under trade names as Freon TE, TE35, TP35, Frigen 113 TR-M, Haltron 113 MOM, and Flugene 113 MA. Fluorinated systems are milder acting and are used in vapor degreasing systems at the boiling point of the solvent mixture.

The solvents may be used for a maximum of 4 hours at 25° C or for a maximum of 1 hour at 50° C.

Rosin fluxes can be removed by either solvent or aqueous cleaners. The water systems contain an additive that reacts with the rosin acids to convert the acids to a water-soluble biodegradable soap. Water-soluble organic-acid fluxes may require the use of a neutralizer to accelerate the solubility of the acid residues and neutralize any residues that may remain. Alcohols are acceptable solvents for rosin-based flux removal; but because of flammability concerns, the fluorinated alcohol blends are preferred. Examples of suitable alcohols are methanol, isopropanol, and special denatured ethyl alcohols, such as SDA1, SDA30, SDA34, and SDA44.

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and physical standpoint.

RECTIFIERS AND THYRISTORS

A surge-limiting impedance should always be used in series with silicon rectifiers and thyristors. The impedance value must be sufficient to limit the surge current to the value specified under the maximum ratings. This impedance may be provided by the power transformer winding, or by an external resistor or choke.

A very efficient method for mounting thyristors utilizing the TO-205AF package is to provide intimate contact between the heat sink and at least one half of the base of the device opposite the leads. This package can be mounted to the heat sink mechanically with glue or an epoxy adhesive, or by soldering, the most efficient method.

The use of a "self-jigging" arrangement and a solder preform is recommended. If each unit is soldered individually, the heat source should be held on the heat sink and the solder on the unit. Heat should be applied only long enough to permit solder to flow freely. For more detailed thyristor mounting considerations, refer to Application Note AN-3822, "Thermal Considerations in Mounting of RCA Thyristors".

MOS FIELD-EFFECT TRANSISTORS

Small-Signal and Power MOSFETs

Insulated-Gate Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in a MOSFET if a type with an unprotected gate is picked up and the static charge on the handler's body allowed to discharge through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOSFETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOSFETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

Power MOSFETs

In addition to the above basic precautions, the following precautions should be taken for safe handling of Power MOSFETs:

1. Gate Voltage Rating — Never exceed the gate-voltage rating of ±20 V.* Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.
2. Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.
3. Gate Protection — These devices do not have an internal monolithic zener diodes connected from gate to source. If gate protection is required an external zener is recommended.

INTEGRATED CIRCUITS

Mounting

Integrated circuits are normally supplied with tin-lead dipped leads to facilitate soldering into circuit boards.

When integrated circuits are welded onto printed-circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. When solder-dipped leads are formed, they must be reflowed or redipped within 40 mils of the package body. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

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*Trade Name: Emerson and Cumming, Inc.

*±10 V for logic-level MOSFETs.

CMOS INTEGRATED CIRCUITS

Handling

All CMOS gate inputs have a diode or resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces protect CMOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. It is recommended that ionizers be used in the handling and assembly areas to minimize damage from electrostatic discharge (ESD). See ICAN-6525, "Handling and Operating Considerations for MOS Integrated Circuits", for proper handling procedures.

Operating

Unused Inputs

All unused input leads must be connected to either the low rail (V_{SS}, V_{EE}, or GND) or the high rail (V_{CC} or V_{DD}), whichever is appropriate for the logic circuit involved. A floating input on a high-current type such as the CD4049 or CD4050, operating at a supply voltage above 5 V, not only can result in faulty logic operation, but can cause the maximum-rated power dissipation to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to the high or low voltage supply rails. A useful range of values for such resistors is from 10 kilohms to 1 megohm. Pins that are I/O must have a terminating resistor.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady-state value of less than the absolute-maximum rating. This value is either 10 mA or 20 mA depending on device family. Input currents of less than the maximum rating prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

Output Short Circuits

Shorting of outputs to the high or low supply rail can damage many of the higher-output-current CMOS types, such as the CD4007, CD4041, CD4049, and CD4050. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For the QMOS HC/HCT/HCU types, outputs may be shorted to V_{CC} (5 V ± 10%) for 1 second maximum and only one output at a time. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below the device maximum-rated output power.

For detailed CMOS IC operating and handling considerations, refer to Application Note ICAN-6525 "Handling and Operating Considerations for MOS Integrated Circuits".

CMOS Power-Supply Distribution and Decoupling

Power distribution should be a prime consideration in all CMOS designs. Although DC power dissipation is very low, dynamic power (due to switching transients) can be high. High-voltage and/or low-temperature operation increase dynamic current transients.

A low-impedance power source and supply-to-ground capacitance bypass placed near each device will significantly reduce noise generation on signal and power lines; system reliability is greatly changed.

Decoupling

Higher speeds, faster edges and higher output-drive currents cause higher-frequency current transients to be imposed on ground and V_{CC} rails of an IC. For LSI, HC, and HCT families, consideration of power-supply distribution and decoupling become important. Before decoupling can be utilized for noise reduction, there must first be a good power-supply distribution network. A good ground connection system and capacitive decoupling must be employed. For details refer to Application Note ICAN-7329, "Power-Supply Distribution and Decoupling for QMOS High-Speed-Logic ICs".

LINEAR INTEGRATED CIRCUITS

BIMOS, BIPOLAR AND CMOS

In linear integrated circuits that employ diode-isolation techniques, there are numerous parasitic devices associated with the primary circuit components. These devices may be activated or turned on by driving inputs and/or outputs beyond the supply-voltage range of the integrated circuit. For example, externally driving the collector terminal of a transistor array below the isolation or substrate potential will forward bias the parasitic isolation diode shown in Fig. 1. Since the collector region and substrate form a comparatively large-area diode, high currents will be sustained, often at levels sufficiently high to melt the metallization to these devices.

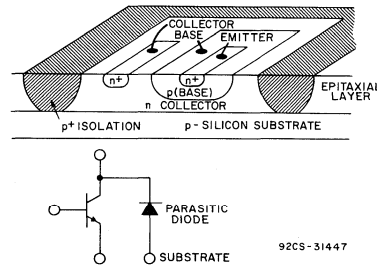

Fig. 1 - Sectional view of conventional "vertical" n-p-n transistor commonly used on IC chip. Also shown is the equivalent circuit and associated parasitic diode.

Operational amplifiers like the 741, and other similar structures, can be damaged by driving a positive-going signal into the input device with power off. The signal will forward bias the collector-to-base junction of the input transistor and, if the positive supply impedance is low enough, drive current back into the supply. Current above the maximum rating may result in damage to the amplifier.

Supply transients are another possible source of damage. They can activate or trigger parasitic SCR devices which can cause an integrated circuit to draw extremely high current. If the supply impedance is sufficiently high, the SCR gate drive in the latched condition is removed by the limiting action of the supply. If the supply impedance is too low, the device will continue to demand high currents until the metallization of either the device or the printed-circuit board fuses open.

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Although device manufacturers take precautions to keep the number of these parasitic devices at a minimum, normal device process variations occasionally make the formation of parasitic devices inevitable. It is essential, therefore, that the user take precautions to insure that an integrated circuit is never operated beyond its maximum ratings, even under momentary transient conditions.

SOLID-STATE CHIPS

Solid-state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special-handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40° C
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. MOS chips that are ESD-sensitive should be handled in an environment where ionizers are employed.
4. During mounting and lead bonding of chips, the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
5. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmospheres which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

Guide to Better Handling and Operation of CMOS Integrated Circuits

by J. Flood and H. L. Pujol

This Note recommends specific handling and operating practices that minimize the probability of damage to CMOS integrated circuits in the manufacturing operation and the field environment.

A description of various gate-oxide networks that protect against electrostatic discharge in both A-series and B-series RCA COS/MOS product is provided. A practical explanation of the SCR latch-up mechanism and its associated failure mode is given. In addition, operating procedures that help prevent device malfunction are described.

HANDLING CONSIDERATIONS

All CMOS devices are susceptible to damage by the discharge of electrostatic energy between any two pins. The gate input is equivalent to a small, low-leakage capacitor (5 picofarads typical) in parallel with a very high resistance (10^{12} ohms typical). This extremely high input impedance lends itself readily to the buildup of electrostatic charges. Therefore, because the gate-oxide breakdown of a CMOS device is typically 80 volts, damage by high levels of electrostatic discharge can occur.

To protect the gate oxide against high levels of electrostatic discharge, protective networks are implemented on all RCA CMOS (COS/MOS) devices, as described below.

Standard Protection Networks

Fig. 1 shows the standard protection network incorporated on all A-series devices and some B-series devices. Input-diode D_2 is a distributed resistor-diode network that appears as two diodes to V_{DD}.

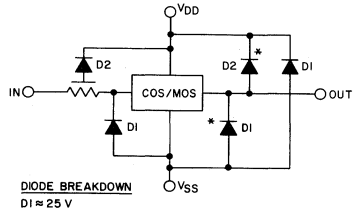


Fig. 1 – Standard protection network.

Improved Protection Network

Fig. 2 shows the improved protection network incorporated on all new B-series devices as well as on all A-series, B-converted types.

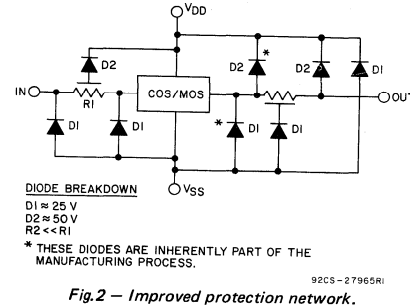


Fig. 2 – Improved protection network.

Other Protective Networks

Fig. 3 shows the modified protective network for a CD4049/4050 buffer. The input diode to V_{DD} is not incorporated so that the level-shifting function can occur.

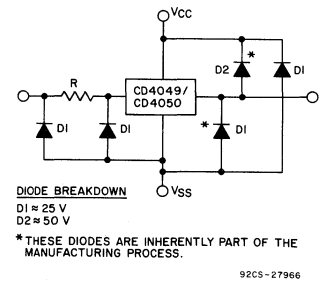


Fig. 3 – Modified protection network.

Fig. 4 shows a transmission gate with the intrinsic diodes that protect against electrostatic discharge.

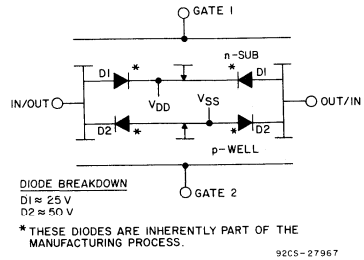


Fig.4 – Transmission gate with intrinsic diodes that protect against electrostatic discharge.

The protection networks described in this Note were characterized by using the equivalent body discharge network of Fig. 5. There are 12 possible combinations by which a device can be damaged. A discussion of the combinations is beyond the scope of

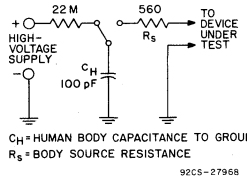


Fig.5 – Equivalent-body discharge network.

this Note; however, Table I shows worst-case protection levels for the above networks. Additional protection can be obtained by adding external series resistors at device inputs. The value of this resistance should be 10 kilohms for gate inputs and 1 kilohm for transmission gate inputs, where applicable. In addition, zener diodes at the output pins can clamp the voltage at a safe level. The zener value should not exceed the absolute maximum rating of the part.

On-chip protection networks are not used on transmission gates to maintain low on resistance. The 800-volt worst case capability is provided by the intrinsic diodes shown in Fig. 4.

TABLE I – Worst-Case Capability of Protective Networks

Protective Network	Worst-Case Capability
Standard (inc. CD4049, CD4050)	1 kV to 2 kV
Improved	4 kV
Transmission Gate	< 800 V

General Handling Rules

Table I indicates the typical, worst-case voltage levels that the above networks can withstand. Because every manufacturing environment is different, levels above those shown in Table I should be anticipated and protected against by following the handling recommendations of Table II.

Basic protection starts with personnel and materials all at the same or ground potential.

Dry weather (relative humidity less than 30 percent) tends to multiply the accumulation of static charges on any surface. Conversely, higher humidity levels (40 to 50 percent) tend to reduce the magnitude of the static voltage generated. In a low-humidity environment, the handling precautions listed above take on added importance and should be adhered to without exception.

HANDLING OF UNMOUNTED CHIPS

In handling unmounted chips, differences in voltage potential should be avoided. A conductive carrier or a carrier having a conductive overlay should be used. Another important consideration is the sequence in which bonds are made; the V_{DD} (device supply) connection should always be made before the V_{SS} (ground) bond.

HANDLING OF SUBASSEMBLY BOARDS

After COS/MOS units have been mounted on circuit boards, proper handling precautions should still be observed. Until these subassemblies are inserted into a complete system in which the proper voltages are applied, the board is no more than an extension of the leads of the device mounted on the board.

It is good practice to put conductive clips or conductive tape on the circuit-board terminals. This precaution prevents static charges from being transmitted through the board wiring to the devices mounted on it.

AUTOMATIC HANDLING EQUIPMENT

When automatic handling equipment is used, it may not always be possible to eliminate static electricity through grounding techniques alone. Automatic feed mechanisms must be insulated from the devices under test at the point where the devices are connected to the test set. The anvil transport portion of the automatic handling mechanism can generate very high levels of static electricity as a result of the continuous flow of devices over and then separating from the anvil. Total control of these static voltages is critical because of the high throughputs associated with automatic handling.

Fortunately, the resolution of this problem is simple, practical, and inexpensive. Ionized-air blowers, which supply large volumes of ionized air to objects that are to be charge neutralized, are commercially available from many supply sources. Field experience with ionized-air techniques reveals this method to be extremely effective in eliminating static electricity when grounding techniques cannot be used.

TABLE II – General Handling Recommendations

	Should be conductive	Should be grounded to common point
Handling equipment	X	
Metal Parts of Fixtures and Tools		X
Handling Trays	X	
Soldering Irons		X
Table Tops	X	X
Transport Carts	X	
Manufacturing Operating Personnel		Utilize grounded, metal or conductive plastic wrist straps with 1-megohm series resistor
General Handling of Devices		Utilize grounded, metal or conductive plastic wrist straps with 1-megohm series resistor

Failure Mechanisms

Electrical damage resulting from handling is usually caused by either of the two following failure mechanisms:

1. Low-level static electricity (voltage of 1 kV to 4 kV). Input diode protection may be overstressed and input leakage currents as high as 1 milliampere across diodes may cause a malfunction.
2. High-level static electricity (voltages greater than 4 kV). Gate oxides may become short-circuited. Inputs to V_{DD} or V_{SS} terminals will be low-impedance inputs.

The presence of these types of device malfunction can be detected by curve-tracer checks of the input protection diodes described above. Diode degradation resulting from static electricity is observable in the low-reverse-breakdown characteristics shown on the curve tracer. On the other hand, damage resulting from high levels of static electricity are observed as a resistive short to V_{DD} or V_{SS}.

Typical Manufacturing Area Procedure

The example below illustrates all of the above recommendations for handling CMOS devices in a typical manufacturing environment. Although existing protective networks offer a high level of protection against electrostatic discharge, this example emphasizes specific precautions that can help eliminate damage.

Receiving Area

Devices should not be removed from their conductive or antistatic carriers. If devices are not received in conductive or antistatic packing material, they should be returned to the supplier.

Incoming Inspection

Physical – Parts should be counted without removing them from their containers.

Storage – Devices should remain in carriers. Even a partial removal of IC's from a carrier should only be done by a grounded operator. Devices removed should be placed in a conductive tray.

Electrical – All testing should be performed by a grounded operator. Devices should be reinserted in conductive carriers after completion of a test.

PC Board Assembly

It is desirable that PC boards have shorting bars installed prior to assembly (soldering). Where possible, CMOS IC's should be the last component installed on the PC board.

Boards should be transported to the wave-solder area in conductive carriers. Flux removal should be done with an acceptable solvent. Examples of specific, acceptable alcohols are isopropanol, methanol and special denatured alcohols such as SDAI, SDA30, SDA34 and SDA44. The removal of flux from non-hermetic and molded-plastic devices by means of soap and water in a dishwasher is NOT recommended as this procedure will adversely affect the long-term life of the device.

OPERATING CONSIDERATIONS

Proper operating procedures are as important as proper handling techniques. A review of RCA COS/MOS A-series and B-series operating characteristics and ratings is given in Table III.

Operating Voltage

When devices are operated near the maximum supply-voltage range, power-supply turn-on or turn-off transients, power-supply ripple or regulation, and ground noise should be suppressed; any of the above conditions must not cause ($V_{DD} - V_{SS}$) to exceed the absolute maximum rating. A good practice is to use a zener protection diode in parallel with the power bus. The zener value should be above the expected maximum regulation

TABLE III – Maximum Ratings of RCA COS/MOS Devices (Voltages referenced to V_{SS})

DC Supply Voltage Range	3 to 15 V (A Series); 3 to 20 V (B Series)
Recommended Operating Voltage	3 to 12 V (A Series); 3 to 18 V (B Series)
DC Input Voltage Range	-0.5 to V_{DD} + 0.5 V
Dissipation per Package	500 mW
Device Dissipation per Output Transistor	100 mW
Storage Temperature Range	-65 to $+150^{o}C$
Operating Temperature Range	
Ceramic Package Types	-55 to $+125^{o}C$
Plastic Package Types	-40 to $+85^{o}C$
Lead Temperature (during soldering) at a distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+ $265^{o}C$

excursion, but should not exceed the maximum supply voltage. Fig. 6 illustrates a practical zener shunt circuit. A current-limiting resistor is included if the supply-current compliance is higher than the zener power-dissipation rating for a given zener voltage. The shunt capacitor value is chosen to supply required peak-current switching transients.

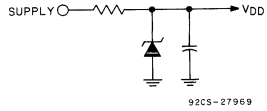


Fig.6 – Zener-diode short circuit.

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current type (such as the CD4009A, CD4010A, CD4041A, CD4049A, CD4050A) can result not only in faulty logic operation, but can cause the maximum power dissipation of 500 milliwatts to be exceeded; the result may be damage to the device. Another consideration with high-current devices is the need for a pull-up resistor between the inputs and V_{SS} or V_{DD} should there be any possibility that the device terminals may become temporarily open or unconnected (e.g., if the printed circuit board driving the high-current types is removed from the chassis). A useful range of values for such resistors is from 0.2 to 1 megohm.

Input Signals

Signals should not be applied to the inputs while the device power supply is off unless the input current is limited to a steady-state value of typically less than 10 milliamperes. Input-signal interfaces that are the allowable 0.5 volt above V_{DD} or below V_{SS} should be current-limited to typically 10 milliamperes or less.

Whenever the possibility of exceeding 10 milliamperes of input current exists, a resistor in series with the input is recommended. The value of this resistor can be as high as 10 kilohms without affecting static electrical characteristics. However, speed will be reduced because of the added RC delay. Particular attention should be given to long input-signal lines where high inductance can increase the likelihood of large-signal pickup in noisy environments. In these cases, series resistance with shunt capacitance at the IC input terminals is recommended. The shunt capacitance should be made as large as possible consistent with the system speed requirements.

Fan-Out – COS/MOS to COS/MOS

All RCA COS/MOS devices have a dc fan-out capability of greater than 50. The reduction in COS/MOS switching speed caused by added capacitive loading should, however, be consistent with high-speed system design. The input capacitance is typically 5 picofarads for most types; the CD4009 and CD4049 buffers have a typical input capacitance of 15 picofarads.

Maximum Clock Rise and Fall Time

All COS/MOS clocked devices show maximum clock rise- and fall-time ratings (normally 5 to 15 microseconds). With longer rise or fall times, a device may not function properly.

Parallel Clocking

When two or more different CMOS devices use a common clock, the clock rise time must be kept at a value less than the sum of the propagation delay time, the output transition time, and the setup time. Most flip-flop and shift-register types are included in this rule and are so noted in the individual data sheets.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can cause the device power dissipation to exceed the safe value of 500 milliwatts. In general, outputs of these types can all be safely shorted when the device is operated with $(V_{DD} - V_{SS}) \leq 5$ volts, but the 500 milliwatt dissipation ratings may be exceeded at higher power-supply voltages. For cases in which a short-circuited load, such as the base of a p-n-p or n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for safe operation below 500 milliwatts. Note that a single output transistor short must be limited to 100 milliwatts.

SCR Latch-Up

Operation above maximum ratings can force CMOS devices into a p-n-p-n SCR "latch-up" mechanism, which can be destructive. Any transients should be avoided and any large loads occurring during operation near the maximum rating should be avoided.

"Latch-up" is considered to be the creation of a low-resistance path between the power supply and ground on a circuit during an electrical pulse; the path remains a low-resistance path after the pulse. In CMOS circuits, several parasitic bipolar transistors exist, as shown in Fig. 7. The p-n-p transistor

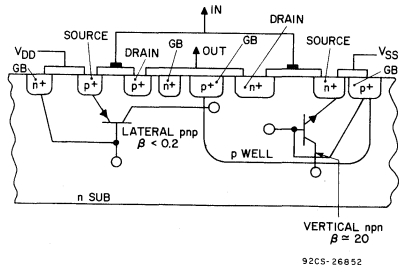


Fig.7 – Parasitic bipolar transistors in CMOS circuits.

is a wide-base lateral structure whose β, normally less than 0.2, is a function of device geometry. The conditions for SCR turn-on are as follows:

1. β n-p-n x β p-n-p ≥ 1
   (vert.) (lat.)
2. The lateral p-n-p and vertical n-p-n base emitter junctions are forward biased.
3. The bias circuit that applies power to V_{DD} and to the input must be capable of supplying current equal to the holding current of potential SCR's.

Fig. 8 shows the equivalent circuit for the SCR structure present in CMOS circuits.

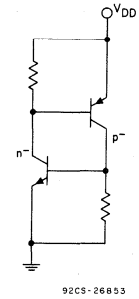


Fig.8 – Equivalent circuit for the SCR structure present in CMOS circuits.

Fig. 9 shows a curve of I_{DD} as a function of V_{DD}, which illustrates the effect of secondary breakdown and SCR latch-up.

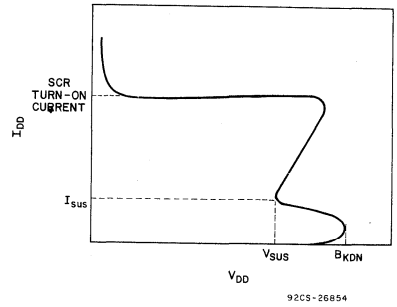


Fig.9 – Curve illustrating effect of secondary breakdown and SCR latch-up.

Table IV shows typical values of breakdown voltage and sustaining voltage and current for RCA COS/MOS A-series and and B-series devices. The table shows that B-series devices are much harder to latch than A-series types because of the higher breakdown voltage.

TABLE IV – Breakdown Voltage and Sustaining Voltage and Current Values

Characteristic	A-Series	B-Series
$V_{BKDN_{min}}$	17 V	25 V
V_{sus}	15 V	22 V
I_{sus}	Type-Dependent 2–40 mA	50–100 mA

ICAN-6532

Fundamentals of Testing COS/MOS Integrated Circuits

by J. Flood

This Note describes the techniques employed in testing RCA COS/MOS devices to assure their adherence to data-sheet specifications, and provides information useful in data-sheet interpretation and in the inspection of incoming devices. RCA COS/MOS devices are available in two basic families: A-series (3- to 15-volt product) and B-series (3- to 20-volt product).

RCA COS/MOS circuits are 100-percent tested by circuit probe in the wafer stage and are 100-percent tested again after they have been packaged. DC tests of RCA devices are performed at 5, 10, 15, and 20 volts; functionality is checked at 3, 17, and 22 volts depending on family (i.e., A or B series). Sample testing is used to assure adherence to quality requirements and ac specifications.

Static tests, high-speed functional and dc parametric tests, are performed at wafer and package stages by means of a Teradyne J283 test set. A Teradyne S157CM test set and a Macrodata MD154 test set are used in dynamic testing. Dynamic tests are performed with 15 and 50 picofarad loads. Testing at 15 picofarads is accomplished primarily by laboratory "bench-test" techniques; automatic testing at 15 picofarads is difficult because of the high input capacitance (approximately 20 to 35 picofarads) of most automatic ac test sets.

Users should follow the sequence below when testing COS/MOS devices:

1. Insert the device into the test socket.
2. Apply V_{DD}.
3. Apply the input signal.
4. Perform the test.
5. On completion of test, remove the input signal.
6. Turn off the power supply (V_{DD}).
7. Remove the device from the test socket and insert it into a conductive carrier. COS/MOS devices under test must not be exposed to electrostatic discharge or forward biasing of the intrinsic protective diodes shown in Fig. 1.

For detailed COS/MOS IC handling and operating considerations, refer to RCA Application Note, Guide to Better Handling and Operating of CMOS Integrated Circuits.[1]

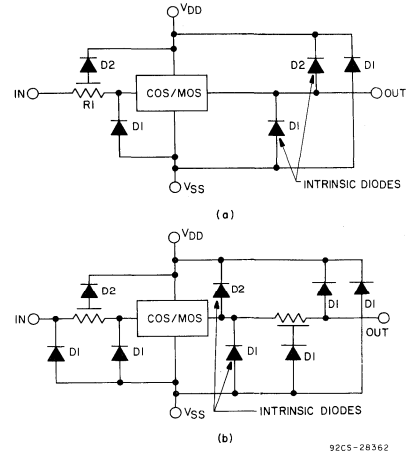


Fig. 1 — (a) Standard protection network used on all CD4000A- and some CD4000B-series devices; (b) improved protection network used on all new RCA COS/MOS devices. Diode breakdown: D1 = 25 V, D2 = 50 V, R2 << R1.

STATIC TESTING

DC-Parameter Testing

DC parameters are those specified for steady-state conditions; dc testing of RCA devices is done at 5, 10, 15, and 20 volts depending on the family under test. Non-varying forcing conditions are applied to the inputs and/or outputs of a package while the device terminals are monitored for expected voltage or current levels.

DC-parameter tests include:

- Functional tests
- Contact tests (diode measurement)
- Leakage tests: quiescent and input
- Breakdown voltage tests
- Output voltage levels
- Input voltage test (includes noise-immunity and noise-margin tests)
- Output drive-current measurements
- Diode tests
- Input-capacitance measurements
- Additional tests as required

A typical CMOS IC test sequence is shown in Fig. 2.

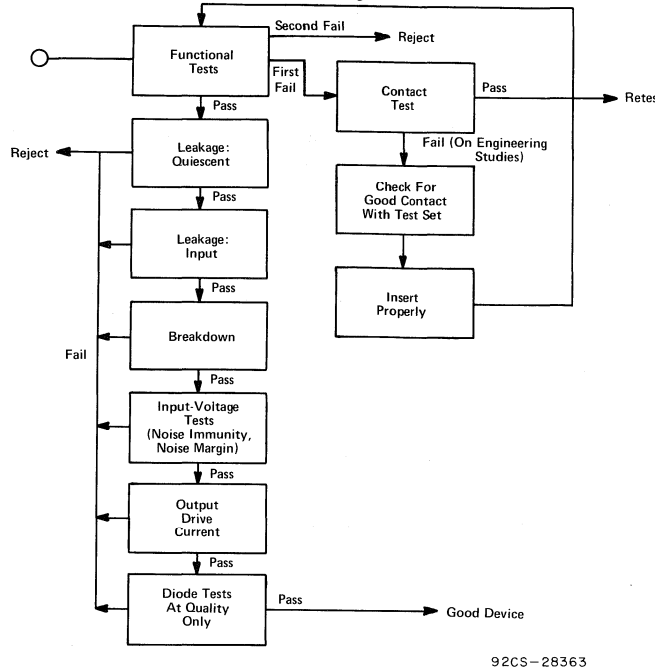


Fig. 2 – A typical COS/MOS IC test sequence.

Functional Tests

Functional tests assure that the device under test will perform its logical operations in accordance with its truth table. The operating voltages for functional tests are shown in Table I. Operation is checked

Table I – Operating Voltage Limits For Functional Tests

	Recommended	Min.	Max.
4000A Series	3 - 12	3	15
4000B Series	3 - 18	3	20

against truth table values by monitoring output-voltage levels for valid logic-high and logic-low levels. Output logic levels for functional tests are:

Logic 0: $\leqslant V_{SS}$ +0.5 V

Logic 1: $\geqslant V_{DD}$ −0.5 V, V_{DD} is referenced to V_{SS}.

Fig. 3 shows an example of a CD4001 NOR gate functional test. V_{DD} is selected to cover the desired range of operation. This test is performed at a relatively low frequency ($\ll f_{CL}$ max.) and with no load other than stray and probe capacitances.

When complex circuits such as the CD4094B, Fig. 4, are tested, input signals must be applied to control the functions being examined. The CD4094B is an 8-stage shift and store register whose eight stages are composed of D-type flip-flops connected in sequential logic form with a common clock. In addition to the flip-flop chain, the device has a latch option at each parallel output stage; the latch is controlled by the strobe input level. The parallel outputs are three-state and are controlled by the output enable level. Data stored in the register is available at the serial outputs on both the positive and negative clock transitions.

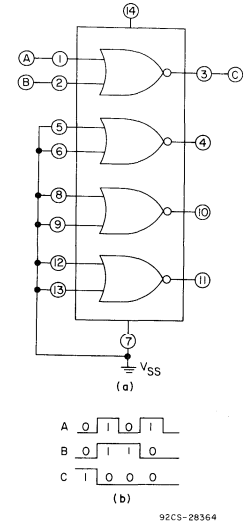


Fig. 3 – Example of CD4001 NOR-gate functional test.

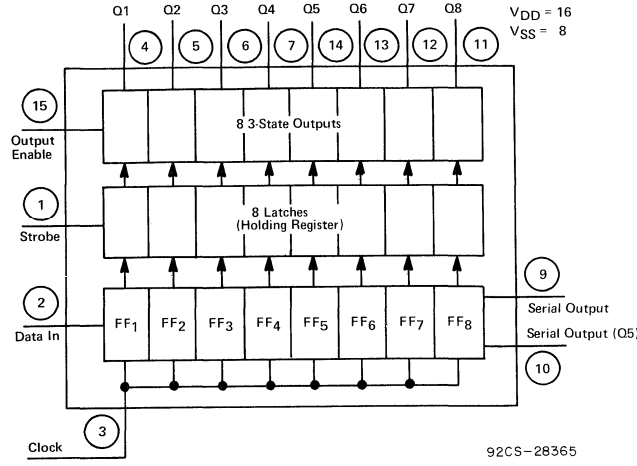


Fig. 4 – Functional diagram of the CD4094B.

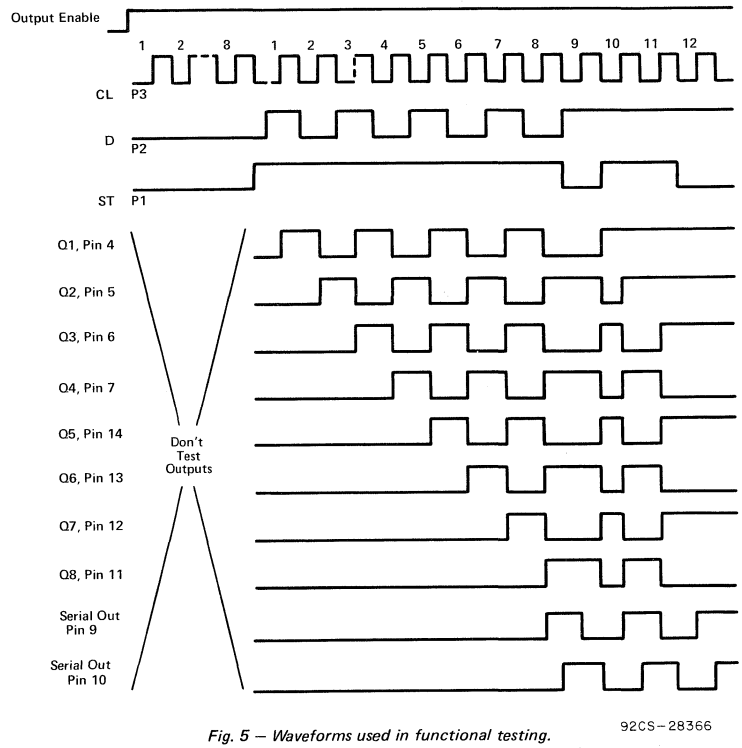


Fig. 5 – Waveforms used in functional testing.

Prior to performance of the static or dc parameter tests, which reflect the data-sheet specifications, all register functions must perform 100 percent. Compliance of a device with functional test requirements is determined by monitoring all outputs for proper operation. Functional testing is performed by applying the waveforms shown in the timing diagram of Fig. 5 to the device under test, in this case the CD4094B of Fig. 4. The tests are performed at a frequency well below the maximum operating frequency of the device. Input logic 1 levels are equal to V_{DD}; input logic 0 levels are equal to V_{SS}. Again, output logic 1 and 0 levels are equal to $V_{DD} - 0.5$ V min. and $V_{SS} + 0.5$ V max., respectively. Functional tests for B-series devices are performed at a $V_{DD} - V_{SS}$ of 22 volts, 2.8 volts, and at intermediate levels depending on the device type.

The timing diagram, Fig. 5, shows 0-level data being clocked into the internal Q output of the shift register while the strobe input is maintained low. After eight positive clock transitions, all the internal Q outputs are at logic 0. Prior to the next positive clock transition, the strobe goes to a 1 state; this condition shifts the zeroes from the internal Q outputs to the external Q outputs and the serial outputs. At this time all outputs are at logic 0. The following clock pulses, those starting at time slot 1, begin shifting 1's and 0's to the parallel outputs. The alternate 1's and 0's are fed into the register up to the negative transition at time-slot 8. At this time the strobe input is sent low to check functionality of the latch. Note that a 0 data bit was transmitted to the Q1 output on the positive clock transition at time-slot 8; however, a positive transition at time-slot 9 does not shift the positive data input to the Q1 output. The Q1 output remains latched low because of the low level at the strobe input. When the strobe goes high, the 1 data bit is transmitted to the Q1 output. At this point the latch functionality plus the functions of the strobe, clock, data inputs, Q_S outputs, and Q outputs, Fig. 4, are fully tested, as shown by the timing diagram.

Leakage Current Tests

Two types of static leakage currents are of concern in COS/MOS devices: Quiescent-leakage and input-leakage current.

Quiescent Leakage Current—In bipolar logic devices, such as TTL devices, the current paths that exist from the power source to ground in the quiescent state cause milliamperes of current to flow even when the device is not functioning. Quiescent leakage may be defined for a COS/MOS device as that current that flows from V_{DD} to V_{SS} when, theoretically, all paths for current flow have been opened because the MOS device is off, Fig. 6.

There is no perfect switch. However, the COS/MOS technology offers quiescent device currents that are orders of magnitude lower than in other forms of digital logic.

Quiescent-leakage tests are performed for all device states according to their respective truth tables. Voltages for quiescent leakage tests are 5, 10, and 15 volts for the CD4000A series and 5, 10, 15, and 20 volts for the CD4000B series. Power dissipation for COS/MOS devices is in the microwatt range regardless of complexity level, and is relatively stable with variations in temperature.

Input-Leakage Current—Input-leakage current is current that flows through reverse-biased diodes, whether intrinsic or diffused, and through the input-protection network connected to the gate. The diodes present in standard and improved protection networks are shown in Fig. 7.

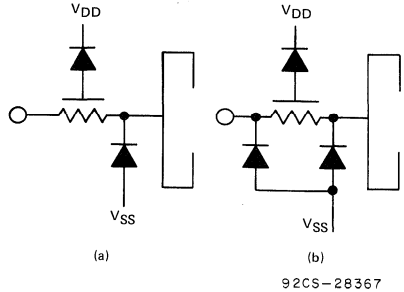


Fig. 7 – (a) Standard and (b) improved protection networks.

Typical input-leakage-current values for COS/MOS devices are in the picoampere range, hence the high input impedance. Automatic test sets cannot measure picoampere values because of test-set resolution. Input currents are measured using 100 nanoamperes as the maximum allowable leakage for a single input.

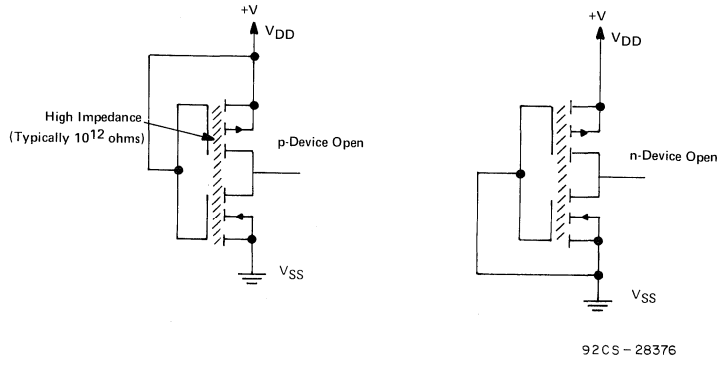


Fig. 6 – Schematic representations of p and n devices when turned off.

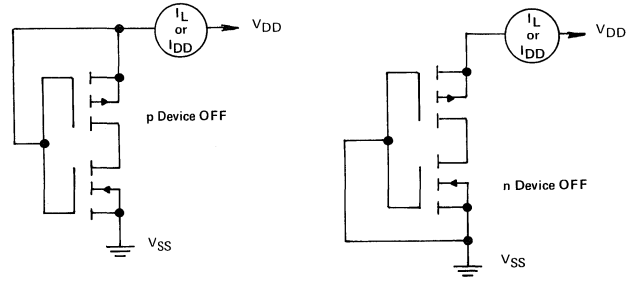


Fig. 8 – Measurement of quiescent leakage current.

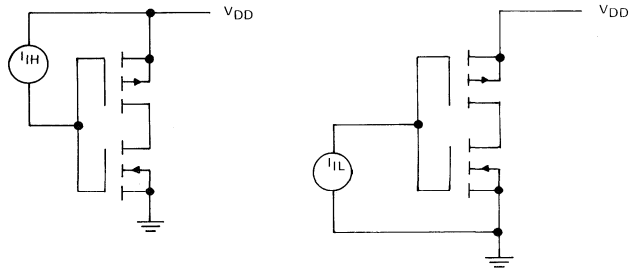


Fig. 9 – Measurement of input leakage.

Examples of quiescent and input leakage test methods are shown in Figs. 8 and 9. In Fig. 8, the quiescent leakage current I_L (I_{DD} may be substituted for I_L) is measured by eliminating all current paths from V_{DD} to V_{SS}. This is done by turning off either the n or the p devices. The current may be measured in the V_{DD} or the V_{SS} line, whichever is more convenient. Unused inputs must be connected either high or low, depending on the channel leakage to be measured.

Input leakage current in Fig. 9 is measured by means of the gate input. Typical input impedance is 10^{12} ohms; therefore, typical input leakage currents are in the picoampere range. Figs. 8 through 14 show various test circuits for the CD4001A.

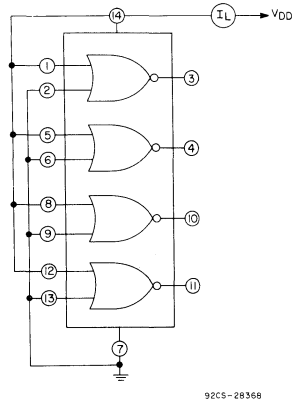


Fig. 10 – Quiescent-device-current test circuit for the CD4001A, leakage-inputs 1 (I_L).

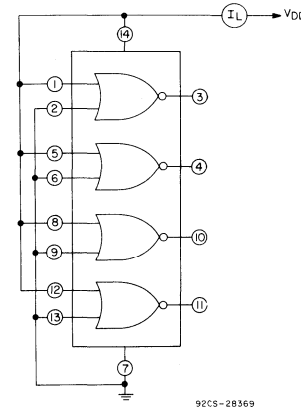


Fig. 11 – Quiescent-device-current test circuit for the CD4001A, leakage-inputs 2 (I_L).

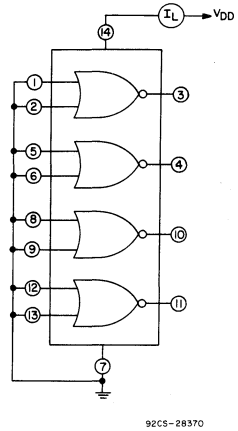


Fig. 12 – Quiescent-device-current test circuit for the CD4001A, leakage - n-devices off (I_L).

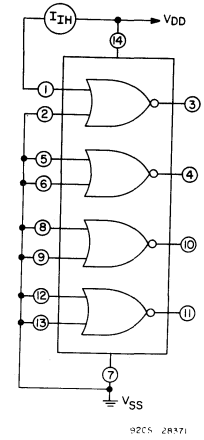


Fig. 13 – Input-current test circuit for the CD4001A, input high (I_{IH}).

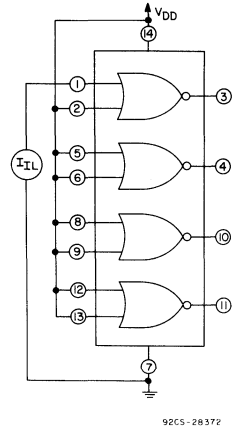


Fig. 14 – Input-current test circuit for the CD4001A, input low (I_{IL}).

The testing of MSI and LSI parts for quiescent leakage current is more complex than that for SSI devices. However, the test is performed in a manner similar to that of the functional test described previously. The CD4090, for example, is connected as shown in Fig. 15. The device is then clocked into its various states, and the current monitored at applicable time slots.

Fig. 16 shows the intrinsic protection circuitry at each external-gate input. With S1 connected to either current source, the voltage drop from the gate input to ground will be one diode drop. A limit of 1.5 volts maximum is usually used to indicate a good diode. With S1 connected to the +100 microampere supply, the presence of the protective diode to the n substrate is tested. With S1 connected to the −100 microampere supply, the presence of the protective diode to the p well is tested. In the event of functional test failures, the above test can be used as a "contact test" to check for proper insertion of the device under test.

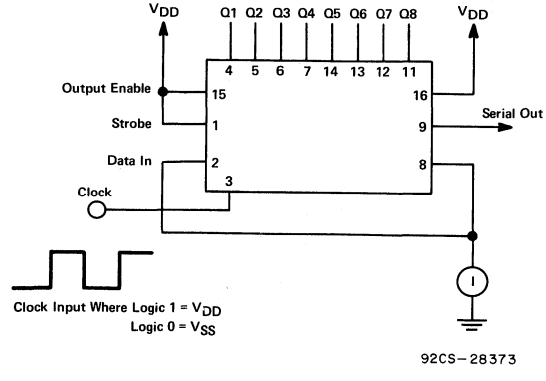


Fig. 15 – Functional-test arrangement for the CD4090.

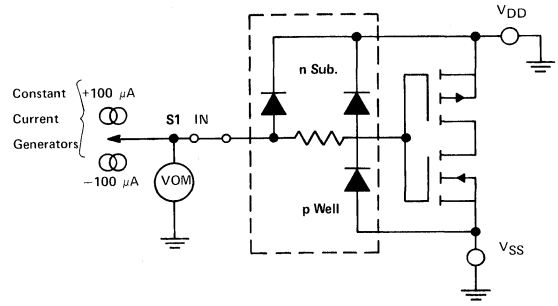


Fig. 16 – Intrinsic protection circuitry at each external input of a COS/MOS device.

Voltage Breakdown Tests

Breakdown tests are performed on the n and p channels of COS/MOS devices in a manner similar to that of quiescent-leakage-current tests. The purpose of the breakdown test is to assure that channel breakdowns can only occur at voltages above the maximum guaranteed supply voltage; Table II gives limits by series. Voltage breakdown test circuits are shown in Fig. 17. With switch S1 in position 1, the n devices are on and the p^+-to-n-substrate diodes are stressed. With switch S1 in position 2, the p devices are on and the n^+-to-p-well diodes are stressed.

Table II – Channel-Breakdown Limits

	Test Voltage	Max. Current Limit
CD4000A Series	15 V	100 μA
CD4000B Series	20 V	100 μA

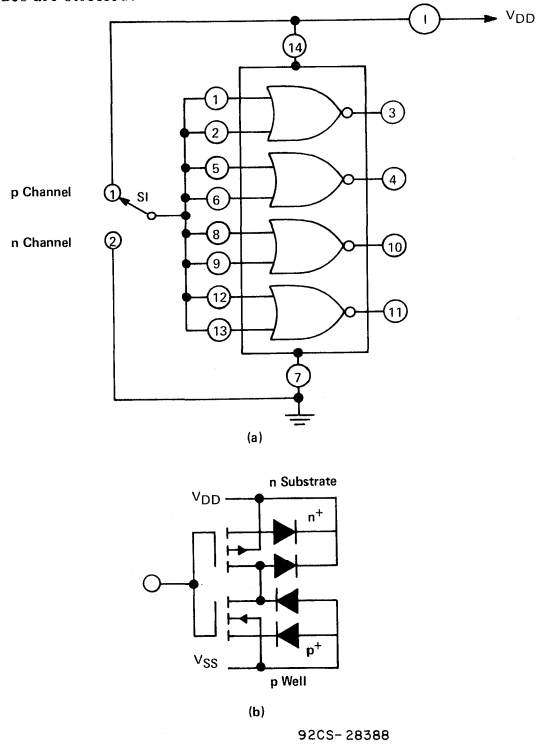


Fig. 17 – Voltage-breakdown test circuit.

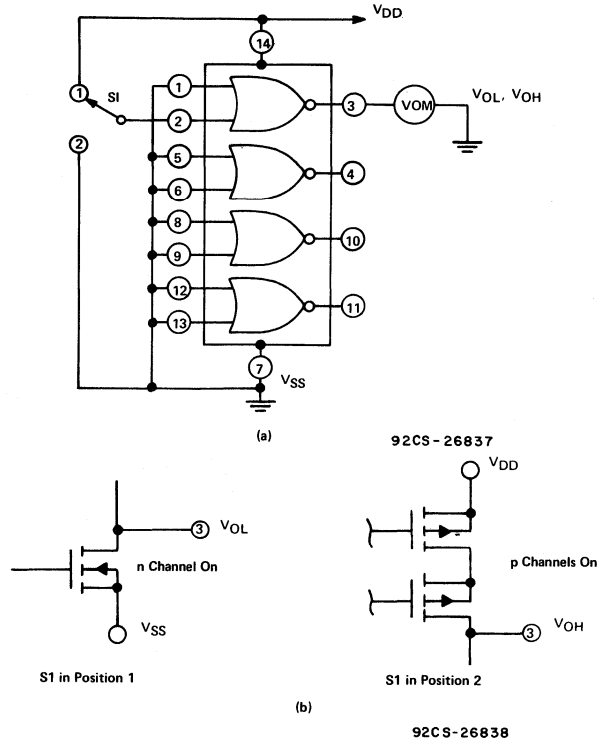


Fig. 18 – Test of output voltage levels (V_{OH} and V_{OL}) of a CD4001A.

Output-Voltage Levels

The output-voltage low (V_{OL}) and the output-voltage high levels (V_{OH}) of a COS/MOS device approach V_{DD} and V_{SS} within a few millivolts. Tests for V_{OL} and V_{OH} are primarily bench-type static tests performed as shown in Fig. 18. With switch S1 in position 1, one n device is turned on and the p devices are turned off. The voltage output will be at V_{SS} + 0.05 volt or V_{SS} – 0 volt. With switch S1 in position 2, all p devices will be turned on and the n devices will be turned off. The voltage output will be at V_{DD} + 0 volt or V_{DD} – 0.05 volt.

Few automatic test sets have the resolution to measure an offset of 50 millivolts from the V_{DD} and V_{SS} supply with satisfactory accuracy at reasonable test speeds. Note that in functional testing, the pass/fail criteria for high and low output states of the device is a maximum of 500 millivolts deviation from V_{DD} and V_{SS}.

Noise Immunity

Noise immunity, V_{NL}, V_{NH}, is defined as the maximum low-level input (V_{IL}) for which an output logic level does not change state, and the minimum high-level input (V_{IH}) for which the output does not change state.

The typical noise immunity of a COS/MOS device is 45-percent of V_{DD}; i.e., the input voltage low and high levels will typically change 45-percent of their values before the output logic level changes. V_{IL} is guaranteed to be a maximum of 30 percent of V_{DD}; V_{IH} is guaranteed to be a minimum of 70 percent of V_{DD}.

Noise Margin

Noise margin is the difference between a device output voltage and V_{IL}; i.e., the magnitude of noise-margin voltage is that noise voltage that may be added to any COS/MOS input/output mode.

Noise margin and noise immunity are guaranteed to meet data-sheet specifications by the performance of input voltage tests, as shown in Fig. 19. The input voltage test is

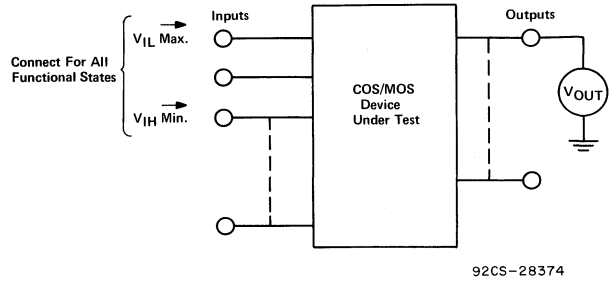


Fig. 19 – Input-voltage-level test arrangement.

performed for each device as in functional testing. V_{IL} and V_{IH} are applied according to the device's truth table. The outputs are monitored for an expected V_{NMH} and V_{NML} state (voltage noise margin, voltage noise margin low).

$$V_{NML} = V_{OL} - V_{IL}$$
$$V_{NMH} = V_{OH} - V_{IH}$$
$$V_{IL} = V_{NL}$$
$$V_{IH} = V_{DD} - V_{NH}$$

Output Drive Current

Tests for output drive currents–I_{DN} (or I_{OL}), sink current, and I_{DP} (or I_{OH}), source current–are conducted by means of the circuits shown in Figs. 20 and 21.

The purpose of the sink-current test, Fig. 20, is to determine the amount of current that the output n device is capable of sinking (with the n channel on) at a given output-voltage level. Fig. 20(a) shows a CD4001AD device whose V_{DD} is equal to 10 volts and whose voltage output is specified at 0.5 volt. The amount of current that the output device can sink varies depending upon the voltage drop across the device (V_{DS}) for a fixed V_{GS}. n-channel drain characteristics are shown in Fig. 20(c).

The purpose of the source-current test, Fig. 21, is to determine the amount of current that the p device is capable of sourcing (with the p channel on) at a given output-voltage level. Fig. 21(a) shows a

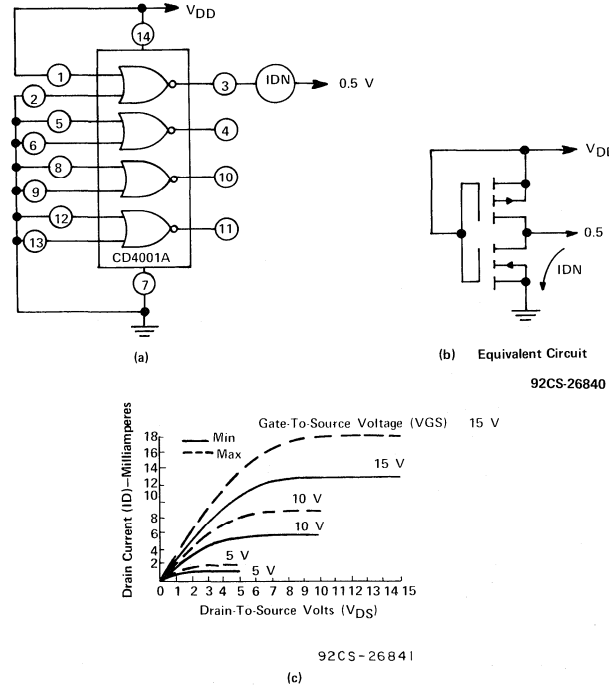


Fig. 20 – Output drive current (I_{DN}), sink-current, test arrangement.

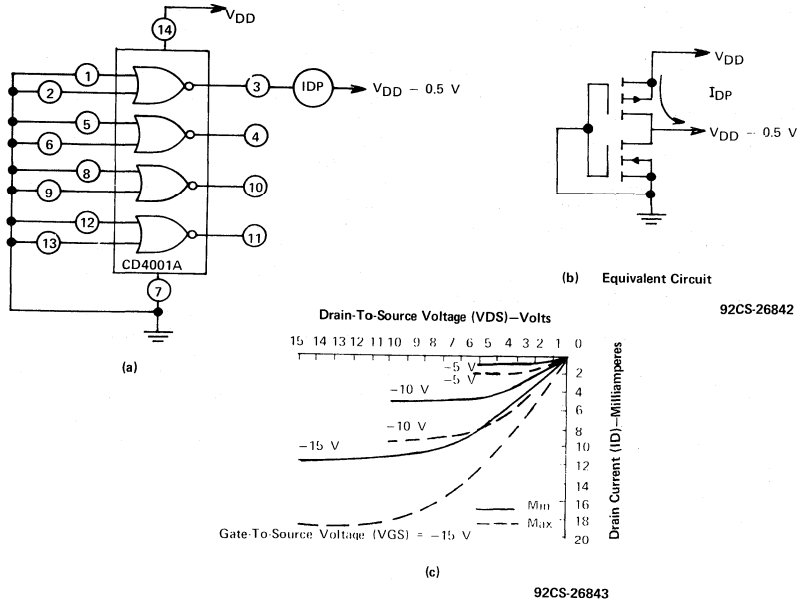


Fig. 21 – Output drive current (I_{DP}), source current, test arrangement.

CD4001AD device whose V_{DD} is equal to 10 volts and whose voltage output is specified at 9.5 volts. Under these conditions, the output drive current will be a minimum of 0.25 milliampere. The amount of current that the device can source varies depending upon the voltage drop across the device (V_{DS}) for a fixed V_{GS}. p-channel drain characteristics are shown in Fig. 21 (c).

These current-voltage relationships can be verified, theoretically, by the use of the following equations.

In the triode region:

$$I_D = \frac{2K'W}{\ell}\left[V_{DS}(V_{GS}-V_{TH}) - \frac{V_{DS}^2}{2}\right] \quad 0 \leqslant V_{DS} \leqslant (V_{GS}-V_{TH})$$

In the saturated region:

$$I_D = \frac{K'W}{\ell}\left[V_{GS}-V_{TH}\right]^2 \quad 0 \leqslant (V_{GS}-V_{TH}) \leqslant V_{DS}$$

where V_{DS} = drain-to-source voltage

V_{GS} = gate-to-source voltage

V_{TH} = device threshold voltage

$K' = \frac{\mu\epsilon_o}{2t_{ox}}$ μ =effective surface mobility of the carrier in the channel

ϵ_o =permittivity of the oxide

t_{ox} =oxide thickness

W = channel width

ℓ = channel length

Input Capacitance

The input capacitance of a device is measured as shown in Fig. 22. A capacitance bridge is connected between each input and V_{SS}. The capacitance is then measured after all stray capacitance has been nulled. The test is performed at a 1-MHz bridge setting. Device input capacitance is considered acceptable if the bridge reading is less than the maximum input capacitance specified on the data sheet.

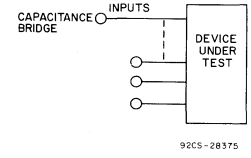


Fig. 22 – Input capacitance measurement.

DYNAMIC TESTING

Propagation Delay and Transition Times

Propagation Delay (t_{PLH}) is measured from the 50-percent point of the input pulse to the 50-percent point of the output pulse as the output goes from a low level to a high level.

Propagation Delay (t_{PHL}) is measured from the 50-percent point of the input pulse to the 50-percent point of the output pulse as the output goes from a high level to a low level.

Transition Time (t_{TLH}) is the time required for the output to make the transition from the low state to the high state (n device turns off, p device turns on). This time is measured from the 10-percent point to the 90-percent point of the output pulse.

Transition Time (t_{THL}) is the time required for the output to make the transition from the high state to the low state (p device turns off, n device turns on). This time is measured from the 10-percent point to the 90-percent point of the output pulse.

Dynamic parameters are measured at a specified load of 15 and/or 50 picofarads. The load specified is for total capacitance including stray and probe capacitance. Frequency is not a critical factor in determining switching speeds of COS/MOS devices. Testing should be done at a frequency compatible with the test set or laboratory equipment involved and must be less than the maximum operating frequency. Fig. 23 shows waveforms

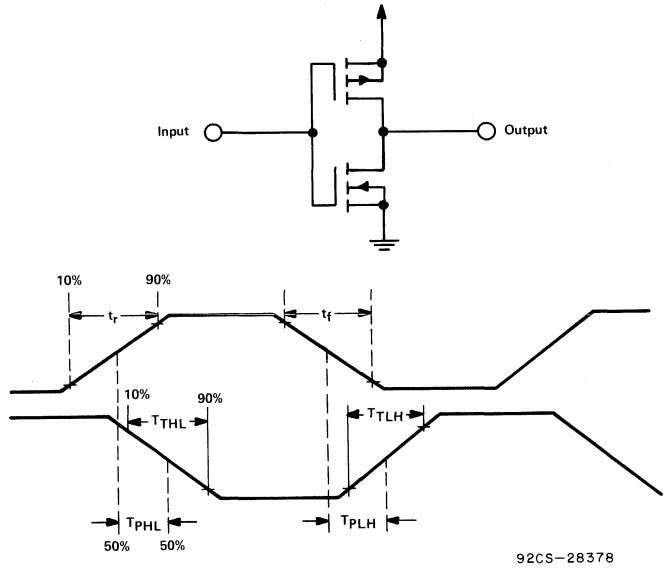


Fig. 23 – Waveforms used in the measurement of propagation delay and transition times.

used in the measurement of propagation delay and transition times.

Note that certain dynamic tests, when performed on a go-no-go basis, are conducted with specified limits as test conditions and with the device outputs monitored. Parameters tested in this way include set-up times, minimum clock, reset and preset pulse widths, clock rise and fall times, maximum clock frequency, and preset and reset removal times. Parameters such as propagation delay and transition times are tested under a set of prescribed conditions so that the test yields actual characteristic data.

Maximum Operating Frequency

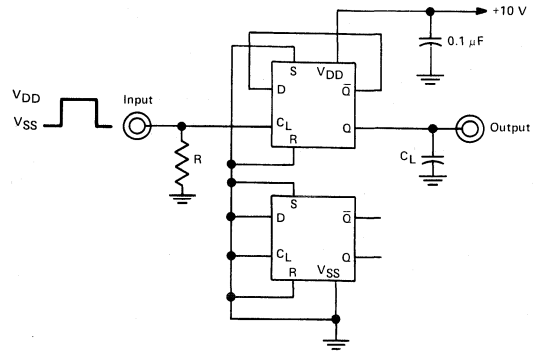
The maximum operating frequency, f_{CL}, is that clock input frequency above which the device will no longer perform its logical function. This frequency is determined by gradually increasing the input frequency while monitoring the output until the device no longer functions properly. The input frequency is then lowered until the device resumes correct operation. The frequency thus determined is the maximum operating frequency of the individual device.

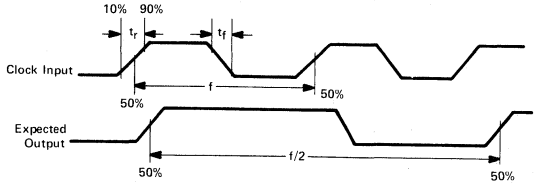
When testing for compliance a device for which a maximum operating frequency has been specified, the maximum specified operating frequency is applied to the device while the outputs are monitored. This is a go-no-go test as opposed to a characterization test.

Fig. 24 shows a CD4013, dual D-type flip-flop, under test for maximum operating frequency at an operating voltage of $V_{DD}-V_{SS}$ of 10 volts.

Set-Up Time

Set-up time (t_S) is the time interval during which a signal is applied and maintained at a specified input terminal before the device recognizes the presence of the specified input pulse. An example of set-up time measurement for a CD4013, Fig. 25, shows a data input which must be present for time t_S (value specified in data sheet) in order for the positive transition of the clock pulse to



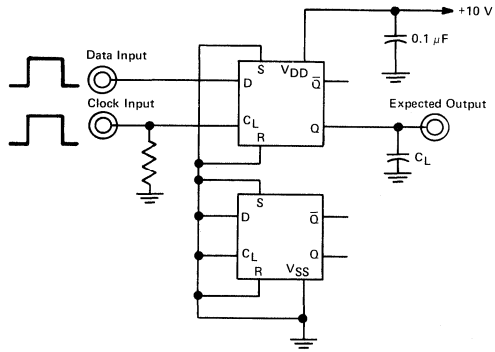


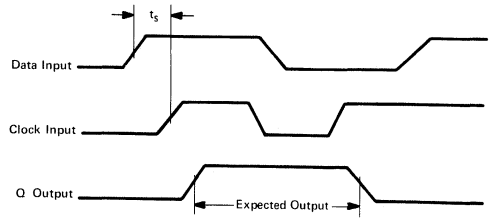
Test Conditions (Per Data-Sheet Specifications*)

* Pulse-Generator Amplitude	10 V
Pulse-Generator Impedance-Matching Resistor (R)	50 ohms
*Pulse-Generator Rise and Fall Times ($t_r = t_f$)	20 ns
*Pulse-Generator Input Frequency (f_{CL})	7 MHz
*Load Capacity – C_L (Including Stray and Probe)	15 pF, 50 pF

92CS-28379

Fig. 24 – Test circuit for measuring the maximum operating frequency of a CD4013A/B.





Test Conditions (Per Data-Sheet Specifications*)

*Pulse-Generator Amplitudes	10 V
Pulse-Generator Impedance–Matching Resistor (R)	50 ohms
*Pulse-Generator Rise and Fall Times ($t_r = t_f$)	20 ns
*Load Capacitance–C_L (Including Stray and Probe)	15 pF, 50 pF
*Setup Time (t_s)	20 ns

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Fig. 25 – Set-up-time test circuit for a CD4013A.

transmit the level at the data input to the Q output. If the data input is not present for a sufficient period of time prior to the positive transition of the clock, the previous state of the data input will be recognized and transmitted to the Q output.

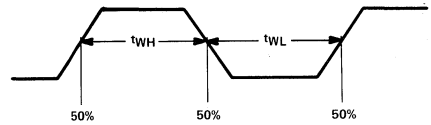
When testing a device for compliance with a specified set-up time, a go-no-go test, the set-up time specified in the data sheet is used as a test condition and the output is monitored for expected operation. When characteristic data is required, the set-up time is varied until the expected output occurs.

Minimum Clock, Set, Reset, and Preset Pulse Widths

Pulse widths, t_W, are defined as the time from the point on the leading edge of the clock-pulse curve which is 50-percent of the maximum amplitude to a point on the trailing edge which is 50-percent of the maximum amplitude, Fig. 26. The minimum pulse width for the clock, set, reset, and preset inputs is that time that the pulse must be present in order for the device to recognize the presence of the pulse.

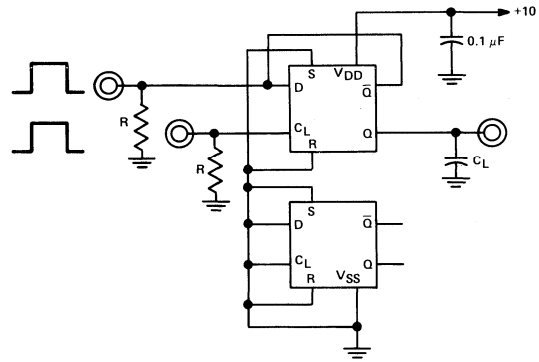
When testing a device for compliance with minimum pulse widths, a go-no-go test, the pulse width specified in the data sheet is used as a test condition and the output is monitored for expected operation. When characteristic data is required, the pulse width is varied until the expected output occurs.

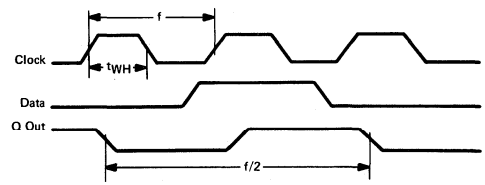
An example of minimum clock-pulse width measurement (t_{WH}) for a CD4013 at a $V_{DD} - V_{SS}$ of 10 volts, Fig. 27, shows the minimum clock-pulse width specified in the data sheet being applied to the clock input of the device under test at a frequency (f) that is less than the maximum operating frequency specified. The clock pulse is applied in one case when the data input is low and is then applied again when the data input is high. (The high and low states of the data input must be present for a time exceeding the specified set-up time.) A device that complies with the minimum clock-pulse width parameter specification will transmit the data input level to the Q output on the positive transition of the clock. Proper operation of the CD4013 can be checked by monitoring for an expected output at Q of f/2.



92CS-28377

Fig. 26 – Waveform used to define pulse widths.





Test Conditions (Per Data-Sheet Specifications*)	
* Pulse-Generator Amplitudes	10 V
* Pulse-Generator Rise and Fall Times	20 ns
Pulse-Generator Impedance-Matching Resistor	50 ohms
* Clock-Pulse-Generator Frequency	<< Max. Operating Frequency
* Load Capacity (C_L) (Total Including Stray)	15 pF, 50 pF

92CS-28383

Fig. 27 – Test circuit for measuring minimum clock-pulse width in a CD4013A/B.

Maximum Clock Rise and Fall Times

The maximum clock rise and fall times (t_{rCL}, t_{fCL}) are the rise and fall times of the clock input signal (measured from 10 percent to 90 percent), above which the device is guaranteed to perform its logical function. This rise and fall time is determined by gradually increasing the clock rise/fall time while monitoring the output until the device no longer functions properly. The clock input rise and fall times are then lowered until the device resumes correct operation. The rise and fall times thus determined are the maximum clock rise and fall time of the individual device.

In testing a device for maximum clock rise and fall times to a specified limit, the maximum specified clock rise and fall times are applied to the clock input while the output is monitored. The input frequency used to perform this test must be less than the reciprocal of $2t_r$; for example, when applying the specified clock rise and fall times for a CD4013 at a $V_{DD} - V_{SS}$ of 10 volts, the maximum clock input frequency that may be used is 100 kHz.

Fig. 28 is an example of a test of maximum clock rise and fall times of a CD4013, dual flip-flop, at an operating voltage, $V_{DD}-V_{SS}$ of 10 volts.

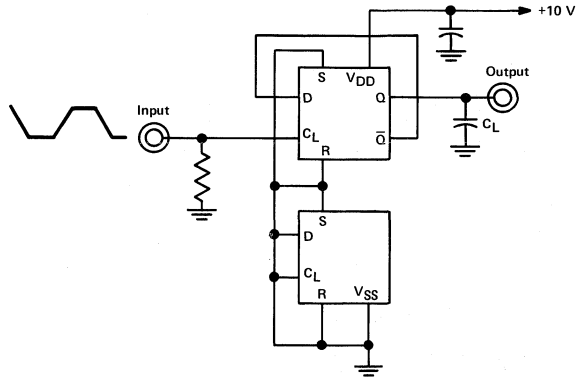
Reset, Set and Preset Removal Time

The reset, set, and preset removal time, t_{REM}, when used in reference to flip-flops, counters, and shift registers, is that time for which the reset, set, or preset pulse must be in its clock enabling state before the device can resume synchronous operation.

When a device is in the preset mode, the JAM input levels are transmitted to the Q output asynchronously. The reset state causes the Q outputs to go to a low level; the set state causes the Q outputs to go to a high level. It is generally an invalid condition to have a device in more than one asynchronous state at the same time.

In testing a device for compliance with data-sheet specifications, the removal time specified is applied at the appropriate input terminal of the device under test. When characterizing a device, the removal time is adjusted relative to the clock input such that expected operation occurs, decreased to the point where expected operation no longer occurs, and then increased until expected operation reoccurs. The time recorded at the reoccurrence of expected operations is the correct removal time (t_{REM}).

An example of a test for minimum preset-enable removal time as specified in the data sheet of a CD4029A, presettable up/down



Test Conditions (Per Data-Sheet Specifications*)	
* Pulse-Generator Amplitude	10 V
* Pulse-Generator Rise and Fall Times (t_{rCL}, t_{fCL})	5 μs
Pulse-Generator Impedance-Matching Resistor	50 ohms
* Pulse-Generator Frequency	100 kHz
* Load Capacity (C_L) (Total Including Stray and Probe)	15 pF, 50 pF

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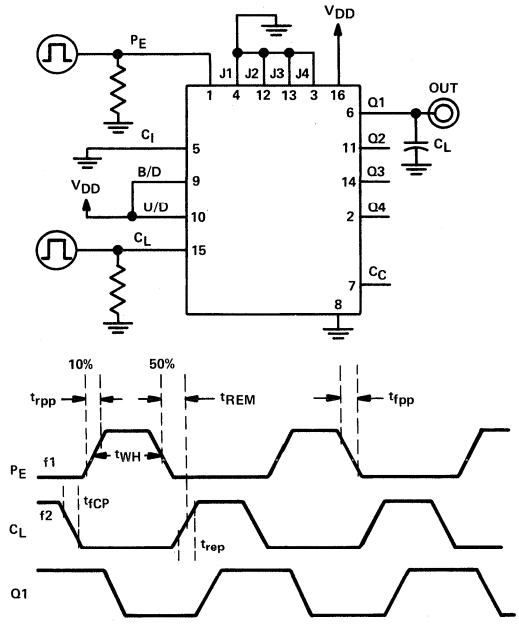
Fig. 28 – Test circuit for measuring maximum clock-pulse width in a CD4013A/B.

counter, is shown in Fig. 29. The JAM inputs J1, J2, J3, and J4 are hard-wired to ground (low). With the preset enable input high, the information on the JAM inputs is transmitted to the Q outputs (regardless of the state of the clock). The preset input is then set low. After a time equal to t_{REM}, the clock-pulse positive transition advances the counter and causes the Q1 output to go high. The transition of the Q1 output from the low to the high state confirms that the preset enable pulse has been removed for a sufficient time to allow the device under test to resume synchronous clocked operation.

Reference

1. Guide to Better Handling and Operation of CMOS Devices, ICAN-6525, J. Flood and H. Pujol, RCA Solid State, 1976.



Test Conditions (Per Data-Sheet Specifications)

Pulse-Generator Amplitude	V_{DD}
Pulse-Generator Rise and Fall Times ($t_{rpp} = t_{fcp}$)	20 ns
Pulse-Generator Impedance-Matching Resistor	50 ohms
Load Capacity (C_L) (Total Including Stray and Probe)	15 pF, 50 pF

92CS-28382

Fig. 29 – Test circuit for measuring preset-enable removal time in a CD4029A/B.

An Introduction to the Use of The General-Processor Unit, GP001

by K. Karstad

This Application Note covers functional operation of the General Processor Unit (GPU) GP001, and contains several examples showing how to do basic programming. It will be evident on working through the examples that many of the bit fields that control the GPU are modifying each other. This situation is not a complete representation of processor operation, but comes about as the result of extraction from the data sheet tables of only that control-field information basic to the illustration of a specific function. This selective extraction was done in order to avoid confusion in this Note and to highlight important functions of the processor. In reality, and in most cases, the control fields cannot be considered separately, as they all have certain side effects. Therefore, during actual program development, the complete data-sheet tables for the GP001 should always be consulted.[1] (A glossary of the terms used in the text and figures of this Note is provided in the Appendix.)

SYSTEM ARCHITECTURE

Overview

The GP001 is an 8-bit, central-processing-unit bit slice intended for use in CPU's, peripheral controllers, microprogrammable computers, and dedicated controllers. It is a high-speed, low-power CMOS/SOS device that can be cascaded, allowing it to efficiently emulate any computer whose word lengths are in multiples of eight bits.

The performance of the GP001 is the result of the coordinated exercise of several distinct subfunctions:a two-port register file, a port 1 buffer register, (P1B), a port 2 buffer register (P2B), a left data type selector (LDTS), a right data type selector (RDTS), an arithmetic logic circuit (ALC), a shifter, a boundary and connect control, separate data input and data output paths and a temporary storage (TS) flip-flop. All of these functions are shown in Fig. 1. The GPU is capable of full-cycle-operation up to 10 MHz; that is, it can access two operands from the file, operate on them through the ALC and store the result in the register file. A more detailed description of each of these subfunctions and their operation is presented below.

Register File

The register file contains 16 words of 8-bits each. The file is parallel-word organized with two 8-bit outputs reflecting the contents of the register enabled to the respective ports. Fig. 2 shows a bit slice of the register file. The two output ports are referred to hereafter in this Note as port 1 and port 2. Any two words addressed by the addresses R and T can be read simultaneously at port 1 and port 2, respectively. Identical data appears at both ports if R and T are equal. Port 1 is addressed via the 4-bit R address; port 2 is addressed via the 4-bit T address.

Data is stored into a selected register through a separate write-data path and under direct control of the load clock (LC). The register addressed by the R address field (port 1) receives data which replaces its previous contents when the load clock goes high. When the clock returns low, the data is locked into the register; i.e., the register is disconnected from the write-data path. Note that it is not possible to write into a register addressed by the T address field.

Port Buffers P1B and P2B

Ports 1 and 2 are connected to port buffers 1 and 2, P1B and P2B, respectively. These buffers operate in different modes under control of the load clock and some of the programming bit fields: S (source select), M (destination select), and A (ALC function).

Port 1 Buffer (P1B) - Port buffer P1B can operate in three different modes, Fig. 3, depending on bit-fields S and M. In mode 1, P1B functions as a latch for the direct-input data, DI. In this mode P1B follows DI while LC is low. Data is latched, retaining the value of DI, at the time of the rising clock edge.

In mode 2, port buffer P1B becomes a master/slave register and takes its input (Port 1) from the register file. In this mode, hereafter referred to as the master/slave mode, the contents of the register file are written into the master when the load clock is high. At the negative-going edge of the clock, the slave is isolated from the master and retains its contents. New data can be entered at the next negative-going clock edge. In mode 2 address field R does not affect buffer P1B when the load clock is low. If R or the contents of the register file (R) change while the clock is low, port buffer P1B will retain its data from the last high-to-low clock transition. This mode is used for writing into the register file from DI.

In mode 3, the P1B buffer **in combination** with the addressed register file forms a master/slave function. While the load clock is high, data is written into the addressed register file (R). At the negative-going clock edge, the data is locked in the master while the slave (P1B) follows the contents of the register file. At the next rising clock edge, the master is once more write-enabled while the contents in the slave are locked up for the duration of the high clock cycle.

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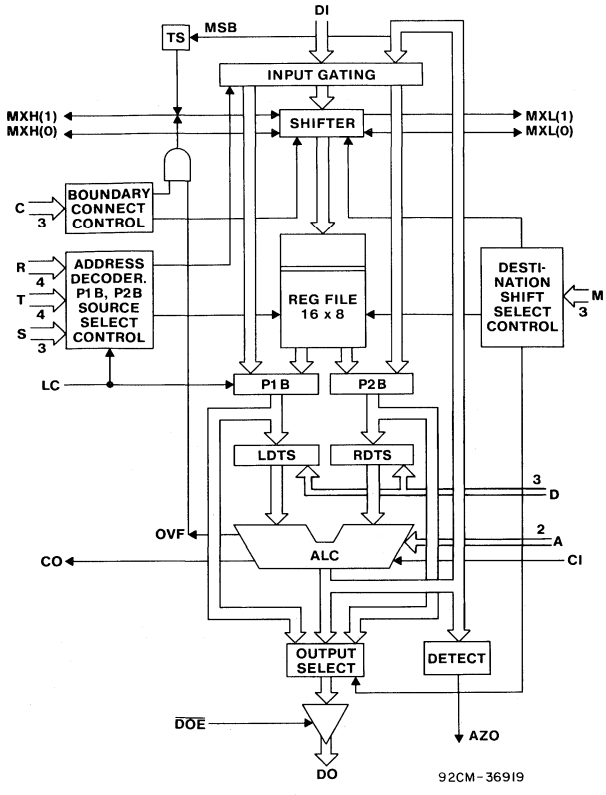

CMOS 8-BIT GPU

Fig. 1 - Block diagram of the CMOS 8-bit general processor unit, GP001.

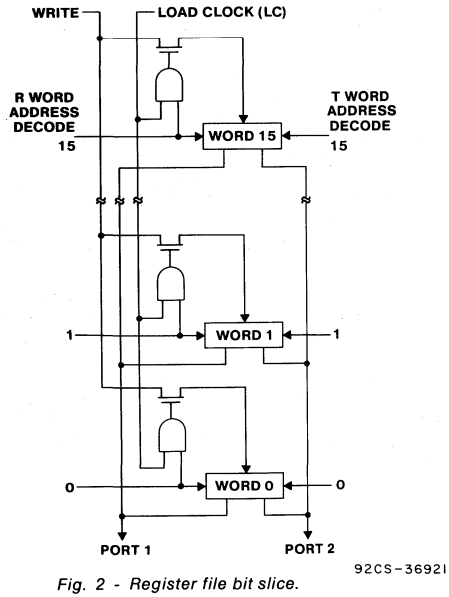

Fig. 2 - Register file bit slice.

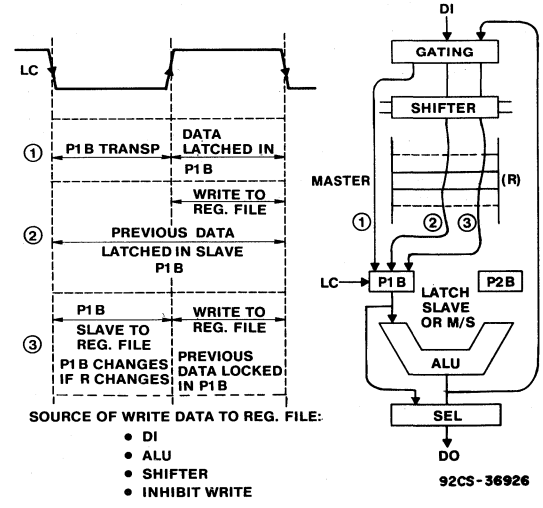

Fig. 3 - Port 1 buffer (P1B) modes.

If the address field R changes while the clock is low, new data is entered into the slave (P1B). The operation of P1B during the low clock cycle, if the address is changed, is the only difference between modes 2 and 3. Mode 3 is referred to hereafter as the slave mode.

Port Buffer P2B - Port buffer P2B can also operate in three modes determined by the control fields A and S, and the address field T. These modes are illustrated in Fig. 4. In the first mode, mode 1, P2B is simply a data follower to incoming data from DI, and is independent of the clock.

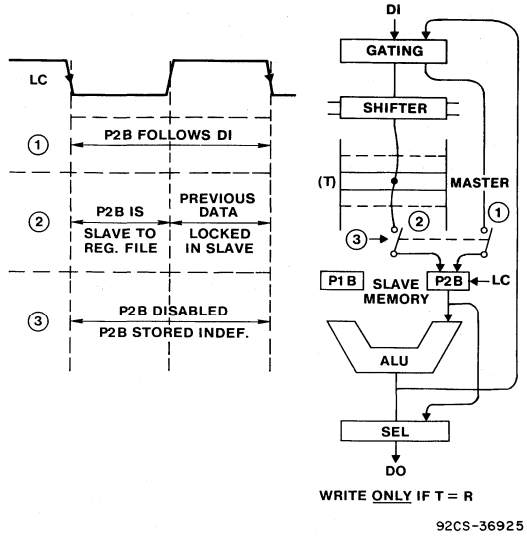

Fig. 4 - Port 2 buffer (P2B) modes.

In mode 2, which is similar to the slave mode described for P1B, port buffer P2B **in combination** with the register file addressed by T forms a master/slave register. As long as the load clock is low, the slave follows the contents of the master, i.e., the register file addressed by T. At the rising clock edge, the master is disconnected and the contents of the slave are stored. At the next negative-going clock edge, the slave can change if the contents of the master change. As described earlier, if the address T changes while the clock is low, P2B will follow the contents of the newly addressed register file. (Note that there is no write path into a register file addressed by T.)

In mode 3, P2B is simply disconnected from the master (register file) by control bits S and A. Whatever the contents were at the time of disabling, they remain indefinitely until the mode is changed.

Data Sources for Register File

The 3-bit M field determines the source of the data to be written into the register file, as illustrated in Fig. 5. If M = 100, the load clock is disabled and nothing can be written into the register file. If M = 000 and S = 01, DI is written into the register file. If M = 001, 010, or 011, the output of the shifter is written into the register file. If M = 101, 110, or 111, the output of the ALC is written into the register file.

Figs. 6 and 7 show the various operating modes of P1B and P2B and how the source of write data to the register file affects P1B in conjunction with the fields M and S.

M	SOURCE OF WRITE DATA FOR REGISTER FILE	
000	S ≠ 01	WRITE INHIBIT
	S = 01	DI
001	SHIFTER	
010	SHIFTER	
011	SHIFTER	
100	WRITE INHIBIT	
101	ALC	
110	ALC	
111	ALC	

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Fig. 5 - Relationship of three-bit M fields to selection of source of data to be written into the register file.

	M									
	111	110	101	100	011	010	001	000		
P1B	5	5	5	1	4	4	4	1	00	S
	SLAVE OF REG. (R)									
	3	3	3	3	3	3	3	2	01	
	LATCH FOR DI							M/S		
	5	5	5	1	4	4	4	1	10	
	SLAVE OF REG. (R)									
	5	5	5	1	4	4	4	1	11	
	SLAVE OF REG. (R + 1)									

1. WRITE INH TO REG. FILE
2. WRITE TO REG. FILE FROM DI
3. P1B IS LATCH FOR DI
4. WRITE TO REG. FILE FROM SHIFTER
5. WRITE TO REG. FILE FROM ALC

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Fig. 6 - Port 1 buffer modes and their relationship to the M and S fields and the source of data to be written into the register file.

	M ≠ 000 A ≠ 01	M = 000 A = 01		
P2B	SLAVE OF REG. (T)	DATA LOCKED	00	S
	SLAVE OF REG. (T)	DATA LOCKED	01	
	FOLLOWER OF DI	SLAVE OF REG. (T)	10	
	FOLLOWER OF DI	SLAVE OF REG. (T)	11	

NOTE:
REG. (T) CAN ONLY BE WRITE ENABLED IF T = R

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Fig. 7 - Port 2 buffer modes and their relationship to the M and S fields and the source of data to be written into the register file.

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Arithmetic-Logic-Circuit (ALC) Operations

The two data type selectors select data for the ALC inputs primarily under control of the D bit field. The left data type selector (LDTS) receives data from P1B and supplies the left ALC port with P1B unmodified, P1B complemented, all zeroes, or P1B right-shifted one bit. For right shift (via LDTS) the A bits must also be programmed (A = 01). In the case where the left operand of the LDTS (P1B) is shifted right one bit, the most significant bit (i.e., the bit that is shifted in) is controlled by the C bit field. For C = 001, the most significant bit of LDTS receives its input from MXH(1), and the least significant bit of LDTS is output to MXL(1). For some values of C, a sign extended shift is caused; i.e., the most significant bit of the left ALC operand is set equal to bit 7 of P1B.

The right data type selector (RDTS) receives data from P2B and supplies the right ALC port with P2B unmodified, P2B complemented, or all zeros. The ALC, controlled by the A bits, provides three basic functions from the GPU: ADD, logical OR, and logical AND. There is one carry-input to the least significant bit, and one carry-output from the most significant bit. A group look-ahead carry circuit is incorporated in the ALC.

The GPU detects boundary conditions during arithmetic operations and indicates overflow. Overflow is defined as a change in the sign bit when performing addition or subtraction. For example, if the sign bit goes to a one state (negative) during the addition of two positive numbers, overflow has occurred. The GPU detects overflow by taking the exclusive OR of the carry-into and the carry-out of the most significant bit. The overflow signal output is time-shared with shift data on the MXH(1) pin under control of the C bits.

Detection of an all-zero output (AZO) of the ALC is also provided. An external pull-up resistor is required for the AZO output, permitting a wire-OR when more than one GPU is used. An all-zero group status is represented by a logical 1 on the bused AZO; a not-all-zero group status is represented by a logical zero.

Note that for logical operations, the carry-out always equals the carry-in. Of course, the carry bit will not affect the result of AND and OR operations.

The method of selecting ALC functions or data-type operands is shown in separate tables in Fig. 8. This information is combined in a matrix in Fig. 9, which shows the various functions that can be implemented by programming the A and D fields. The basic arithmetic and logical functions are:

ADD	AND
SUBTRACT	OR
COMPLEMENT	NAND
INCREMENT	NOR
CLEAR	SHIFT RIGHT AND ADD
PASS	

The shift right one bit and ADD function is useful in implementing multiply algorithms. Note also that P1B - P2B and P2B - P1B subtractions can be done. Exclusive OR and exclusive NOR functions can be performed, but require more than one microcycle.

A	FUNCTION	OPERATION
00	ADD	LEFT + RIGHT + CI
01	ADD	LEFT + RIGHT + CI
10	AND	LEFT ∧ RIGHT
11	OR	LEFT ∨ RIGHT

D	LDTS		RDTS
000	0		$\overline{R}$
001	L		$\overline{R}$
010	A ≠ 01	$\overline{L}$	$\overline{R}$
	A = 01	1/2 * $L^{\dagger}$	
011	$\overline{L}$		0
100	0		R
101	L		R
110	A ≠ 01	$\overline{L}$	R
	A = 01	1/2 * $L^{\dagger}$	
111	L		0

†SHIFTED RIGHT ONE BIT

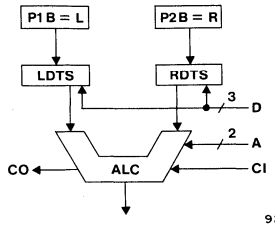

Fig. 8 - Method of selecting arithmetic logic unit functions or data-type operands.

D \ A	00	01	10	11	MNEMONICS 00	01	10	11
000	$\overline{R}$+CI	$\overline{R}$+CI	0	$\overline{R}$	[1] COMP R	[1] COMP R	CLR	NOT R
001	L+$\overline{R}$+CI	L+$\overline{R}$+CI	L ∧ $\overline{R}$	L ∨ $\overline{R}$	[2] SUB L, R	[2] SUB L, R	[4] INHL, R	[5] IMP R, L
010	$\overline{L}$+$\overline{R}$+CI	$\frac{L}{2}$+$\overline{R}$+CI	$\overline{L}$ ∧ $\overline{R}$	$\overline{L}$ ∨ $\overline{R}$		[3] SUB $\frac{L}{2}$, R	NOR L, R	NAND L, R
011	$\overline{L}$+CI	$\overline{L}$+CI	0	$\overline{L}$	[1] COMP L	[1] COMP L	CLR	NOT L
100	R+CI	R+CI	0	R	[3] INC R	[3] INC R	CLR	PASS R
101	L+R+CI	L+R+CI	L ∧ R	L ∨ R	ADD L, R	ADD L, R	AND L, R	OR L, R
110	$\overline{L}$+R+CI	$\frac{L}{2}$+R+CI	$\overline{L}$ ∧ R	$\overline{L}$ ∨ R	[2] SUB R, L	[4] ADD $\frac{L}{2}$, R	INH R, L	[5] IMP L, R
111	L+CI	L+CI	0	L	[3] INC L	[3] INC L	CRL	PASS L

∧ = AND, ∨ = OR, ∀ = EX. OR

NOTES:
1. CI = 1, TWO'S COMPLEMENT
2. CI = 1, TWO'S COMPLEMENT ARITHMETIC
3. CI = 1
4. INH L, R = $\overline{L}$ ∧ R; INH R, L = L ∧ $\overline{R}$ } INHIBIT FUNCTION
   L ∀ R = (L ∧ $\overline{R}$) ∨ ($\overline{L}$ ∧ R)
5. IMP R, L = $\overline{L}$ ∨ R; IMPL, R = $\overline{L}$ ∨ R } IMPLICATION FUNCTION
   L ∀ R = (L ∨ $\overline{R}$) ∧ ($\overline{L}$ ∨ R)

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Fig. 9 - Operand and arithmetic-logic-unit function matrix.

Shift Operations

In addition to the one-bit right shift of LDTS described above, there is a dedicated shifter providing powerful left-right shift capability on the output of the ALC before it is stored back in the register file. The shift-select logic is capable of straight-through (no shift) operation, shifting the ALC output one bit position right, two bit positions right, or one bit position left. The destination of the shifted data is always the register specified by the port 1 address (R field). Direct data input (DI) to the register file from the data input pins also flows through the shifter (unshifted). Again, data is written into the register specified by the port 1 address. The shift function is determined directly by the M bits. The M field can also disable the load clock to the register file, thereby preventing data from being written. The C bits control shifting indirectly; they are the boundary connect control.

During a shift operation, the user has a wide choice as to the shift carry that replaces the vacant bit position. The programming is summarized in Fig. 10. For example, for M = 010 and C = 010, a one-bit right shift takes place with a 1 going into the most significant bit position.

M	SHIFTER FUNCTION
001	ALC OUTPUT LEFT, ONE BIT
010	ALC OUTPUT RIGHT, ONE BIT
011	ALC OUTPUT RIGHT, TWO BITS

C	VALUE GOING INTO BIT POSITION LEFT VACANT BY SHIFT OPERATION			
	LEFT, ONE	RIGHT, ONE	RIGHT, TWO	
	→ BIT 0	→ BIT 7	→ BIT 7	→ BIT 6
000	MXL(0)	ALC(7) ⊻ OVF	ALC(7) ⊻ OVF	ALC(7) ⊻ OVF
001	MXL(0)	MXH(0)	MXH(1)	MXH(0)
010	1	1	1	1
011	0	0	0	0
100	MXL(0)	ALC(7) ⊻ OVF	ALC(7) ⊻ OVF	ALC(7) ⊻ OVF
101	MXL(0)	MXH(0)	TS	MXH(0)
110	MXL(0)	MXH(0)	P2B(7)	MXH(0)
111	MXL(0)	MXH(0)	P2B(7)	MXH(0)

⊻ = EX. OR

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Fig. 10 - Programming, used during a shift operation, to choose the shift carry that replaces the vacant bit position.

The C field, which is the boundary connnect control, determines what is input and output to four leads. MXH(1) and MXH(0) are the most significant shift bits and bidirectional pins. MXL(1) and MXL(0) are the least significant shift bits; of these, MXL(0) is bidirectional while MXL(1) represents tristate output only.

The C bits provide three general classes of states for the four MX shift pins. The first class configures the GPU for normal intercircuit shift operations in a multiple GPU machine (C = 001). The second class of states causes the overflow status indicator to be output on MXH(1) while zero or one is shifted into the shifter (C = 010 or 011). The third class of states causes special outputs to be connected to the MXH bits for left shifts and MSB extension for right shifts.

The C field conditions the data paths of the MX bits for shift operations; if a shift is not specified by the M bits, the C-bit decoding does not affect the data entering the shifter. C = 000 turns off the MXH bits regardless of the M-bit control; however, the MXL bits are not affected.

Fig. 11 summarizes, in table format, boundary and connect status.

C	BOUNDARY AND CONNECT CONTROL
000	MXH(0), MXH(1) - HI Z MXL(0), MXL(1) - DEPENDS ON M-BITS
001	NORMAL INTERCIRCUIT SHIFT CONNECTIONS
010	1 SHIFT IN; OVF → MXH(1)
011	0 SHIFT IN; OVF → MXH(1)
100	MSB EXTENDED FOR RIGHT SHIFTS ELSE: ALC(7) → MXH(0); ALC(6) → MXH(1)
101	ALC(7) → MXH(0); TS → MXH(1)
110	ALC(7) → MXH(0); P2B(7) → MXH(1)
111	ALC(7) → MXH(0); P2B(7) → MXH(1); ALC(7) → TS

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Fig. 11 - Effect of C bits on the boundary conditions of the shifter.

The Temporary Storage (TS) Bit

Bit 7 of the ALC output can be latched into the D-type flip-flop temporary storage bit, TS. TS is enabled for input only when C=111. To store data in TS, the C bits must change to a value other than 111 before bit 7 of the ALC changes. Whenever TS holds meaningful data, C must never be allowed to equal 111, which could possibly happen on a transition of the C bits, for example, from 011 to 100.

Data Output

The GPU can output 8-bits in parallel on the data output (DO) pins if the data output enable ($\overline{DOE}$) signal is low. One of three values can be output on DO: the output of the ALC, the output of P1B, or the output of P2B. The M bit field controls the output gating, as shown in Fig. 12.

M	$\overline{DO}$ ($\overline{DOE}$ = 0)
000	ALC
001	ALC
010	ALC
011	ALC
100	ALC
101	ALC
110	P2B
111	P1B

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Fig. 12 - Relationship of M bit-field controls and output gating.

EXAMPLES OF BASIC OPERATIONS

System Configuration

Some sample operations are given below to illustrate use of the bit fields that determine GPU operation. These bits form part of the microword input from the pipeline register, which is loaded from micromemory. The micromemory is addressed by the output of the microcontroller. Note that the address fields R and T for the register file could come directly from the instruction register (IR). Typically, a bit in

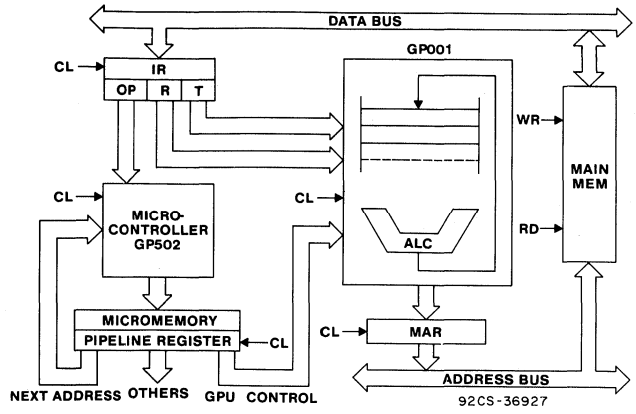


Fig. 13 - The general processor unit in a basic bit-slice system architecture.

the pipeline register controls a multiplexer that selects either the IR or the pipeline as source for the address fields.

Fig. 13 shows how the GPU fits into a basic bit-slice system architecture. A typical mode of operation is as follows:

The micromemory initiates a fetch of a machine instruction from main memory. Assume that the program counter (PC) is in the register file. The pipeline register instructs the GPU to output the contents of the PC to the memory address register (MAR) and to enable the MAR onto the address bus. The instruction is read and loaded into the IR over the data bus. The opcode is next decoded by the microcontroller, which outputs an address for the entry point of a microroutine that executes the fetched machine instruction. The contents of the addressed micromemory location then load the pipeline register. Generally, a long string of bits exercise the bit-fields of the GPU in the execution of the desired instruction, for example, the addition of the operands from two scratch-pad registers and the loading of the result back into one of the registers. The execution of a machine instruction may take more than one microcycle, depending upon the nature of the instruction and the sophistication of the architecture.

In the examples in this Note only the programming of the GPU itself of concern, and all GPU sample operations are performed in one microcycle.

Addition

Assume that two operands have already been loaded into scratchpad registers in the register file, and that the operation R(2) + T(3) → R(2) is to be performed with a CI, carry in, of zero. The required coding of the microword portion for the GPU is shown in Fig. 14. The contents of registers 2 and 3 are read with P1B and P2B in a slave mode with respect to the register file. The operands are added with carry, and the ALC output written back into number two in the register file, all in one microcycle. Overflow is output on pin MXH(1), but can also be detected by monitoring ALC(7) if data out is enabled.

.....	OUT EN	CARRY	DEST SEL	BOUND & CONNECT	DATA TYPE	ALC	SOURCE SEL	ADDRESS		.....
	$\overline{DOE}$	CI	M	C	D	A	S	T	R	
.....	X	0	101	010	101	00	00	0011	0010	.....

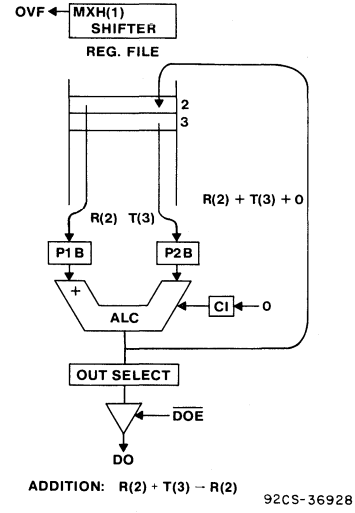


Fig. 14 - Coding and system function for addition.

Subtraction

Subtraction is most easily done with the two's-complement method; i.e., the subtrahend is complemented and added to the minuend plus one. This operation is shown in Fig. 15. The D bits are chosen so that one of the operands, presumably already in the register file, is complemented.

	OUT EN	CARRY	DEST SEL	BOUND & CONNECT	DATA TYPE	ALC	SOURCE SEL	ADDRESS		
	$\overline{DOE}$	CI	M	C	D	A	S	T	R	
	X	1	101	010	001	00	00	0001	0000	R(0) – T(1)
	X	1	101	010	110	00	00	0001	0000	T(1) – R(0)

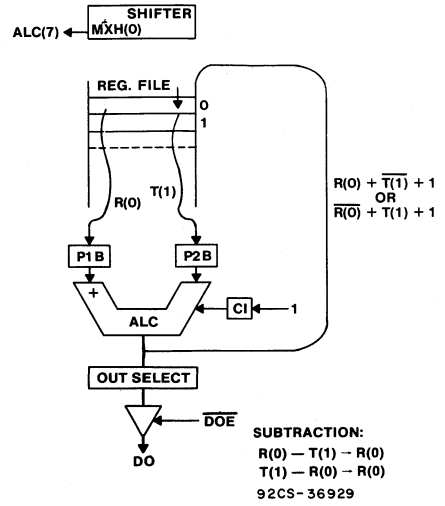


Fig. 15 - Coding and system function for subtraction.

Then a carry of one is added to the sum and the result written back into the register file in the same microcycle. The MSB, the sign bit, available on pin MXH(0), must be monitored.

	OUT EN	CARRY	DEST SEL	BOUND & CONNECT	DATA TYPE	ALC	SOURCE SEL	ADDRESS	
	$\overline{DOE}$	CI	M	C	D	A	S	T	R
	0	X	110	XXX	010	11	00	0110	0101

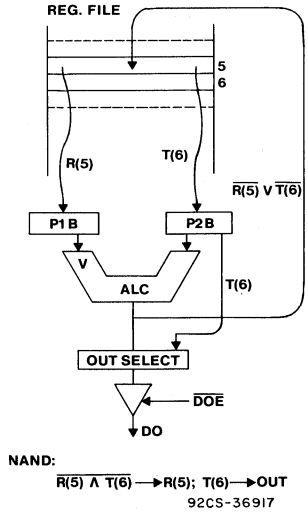


Fig. 16 - Coding and system function for NAND operation.

NAND

Although the A bits can only select ADD, AND, and OR functions, a NAND function is easily implemented by choosing D = 010, which complements the two operands and then OR's them. This operation is shown in Fig. 16. Note that by selecting M = 110, the operand in register 6 is also available at the output, provided the drivers are enabled.

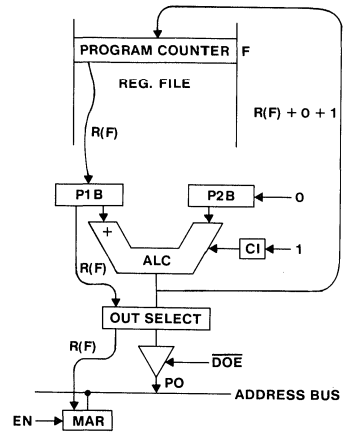
Increment

When there is a need to increment a register, write the result back into the register, and at the same time output the original value, the sequence shown in Fig. 17 is followed. The figure shows a typical example in which one of the scratchpad registers is used as the program counter and its value output to the MAR. The ALC operation is ADD with carry = 1 where the right operand is set to zero. By adding a bit to the pipeline register, the PC value can be made available to the MAR. All of these operations take place in the same microcycle.

Load Data - Pass Data

Loading into the register file from input pins DI takes place as shown in Fig. 18. The register is written into during the high clock cycle. In the mode shown (with S = 01 and M = 000), port P1B acts as a master/slave register. At the negative-going clock transition, the data is locked in the slave and cannot be changed until the next high-to-low transition. In other words, during this direct input to the register file, P1B retains its previous contents, so that pipelining of the GPU is possible. That is, simultaneous with the direct input, the result of the ALC operation appears on the output (if enabled). When the load clock goes low again, P1B follows the register file.

....	MAR EN	OUT EN	CARRY	DEST SEL	BOUND & CONNECT	DATA TYPE	ALC	SOURCE SEL	ADDRESS		....
	MAR	$\overline{DOE}$	CI	M	C	D	A	S	T	R	
	1	0	1	111	XXX	111	00	00	XXXX	1111	



INCREMENT PC: PC → MAR; PC+1 → PC

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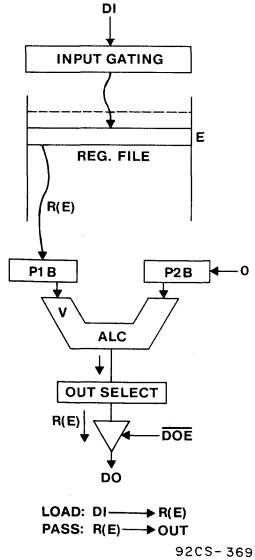
Fig. 17 - Coding and system function to increment the program counter.

The ALC operation shown in this example amounts to PASS data. With D = 111 and A = 11, the data is simply OR'ed with zero.

	$\overline{DOE}$	CI	M	C	D	A	S	T	R	
	0	0	000	XXX	111	11	01	XXXX	1110	



LOAD: DI → R(E)
PASS: R(E) → OUT

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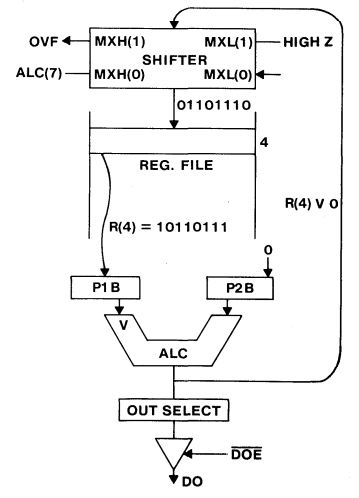
Fig. 18 - Coding and system function for the load data, pass data operation.

Shift Operation

As an example of shift operation, Fig. 19 shows a shift left one bit, with a zero forced into the LSB. The content of the

.....	$\overline{DOE}$	CI	M	C	D	A	S	T	R	.....
	X	X	001	011	111	11	00	XXXX	0100	



SHIFT LEFT, 0: SHL R(4); 0 → LSB

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Fig. 19 - Coding and system function for the shift operation.

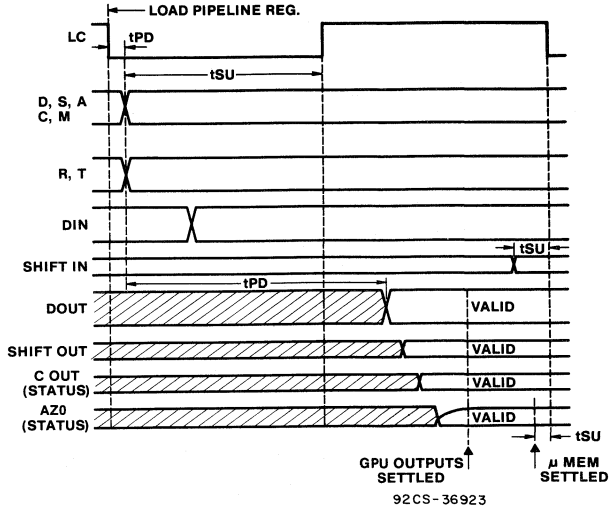

Fig. 20 - Major events in a clock cycle.

register file is read and OR'ed with 0. The output of the ALC is then shifted left one bit with a zero forced into the bit position left vacant:the output of the shifter is written back into the register file. If C = 010, a one would go into the LSB position; for C = 001, whatever is input on the MXL(0) pin fills the LSB.

SYSTEM OPERATION AND TIMING

In order to discuss clock-cycle timing for the GPU, the timing must be considered in the context of a typical control structure, for example, the one shown in Fig. 13. The pipeline register is assumed to be loaded with the falling edge of the clock signal. As a result of applying this newly loaded command to the inputs of the GPU, the GPU will produce a new set of outputs, which have to settle sometime after the rising edge of the clock signal. Some of these GPU outputs are then used as status flags to the microcontroller, where they are used in the formation of the next address for the microprogram memory. Finally, the output of the microprogram memory is assumed to be settled shortly before the falling edge of the clock signal, in time to be loaded into the pipeline register with the falling edge of the clock. These relationships are shown in Fig. 20.

Inputs to the GPU (both data and control) must be steady at all times from set-up time prior to the clock until the hold time after the clock. The set-up time allows the system sufficient time to perform the correct operation, on the correct data, so that the correct ALC data can be written into the register file properly. Hold time for R and T is required to assure that addresses do not change while the clock is low.

MULTISLICE OPERATION

The GPU is an 8-bit-wide slice of a microprocessor. All registers in the GPU, the ALC, and the shifter are 8-bits wide. The design allows concatenation of GPU's to obtain equivalent microprocessors of greater widths. Any number of GPU's may be concatenated, yielding processors of 8 x n bit width.

Fig. 21 illustrates concatenation. The carry-out (CO) of each GPU (except MSS, most significant slice) is connected to the carry-in (CI) of the next more significant GPU. The all-zero detection function is integrated by joining the AZO pins of all GPU's as open drain outputs. The shifters are concatenated by connecting the MXH(0) and MXH(1) pins

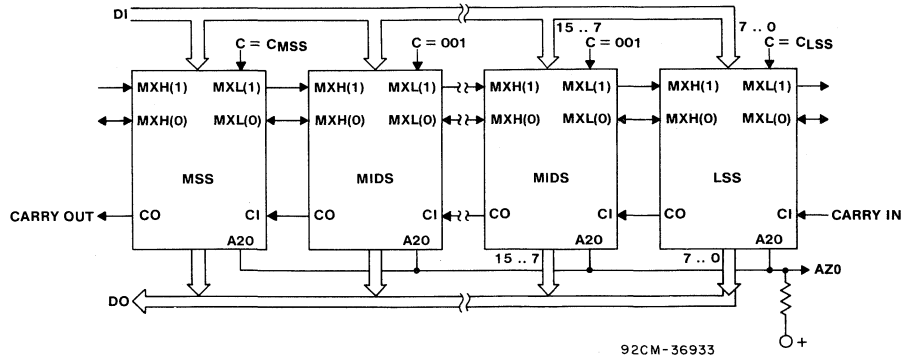

Fig. 21 - Concatenation of general processor units.

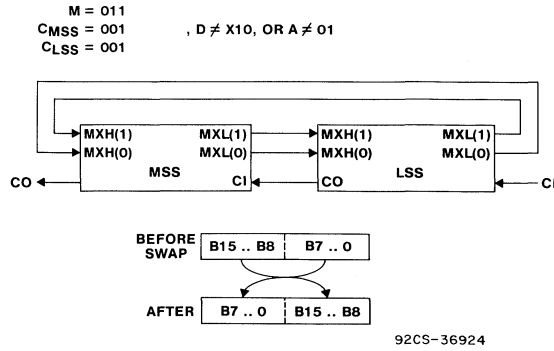

Fig. 22 - Example of ringshift right two bits to implement byte swapping.

of each GPU (except MSS) to the MXL(0) and MXL(1) pins, respectively, of the next more significant GPU. The register addresses R and T, as well as the control signals A, D, M, S, $\overline{DOE}$, and LC are common to all GPU's. The C bits determine whether a GPU behaves as an MS, MID, or LS slice, and thus three distinct sets of C bits must be provided. Note that the control setting C = 001 of the MID GPU's may be hardwired. This is the interconnect mode.

One configuration of a 16-bit machine which allows rotate left or right is shown in Fig. 22. By selecting the M and C fields as shown, a byte swap can be implemented in four microcycles, since M = 011 yields a shift right of two bits. The data-sheet tables show that for M = 011, and C = 001, the LSB, ALC(0), is output on the MXL(0) pin. Since the MXH(0) pin is in the input mode, these two pins can be connected for right ringshift. Similarly, MXL(1) and MXH(1) can be connected, since MXH(1) is in the input mode, and the MXL(1) pin outputs bit ALC(1).

REFERENCE

1. "EPIC (Emulation and Programmable IC Family), CMOS 8-Bit General Processor Unit (GPU)," RCA Solid State Data Sheet for the GP001, File No. 1324.

APPENDIX

GLOSSARY OF TERMS

A	-	2-bit ALC function field
ALC	-	Arithmetic logic circuit
AZO	-	All-zero output
C	-	3-bit boundary and connect control field
CI	-	Carry in
CO	-	Carry out
COMP	-	Complement
CPU	-	Central processor unit
D	-	3-bit data type select field
DI	-	Direct input data
DO	-	Data output
$\overline{DOE}$	-	Data output enable
EN	-	Enable
GPU	-	General processor unit
IMP	-	Implication function
INH	-	Inhibit functions
IR	-	Instruction register
LC	-	Load clock
LDTS	-	Left data type selector
LSB	-	Least significant bit
LSS	-	Least significant slice
M	-	3-bit destination select field
MA	-	Memory address
MAR	-	Memory address register
MIDS	-	Middle slice
MR	-	Master
MS	-	Master-slave
MSB	-	Most significant bit
MSS	-	Most significant slice
MXH(N)	-	Most significant shift bit
MXL(N)	-	Least significant shift bit
OP	-	Operation code
OVF	-	Overflow
P1B	-	Port 1 buffer register
P2B	-	Port 2 buffer register
PC	-	Program counter
R(N)	-	Content of register file addressed by N
R	-	4-bit address field for port 1
RD	-	Read
RDTS	-	Right data type selector
S	-	2-bit source select field
SUB	-	Subtract
T	-	4-bit address field for port 2
TS	-	Temporary storage flip/flop
t_{PD}	-	Propagation delay time
t_{SU}	-	Set-up time
WR	-	Write
Z, High	-	High impedance

INTRODUCING AND APPLYING THE 8 X 8 CMOS/SOS MULTIPLIER, GP503

by K. Karstad

FUNCTIONAL DESCRIPTION

The GP503 is an asynchronous, 8 x 8-bit, expandable multiplier implemented in CMOS/SOS technology.[1] Its expansion features make possible the fabrication of multipliers for operands of any practical length by assembling arrays consisting entirely of GP503 multipliers. The GP503 can be interfaced as an I/O device to most parallel-bus-driven CPU systems. It is, however, specifically intended to complement the EPIC chip set as an I/O device. Thus, as a dedicated hardware multiplier, it unburdens the GPU and increases system throughput.

The GP503 is operated asynchronously. It needs no clocking, and the entire multiply operation occurs within a single microcycle. The multiplier can perform the operation c = b x a + B, or, if the B- inputs are all zero, the operation c = b x a. Two latch controls, L_a and L_b, provide independent latching of the multiplicand and the multiplier, as well as transparent operation of the latches. Two mode controls, M1 and M2, determine whether the multiplier functions as a single slice, i.e., an 8 x 8-bit multiplier, as a least significant slice, as one or more middle slices, or as a most significant slice. A set of tristate drivers is provided for the output signals (the product). The drivers are controlled by two enable signals, EN1 and EN2.

The GP503 is available in a 64-pin, leadless-chip-carrier package.

ARCHITECTURAL FEATURES

The GP503 performs multiplication based on Booth's Algorithm,[2,3] two bits at a time. The multiplication technique for twos-complement numbers using the add and shift method is complicated by the correction step needed when the multiplier is negative. Much of this complication is eliminated in a powerful multiplication algorithm for twos-complement numbers developed by A.D. Booth; the algorithm treats positive and negative numbers uniformly and thereby eliminates the need for correcting the result.

The multiplier consists of two registers (one holding the multiplicand and the other the multiplier), four identical stages that generate a multiple of the multiplicand and add it to or subtract it from the product, and a set of tristate output drivers.

When the multiplier is used as a slice of an array, the next two significant bits of the multiplicand and the multiplier must also be available because of the requirements of Booth's Algorithm. These bits are entered through the pins designated b_{in} and a_{in}, respectively, as shown in Fig. 1. At the least significant end of the operands, where no less significant bit exists, zero must be supplied to b_{in} and a_{in}. Thus, even though the GP503 is an 8 x 8-bit multiplier, the operands are essentially nine bits wide.

The multiplier has two operand registers that latch the values input on b_{7-0}, b_{in} and a_{7-0}, a_{in}, respectively. The two registers are independently controlled by two latch-enable inputs, L_b and L_a, respectively. When L_a and L_b are low, the latches are transparent to the incoming operand data. When the enable inputs are high, the values in the registers are latched and do not change.

As mentioned above, there are four identical adder stages in the multiplier. The function of each stage is primarily determined and dynamically controlled by three bits of the multiplier. As shown in Fig. 2, depending on the value of these three bits, a multiple (0x, 1x, or 2x) of the multiplicand must be added to or subtracted from the product. These three bits of the multiplier are recoded into three control bits. Two of these bits, PASS and SHIFT, control the generator of multiples. The third bit, COMPL, controls the complementer and internally generated carry-in (which is enabled only if M1 is low).

The generator of multiples can output zero, the value of the multiplicand (sign extended one bit), or the multiplicand shifted left one bit (using the value from the b_{in} latch as the least significant bit). The generator of multiples is controlled by the recorder outputs PASS and SHIFT, as shown in Fig. 3. For example, if PASS is low and SHIFT high, the multiplicand is shifted left one bit in the generator of multiples.

The complementer is controlled by the COMPL output of the recorder. If COMPL is low, the complementer passes on the ouput of the generator of multiples unchanged. If COMPL is high, the complementer complements the outputs of the generator of multiples.

The carry-in for the adder in each stage is taken from the CI pin if M1 is high, and is internally generated if M1 is low. If the carry-in is internally generated, it is equal to the value of the COMPL output of the recorder; i.e., 0 for additions and 1 for subtractions.

The mode control bit, M2, controls the behavior of the most significant end of each stage. For most-significant-slice and single-slice multipliers, M2 = 0. A 9-bit adder is required because a factor of twice the multiplicand may have to be added or subtracted, which makes the extra bit necessary. For least-significant-slice or middle-slice multiplies, M2 = 1, and only an 8-bit adder is needed. Therefore, under the control of M2, the ninth bit slice of the adder in each stage can act as an adder slice, or it can merely pass the carry-in from the eighth bit slice of the adder to the carry-out pin CO_i, and pass the value input on pin A_{2i-2} as the ninth bit of output from the adder of stage i. Thus, when M2 is high, the ninth bit slice of the adder in each stage is totally transparent.

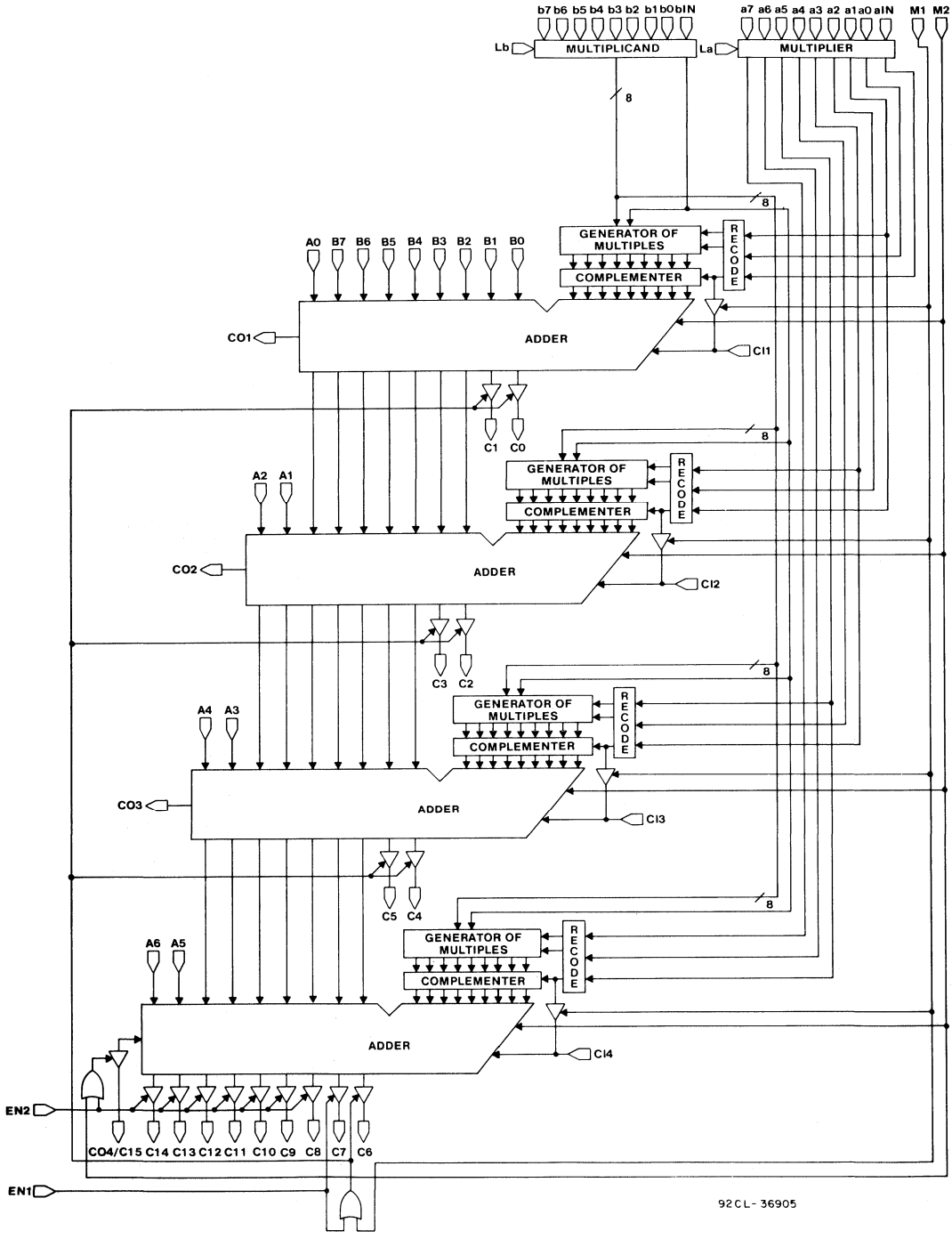

Fig. 1 - Functional block diagram of the 8 x 8-bit multiplier, GP503.

a2i	a2i-1	a2i-2	SHIFT	PASS	COMPL.	OPERATION
0	0	0	0	0	0	ADD 0X MULTIPLICAND
0	0	1	0	1	0	ADD 1X MULTIPLICAND
0	1	0	0	1	0	ADD 1X MULTIPLICAND
0	1	1	1	0	0	ADD 2X MULTIPLICAND
1	0	0	1	0	1	SUBTRACT 2X MULTIPLICAND
1	0	1	0	1	1	SUBTRACT 1X MULTIPLICAND
1	1	0	0	1	1	SUBTRACT 1X MULTIPLICAND
1	1	1	0	0	0	ADD 0X MULTIPLICAND

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Fig. 2 - Recorder functions.

SHIFT	PASS	MULTIPLE	OUTPUT ON BIT NO.								
			8	7	6	5	4	3	2	1	0
0	0	0X	0	0	0	0	0	0	0	0	0
0	1	1X	b7	b7	b6	b5	b4	b3	b2	b1	b0
1	0	2X	b7	b6	b5	b4	b3	b2	b1	b0	bIN
1	1	ILLEGAL	NEVER OCCURS								

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Fig. 3 - Functions of the generator of multiples.

ARRAY CONSTRUCTION

General - The mode-control bits (M-bits) make it possible to expand the GP503 to any practical size multiplier, from 8 x 8 on up. The M-bits reconfigure the internal logic structure so that the carry inputs and carry outputs depend upon the particular location of a multiplier in an array; i.e., most significant slice, least significant slice, middle slice, or single slice. M-bit control decoding is shown in Fig. 4.

The two 8-bit operands, the multiplier and multiplicand, are applied to the pins designated a_0 through a_7 and b_0 through b_7, respectively; their product appears as outputs C_0 through C_{15} (C_{15} appears on the shared CO_4/C_{15} pin only if M = 0). A third 8-bit word may be applied to the expansion inputs (B_0 through B_7) to implement the arithmetic function, c = (b x a) + B, which is required when building large multiplier arrays.

M1	M2	MULTIPLIER MODE	CARRY-IN SIGNALS	9-th BIT SLICE OF ADDER	CO4/C15	
0	0	SINGLE	INTERNAL	ACTIVE	EN2 = 0	HIGH Z
					EN2 = 1	C15
0	1	LEAST SIGNIFICANT SLICE	INTERNAL	TRANSPARENT	CO4	
1	0	MOST SIGNIFICANT SLICE	CIi	ACTIVE	EN2 = 0	HIGH Z
					EN2 = 1	C15
1	1	MIDDLE SLICE	CIi	TRANSPARENT	CO4	

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Fig. 4 - Effect of the mode bits, M.

Data is presented to the a and b inputs while the respective latch control lines (L_a, L_b) are held low. When the latch control lines are raised to a high level, the input data is latched, and will remain stable until a negative transition of the latch control, at which time new operands may be introduced.

Four carry-in signals (CI_1, CI_2, CI_3, and CI_4) and four carry-out signals (CO_1, CO_2, CO_3, and CO_4) link each of the four stages of the GP503 with other multipliers in an array.

The GP503 can be fashioned into a functional multiplier in three ways:

1. Single-slice use (8 x 8 bits)
2. Concatenation (8n x 8 bits)
3. Cascading and concatenation (8n x 8m bits)

Single-Slice Use of the GP503 Multiplier - The GP503 is used as an 8 x 8-bit multiplier by setting both the mode control bits (M_1, M_2) to 0 and connecting the CO and A pins as shown in Fig. 5. (The connections between the CO bits

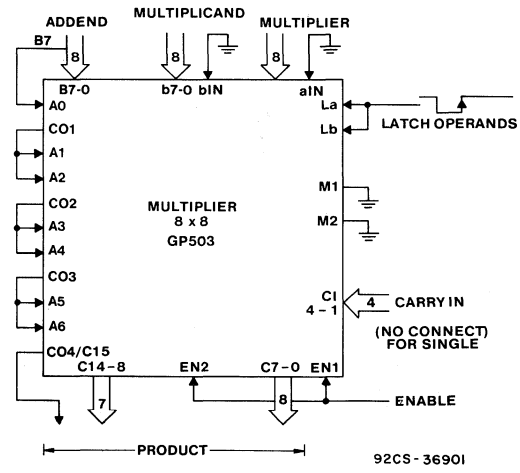

Fig. 5 - The GP503 configured as a single-slice 8 x 8-bit multiplier.

and A bits are required at the most significant end of any GP503 multiplier array to provide extension of sum from the first, second, and third stages). a_{in} and b_{in} are both set to zero. Note that if M_1 is low, the carry-in signals are internally generated, and the CI_1 pins must be externally electrically free to float. In this case, the pins are internally driven. To perform the multiplication c = b x a, B_7 through B_0 and A_0 are set to 0. To perform the operation c = b x a + B, the 8-bit value B is applied to B_7 through B_0, and A_0 is tied to B_7 to provide sign extension. The product appears on pins C_{15} through C_0.

Fig. 6 provides an example of how the single-slice multiplier is used in a 16-bit bit-slice minicomputer architecture where it generates a 16-bit product during one microcycle of operation. It is assumed that the 8-bit multiplier is already stored in a scratchpad register of the least significant 8-bit slice of the GPU GP001.[4] Similarly, it is assumed that the multiplicand is stored in the most significant 8-bit GPU slice

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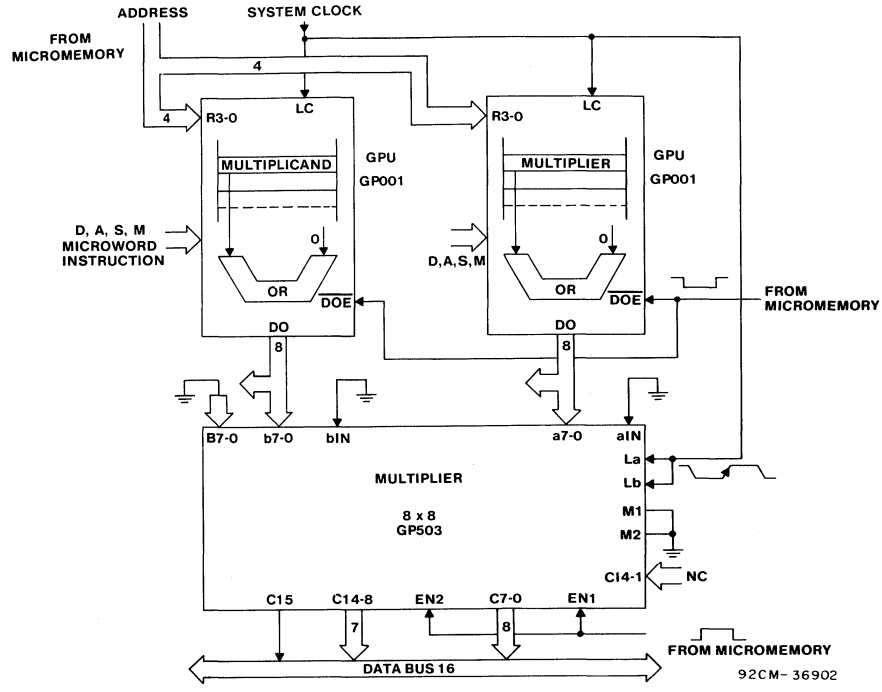


Fig. 6 - Interfacing the GP503 to a 16-bit GPU bit-slice system.

at the same register address, R. A microword is then generated from the micromemory with the control fields needed to input the operands to the multiplier. For example, if D = 111, A = 11, S = 00, M = 100, R = 0000, and $\overline{DOE}$ = 0 (see the data sheet for the GPU 001), the following operation takes place during one microcycle. Both scratchpad registers are addressed and their contents read and supplied as the left data type operand to the arithmetic logic units, ALUs. The ALUs perform an OR operation with the right data type forced to zero. The outputs of the ALUs are enabled and enter the b and a inputs of the multiplier. At the positive-going edge of the system clock, the operands are latched in the multiplier.

The 16-bit product is available (at 10-volts operation) at the c pins of the multiplier typically 110 nanoseconds after the operands are stable at the input. However, in this system architecture, the next microcycle must be in effect before the output can be put out onto the data bus. At this time the product can be written into its destination, for example, main memory.

Another application of the multiplier is shown in Fig. 7, where it is used in a CDP1800-series-based 8-bit microprocessor system. Independent latches for the two operands and tristate enable signals for the product make it easy to interface the multiplier as a simple I/O device. The application shown takes advantage of a feature that permits 16 bits of data to be output with a single instruction over the address bus, even though the CDP1802 is an 8-bit processor.[5]

In the application, the multiplicand and multiplier are stored in one of the scratchpad registers of the CDP1802. When output instruction SEL 1 is executed, both operands go out over the address bus. The multiplicand is latched first by

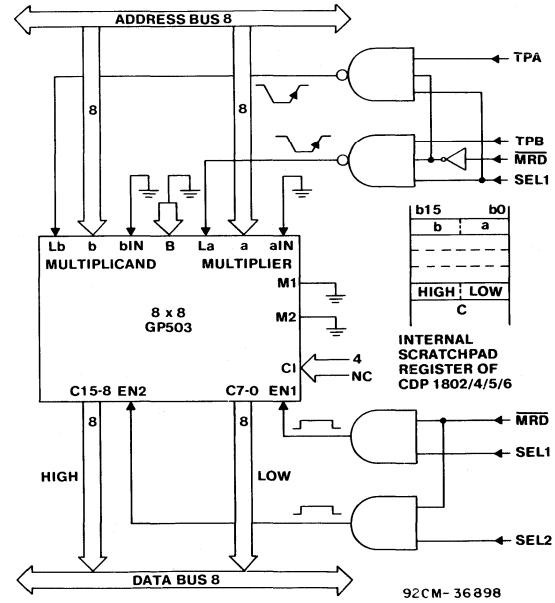


Fig. 7 - The GP503 multiplier interfaced to a CDP1800-based microsystem.

timing pulse TPA, then the multiplier is latched by timing pulse TPB, all in the same execute cycle. The 16-bit product is read by two input instructions, SEL 1 and SEL2, which in turn enable the two tristate drivers.

While the product is generated in approximately 200 nanoseconds (at 5 volts), it takes one instruction to write the operands and two to read the product for a total time of 24 microseconds per multiply using a 2-MHz clock rate. A software routine to do 8 x 8 multiplication in the same system requires from 2.7 to 4.2 milliseconds.

Concatentation of Multipliers - The length of the multiplicand can be increased in increments of 8 bits by concatenating a number of multipliers, as shown in Fig. 8. Concatenated GP503 multipliers can implement 16 x 8-bit multiplication, 24 x 8-bit multiplication, etc. The 16 x 8-bit multiplier in Fig. 8 consists of two GP503 multipliers, one in most-significant-slice mode and the other in least-significant-slice mode.

On the most-significant-slice unit, the mode control bits are set $M_1M_2 = 10$; on the least-significant-slice unit the control bits $M_1M_2 = 01$. No connections should be made to the CI inputs of the least significant slice. To perform the multiplication c = b x a, pins B_{15} through B_0 are all set to 0.

Longer concatenated configurations are straightforward extrapolations of this example.

Cascading of Arrays of Concatenated Multipliers - Concatenation has the effect of creating multiplier arrays with longer multiplicands (b - operand). In most applications this is not sufficient. To create square arrays (16 x 16, 24 x 24, etc.), the multiplier (a - operand) must also be increased.

A 16 x 16-bit multiplier can be constructed by cascading two 16 x 8-bit multiplier arrays, each consisting of two concatenated GP503 multipliers. Fig. 9 illustrates such an array. The upper two GP503 multipliers multiply the 16-bit multiplicand by the eight least-significant bits of the multiplier. Bits C_7 through C_0 form the eight least significant bits of the product, while bits C_{23} through C_8 are forwarded to the B inputs of the lower two GP503 multipliers.

The lower two multipliers multiply the 16-bit multiplicand by the eight most significant bits of the multiplier and add the value expressed by bits C_{23} through C_8. The 24-bit product thus computed by the lower two multipliers forms the 24 most significant bits of the 32-bit product.

RADIATION TOLERANCE

In addition to all of the well-known advantages of the CMOS technology, the SOS technology offers excellent tolerance to radiation, an important factor in aerospace applications. Figs. 10 and 11 show measured radiation properties of the GP503 multiplier. During measurement, the chip was functional up to a dose of 1 Mrad/Si. Over the range from 0 to 1 Mrad/Si, the speed of the device decreases approximately 35 percent; the dynamic current increases by approximately the same amount. A mean upset rate of $4x10^{11}$ rads(Si)/s has been measured for this part.

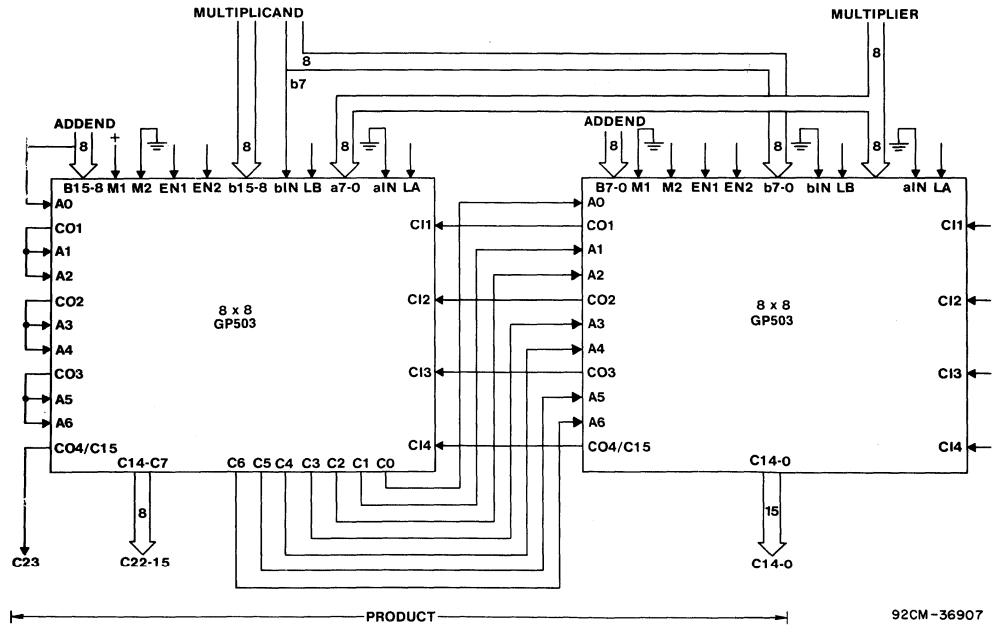


Fig. 8 - Array of two concatenated GP503s forming a 16 x 8-bit multiplier.

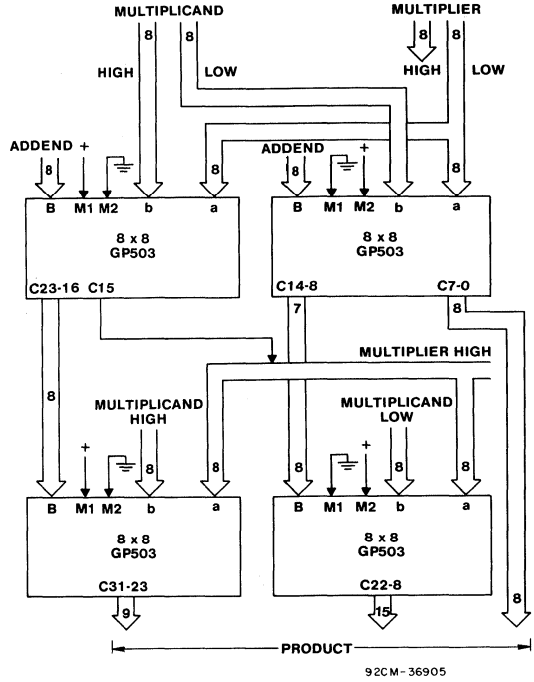


Fig. 9 - Array of four cascaded and concatenated GP503 GPUs forming a 16 x 16-bit multiplier.

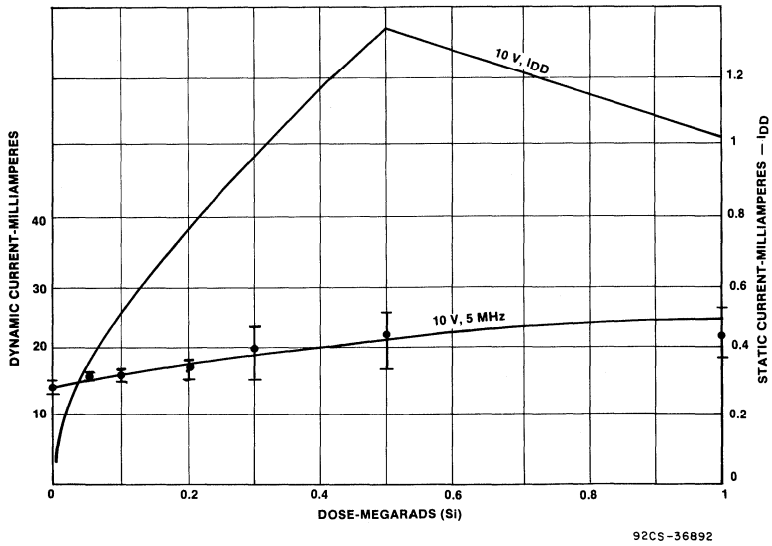


Fig. 10 - Dynamic and static current distribution for five lots of GP503 multipliers.

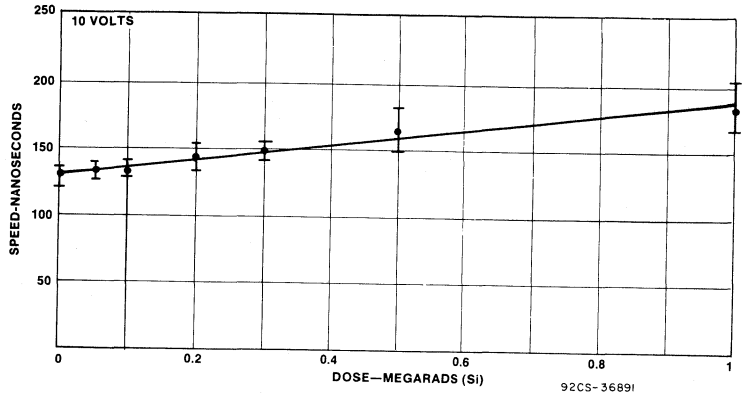


Fig. 11 - Speed distribution for five lots of GP503 multipliers.

REFERENCES

1. "EPIC (Emulation and Programmable IC Family), 8-Bit by 8-Bit Multiplier," GP503, RCA Solid State Data Sheet, File No. 1323.
2. **Computer Architecture and Organization,** John P. Hayes, McGraw-Hill Book Company, pp. 182: "Booth's Multiplication Algorithm."
3. **Computer Arithmetic,** Edited by Earl E. Swartzlander, Jr. pp. 100: "A signed binary multiplication technique," by Andrew D. Booth.
4. "EPIC (Emulation and Programmable IC Family), CMOS 8-Bit General Processor Unit (GPU)," RCA Solid State Data Sheet, File No. 1324.
5. "Register-Based Output Function for RCA COSMAC Microprocessors," RCA Solid State Application Note ICAN-6562.

ACKNOWLEDGMENT

Radiation data supplied by A. Shevchenko.

ICAN-7226

A Primer on Microprogramming and Bit-Slice Architecture Exemplified In Systems Using Members of The EPIC CMOS/SOS Family

by K. Karstad

Introduction

While the idea of microprogramming is more than 30 years old, and most computers today are microprogrammed, the concepts of bit-slice architecture and user-microprogrammable systems are unfamiliar to many in the growing number of microcomputer design engineers. This Application Note takes the mystery out of the terms "bit-slice" and "microprogramming" and relates them to familiar system organizations.

The Note is organized to first define and describe the concepts of microprogramming and bit-slice architecture and then their advantages, limitations, and applications. The basic functional elements, particularly the central processing unit (CPU) and the controller that make up the computers utilizing these concepts are examined individually and then tied together in a simple but operational 16-bit computer that is both microprogrammable and bit-slice structured. (A glossary of the terms used in the text and figures of this Note is provided in the Appendix.)

MICROPROGRAMMING

Microprogramming a computer is not the same as programming a microcomputer. Microprogramming is simply a technique for designing control systems. This Application Note discusses the control of a CPU and system resources in a computer system. However, a control system could be a stand-alone system simply turning control lines on and off in some timed fashion.

Fig. 1 shows the basic components of a classical von Neuman computer architecture. A main memory contains instructions and data to be operated upon. The arithmetic logic unit (ALU) processes the information, and a computer control unit (CCU) oversees the flow of control signals that determine ALU operation and steer data to and from the ALU as well as into and out of I/O devices. Also fundamental to computer operation are a memory address register (MAR) and program counter (PC) (here shown as part of the main memory), some scratchpad registers incorporated in the CPU, and an instruction register (IR), which is part of the CCU block. It is the function of the CCU to decode the operation-code portion of the IR and generate the sequence of control signals needed by the CPU, the memory, and the I/O portions of the system.

Two of these major components are recognizable in the organization of a typical microprocessor chip: the control system, which makes decisions and issues the resulting commands to the rest of the hardware, and the ALU, where calculations are actually carried out. Control lines connecting the hardware logic direct the processing and flow of

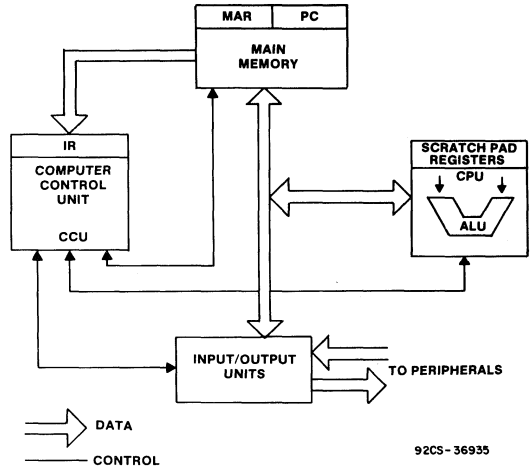


Fig. 1 - Basic classical computer.

data. These lines must be turned on and off at the right moment to get the right control signals to the right place. Precise timing is called for. The rhythm of the entire processor is, therefore, synchronized to a clock. Each machine-level instruction corresponds to a sequence of clock cycles, with each clock cycle marking a single transfer of information along the data path. The function of the control system is to supply the control signals during the appropriate clock cycles.

In the early days of computers, the control system was hardwired with a network of logic to enable it to recognize each machine-level instruction. But since each instruction generated a different sequence of control signals, the system became quite complex as the number of instructions increased. Changes could only be made, and bugs removed, by rewiring. However, as computers developed, a new way of designing control systems to overcome the complexity and inflexibility of hardwired or permanent control systems was proposed.[1] The idea was to think of the control system as a matrix, Fig. 2, in which each row of squares corresponds to a clock cycle and each column is associated with a control line. The control lines go to the CPU and other parts of the system, and choosing a sequence of operations becomes a matter of putting the right binary symbols in the right squares. A one in a square signifies that a particular control line is on during a specific clock cycle.

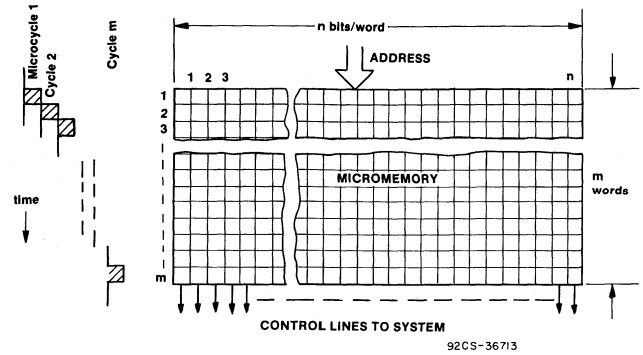


Fig. 2 - Computer control system implemented through the use of a memory matrix structure.

It is immediately evident that the hardware equivalent of the control matrix is a memory structure. This structure is called a micromemory to distinguish it from main memory. The content of each cell in a row determines the state of the corresponding control line for the duration of one clock cycle. The content of each row becomes a microinstruction or microword. The machine-level instruction, which is fetched from the main memory and stored in the instruction register, serves to select a row (or sequence of rows) in the control memory. Hence, the machine-level instruction (hereafter referred to as a macroinstruction) becomes an address designating a row or start address in micromemory. A sequence of microinstructions that executes a macroinstruction is called a microprogram. These concepts are illustrated in Fig. 3, which shows that the macroinstruction is interpreted or decoded by the microcode so as to yield the control signals that manipulate the flow of information in the data path.

The number of bits in a microword can be quite large; hence, techniques have evolved for reducing the cost of a microprogram memory. When a single microinstruction is being executed, generally only a few of the control lines are active; the rest are off. Therefore, it is often possible to supply the same control information by encoding. The approach is to find two wires that are not both on for the same microinstruction, eliminate one, and make the other serve a dual purpose. This arrangement results in a larger number of microinstructions, but each with fewer bits.

An encoded set of microinstructions is described as "vertical" because the resulting microprogram is usually tall and narrow, as shown in Fig. 4. A non-encoded set of microinstructions is described as "horizontal" because the resulting microprogram is usually short and wide. Horizontal microcoding generally means a faster computer since more operations can be performed simultaneously.

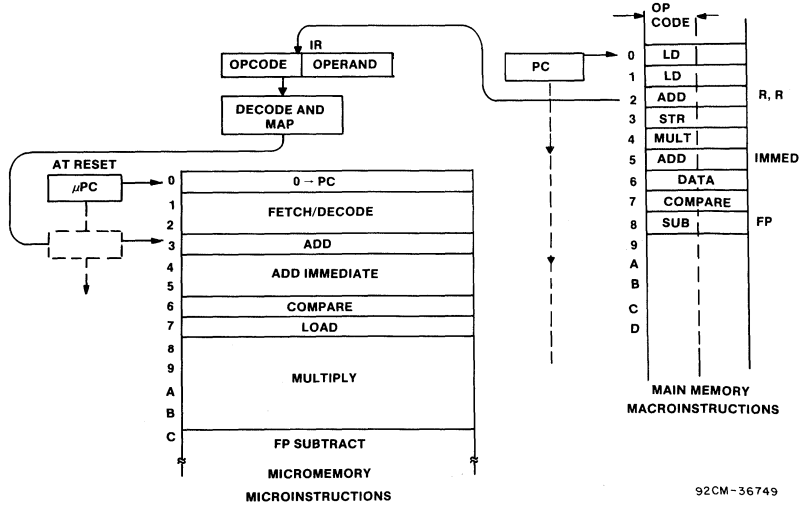


Fig. 3 - Interaction of micro and main memories.

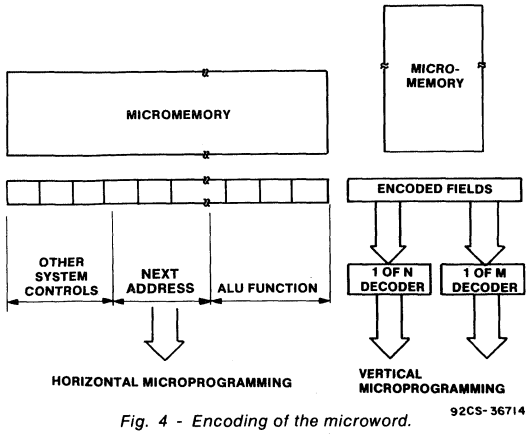


Fig. 4 - Encoding of the microword.

As indicated above, most microcomputers today are microprogrammed, but few of them allow the user to write the microcode. The microprocessors have a fixed instruction set and are general-purpose problem solvers. This Application Note discusses computers that are user microprogrammable, computers that can be specifically tailored for a given application and for which the user designs his own optimum instruction set. In most microprogrammed control sections, the microinstructions are stored in ROMs or PROMs. It is possible, however, to use RAMs for the micromemory, i.e., to have a writable control store. By loading different instruction sets, a fixed hardware configuration appears as different machines, dependent on the instruction set. The design is said to emulate different computers. With a writable control store it is also possible to change the content of the microprogram memory dynamically while the computer is in operation.

BIT-SLICE ARCHITECTURE

Bit-slice machines differ from single-chip processors primarily in the architectural philosophy of their CPUs. The data-processing functions and the control functions (i.e., the decoding circuitry for the instructions) are both hardwired on the same chip in the single-chip microprocessor. Single-chip processors also have a predefined and unchangeable word-length architecture and a fixed instruction set. The opposite holds true for microprogrammable bit-sliced microprocessors. They can be configured to provide a wide variety of digital system architectures with various word lengths and instruction-set capabilities.

The term "bit-slice" comes about because there are limitations on chip complexity, pin numbers, and chip size. The processing section of the CPU is, therefore, partitioned vertically instead of horizontally along functional lines. The vertical partitioning slices the registers and the ALU into equal-length and functionally equivalent parts called bit-slices, or sometimes RALU (register arithmetic logic unit). Commercially, RALUs generally handle 2, 4, or 8 bits, and can be cascaded to form processing sections of any width that is a multiple of the basic unit. The functional diagram of a bit-slice microprocessor that is microprogrammable is shown in Fig. 5. The concatenated arrangement requires that all control lines for each slice be connected in parallel and that the carry output of one chip be connected to the carry input of the next. The arithmetic or logical operations and the sources and destinations for the ALU are the same for all slices. The input data bus is divided into sections of the proper width when entering the processor slices, and the output data bus is recombined when exiting the slices.

Consider the typical control section in Fig. 5; it consists of a microprogram memory, a microprogram sequencer or controller, and some additional logic. The microprogram memory (ROM/PROM or RAM) contains the microinstructions that specify the steps through which the machine

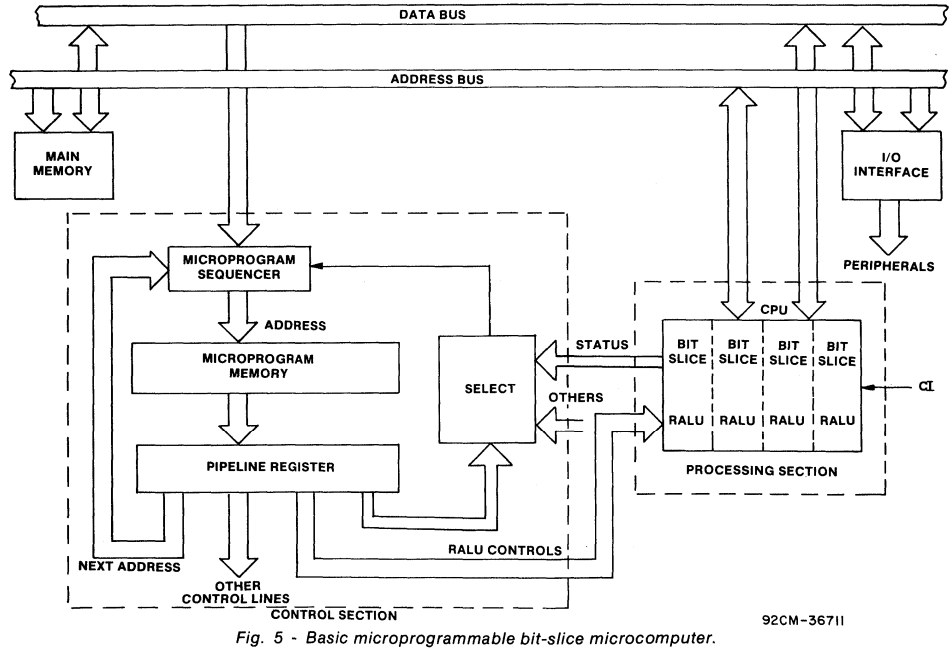


Fig. 5 - Basic microprogrammable bit-slice microcomputer.

sequences and controls the parallel operation of the bit-slices. The sequencer provides the macroinstruction decode logic and determines how the next microprogram address is generated for sequencing the microprogram.

The size of the microprogram memory expands vertically as a function of the number of macroinstructions included in the instruction set. The width of the microinstruction is expanded by cascading a number of similar memory chips. A non-encoded microinstruction may be as wide as 200 bits.

All arithmetic and logic operations are carried out in the processing section, which is composed of functionally equivalent bit-slice chips. In general, a typical slice contains some or all of the following: an ALU, a multiple-word register file, a shifter, input and output data lines, and control inputs.

In the basic configuration of Fig. 5, the microprocessor fetches macroinstructions from the system's main memory under the direction of microinstructions read from its microprogram memory. The operation code of the macroinstruction is "interpreted" by the microprogram sequencer, i.e., mapped into a microprogram memory address and then executed as a series of microsteps. The operand portion (if any) of the macroinstruction is routed to the bit-slices and used either in computations or in main-memory address manipulation.

It is important not to confuse the functions of main memory and micromemory. The system's main memory contains the application program expressed in macroinstructions or machine-level instructions. The microprogram memory of the control section contains microprograms that define the macroinstructions, and thus it gives the machine its "personality" or specific instruction set. Note that the microprogram memory also generates control pulses timed to control the rest of the system. These pulses could typically be latching data into registers or enabling data onto buses.

A designer of microprogrammable bit-slice computers is concerned with two levels of programming: the macro level and the micro level. He must define or choose a macroinstruction set for his application program. And he must implement a set of microprograms that execute his macroinstructions and give the computer its unique character.

SYSTEM COMPONENTS

A simple, but functionally operational, 16-bit microcomputer that employs both microprogramming and bit-slice architecture, as discussed above, can be constructed from the key building blocks of the EPIC (Emulation/and Programmable IC) chip family.[2] This family contains more than a dozen LSI CMOS/SOS chips which, in various combinations, can be configured into microprogrammable computers with great flexibility of architecture, data format, and overall capability. In addition to all the advantages of the CMOS technology, the SOS technology offers excellent tolerance to radiation, an important factor in aerospace applications. The EPIC family centers around an 8-bit slice, two controllers or sequencers, an interrupt controller, an 8 x 8-bit multiplier slice, RAM and ROM, and a number of universal gate arrays that integrate the logic required to join the major system blocks into a minimum-parts computer system.

The tutorial computer uses the 8-bit slice GP001, and the sequencer GP502, but otherwise readily available CMOS RAMs and EPROMs with high-speed (74HC) CMOS latches and registers to connect the key system parts into a viable computer. For practical reasons, since speed is not a primary factor in the demonstration, the system runs at 5 volts. For maximum speed, the EPIC chips should be operated at 10 volts, but this requirement conflicts with the voltage rating of the 74HC high-speed logic family. The 5-volt system is satisfactory to demonstrate concepts, and for evaluation. In an optimized, full-speed, minimum-parts system, a designer might want to choose some existing EPIC parts for interfacing the control and processing part of the system, or he might choose to implement custom logic in universal gate arrays.

General Processor Unit, GP001

The general processor unit, GP001, Fig. 6, is an 8-bit CPU bit-slice implemented in CMOS/SOS technology.[3] Devices can be cascaded to allow emulation of any computer whose word lengths are a multiple of 8 bits. The ALU functions selected by a 2-bit field, A, are ADD, AND, and OR. The operands are derived from two port buffers, P1B and P2B, but can be modified before entering the ALU by a 3-bit select field, D. The data-type operands, left and right, can feed the ALU data that is unmodified, inverted, or equal to zero. Hence, a greater number of arithmetic and logic functions can be executed than indicated above. At a minimum, the following operations can be selected and performed in one microcycle: ADD, SUBTRACT, COMPLEMENT, INCREMENT, CLEAR, PASS, AND, OR, NAND, NOR, and SHIFT RIGHT & ADD. A microcycle is defined as the time it takes to execute a microinstruction. An additional control field also allows SHIFT LEFT or RIGHT ONE BIT and SHIFT RIGHT TWO BITS.

Each bit-slice has carry-in and carry-out leads with fast group look-ahead carry incorporated on the chip. Group look-ahead carry is a technique that provides fast internal carry propagation.

The register file comprises sixteen 8-bit words, and is a dual-port file accessed by the two address fields R and T. The contents of a register addressed by the R field are transferred to the left port buffer, P1B, while the contents of the register addressed by the T field are transferred to the right port buffer, P2B. If R = T, identical data is read from the two ports simultaneously. Each register can be written into from the data-in (DI) leads when selected by the R field and when the clock is high. The register file and the port buffer act in a master/slave configuration. Thus, pipelining of the CPU is possible; i.e., during a high clock cycle, content previously stored in a register can be read while new data is being loaded. In addition to the write mode just described, the port buffers (P1B and P2B) can operate in other modes, depending upon the 2-bit S field: Data In can be latched into P1B directly or stored indefinitely in P2B, or P1B and P2B can act as slaves to the register file.

The M-bits together with the C field provide left/right shift capability for the ALU output before it is stored in the register file. The shift select (M) moves the ALU output one or two bit positions right, one position left, or passes data without shift. The 3-bit boundary-control field, C, determines what is output on the shift lines and which ones are in input mode. When cascading bit-slices, the MXH leads are connected directly to the MXL leads of the next more significant slice. For ring-shift operation, no external parts are required. The most significant leads, MXH, are looped back to the least significant leads, MXL.

ALU status is provided by separate carry-out and all-zero detect leads. Overflow of the ALU is indicated on the MXH1 line, which is timeshared.

The value of the M-bits also determines if the output of the ALU, the shifter, or the Data In is written into a register, or if

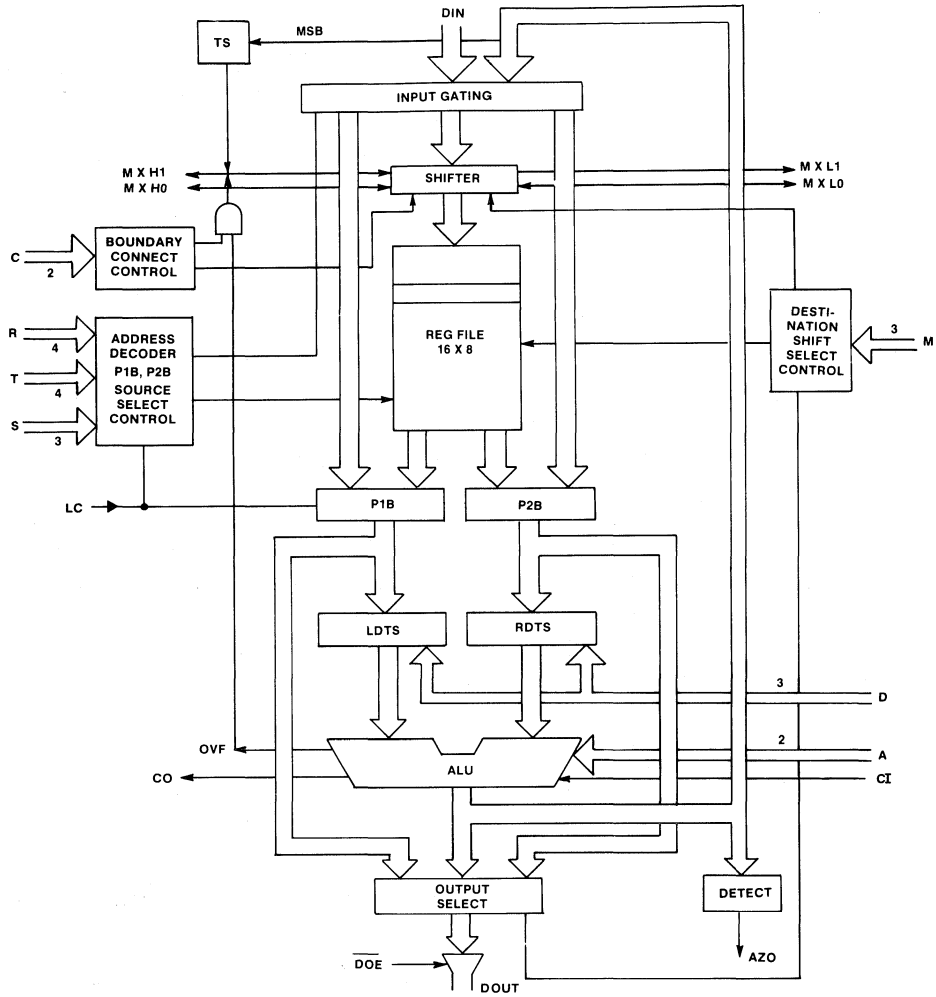


Fig. 6 - General processor unit, GP001.

writing is inhibited. If the three-state output drivers are enabled, either the output of the ALU or the content of P1B or P2B is selected.

Full-cycle operation of the CPU is possible to 10 MHz at a V_{DD} of 10 volts. In full-cycle operation, two operands are accessed from the register file, processed in the ALU, and the result returned for storage in the register file, all in one microcycle of typically 100 nanoseconds.

Microprogram Sequencer, GP502

The control section of a microprocessor gives the machine its "personality." The two main parts of the control section are the microprogram memory, which holds the micro-instructions, and the microprogram sequencer. The main purpose of any sequencer is to present an address to the microprogram memory so that a microinstruction is fetched and executed.

Sequencers may be implemented for simple sequential control circuits that do not have branching capabilities. In the simplest form of sequencer, Fig. 7, only an address counter is required for stepping through the microinstruction. The address of the next microinstruction is selected by incrementing the address counter by one on each clock cycle. The counter technique permits only sequential control; neither conditional nor unconditional flow is possible. Fig. 8 shows a configuration where the address register is loaded with the next address from a field in the currently executed microinstruction. This configuration adds unconditional jumps in the program, but no conditional change in the flow of control. Logic and features could be added until a flexible and powerful LSI controller resulted. One such device is the GP502, shown in Fig. 9, which is essentially a small microprocessor in its own right with its own instruction set. The GP502 is implemented in CMOS/SOS technology, and is functionally and pin equivalent to the popular industry standard AM2910.

The GP502 chip allows addressing of up to 4k words of microprogram. The controller contains a four-input multi-

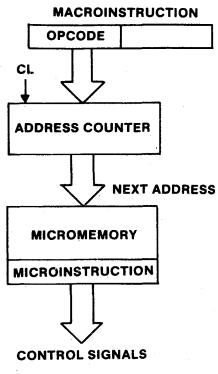


Fig. 7 - The simplest form of sequencer in which only an address counter is required for stepping through the microinstructions.

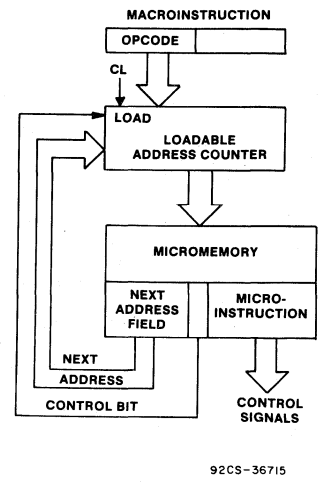


Fig. 8 - A sequencer in which the address register is loaded with the next address from a field in the currently executed microinstruction.

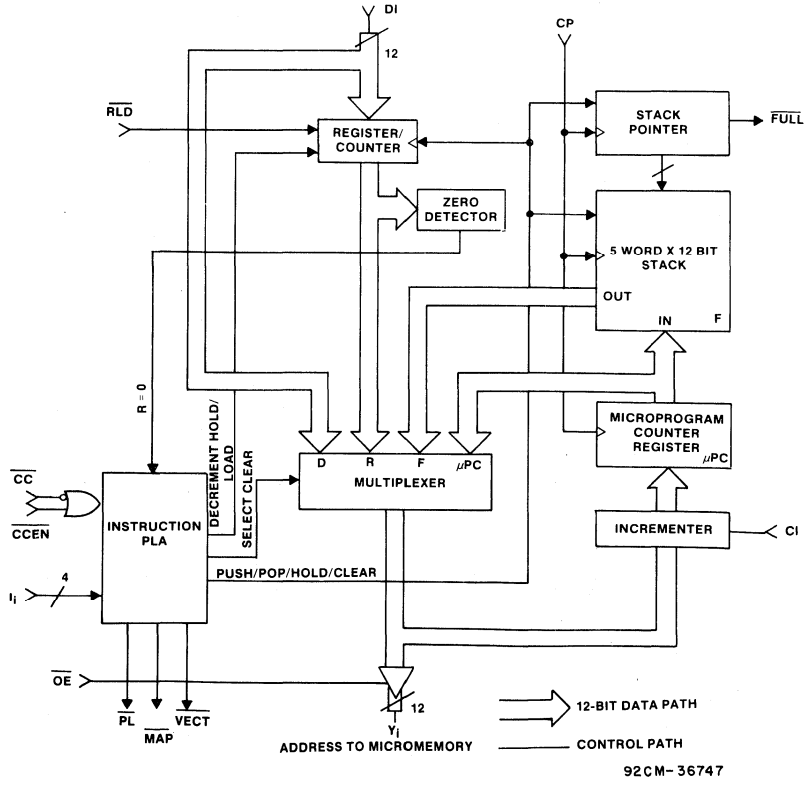


Fig. 9 - The microcontroller, GP502.

plexer that is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

The register/counter is the source when a load instruction is used and the $\overline{RLD}$ (register load) line is low. The counter is loaded from DI on a positive clock pulse. The second source for the multiplexer is the direct inputs. This source is used for branching. The GP502 contains a 12-bit microprogram counter and incrementer. When the carry-in to the incrementer is high, the microprogram register is loaded on the next clock cycle with the current output word plus one. Sequential microinstructions are thus executed. When the carry-in is low, the incrementer passes the output word unmodified, so that the microprogram counter is reloaded with the same word on the next clock cycle. The same microinstruction is thus executed any number of times. The fourth source at the multiplexer is a 5-word by 12-bit stack used to provide return-address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer, which always points to the last file word written.

Sixteen instructions are implemented in the GP502 by a 4-bit input field, I. The instructions control not only the source to the multiplexer, but also three enable signals: $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$. For each instruction, only one of these three outputs is active. They normally control three-state enables as the primary source for microprogram jumps. $\overline{PL}$ normally enables the next address field of a pipeline register. $\overline{MAP}$ enables a PROM, which maps the macro-instruction starting address. $\overline{VECT}$ enables a third source, usually the vector output of an interrupt controller. External parts must be added to the sequencer to obtain these features.

OVERALL SYSTEM DESIGN

A 16-bit microcomputer configuration is shown in Fig. 10. The processing section contains two concatenated GP001 8-bit slices. The control section consists of a microprogram memory and the sequencer GP502 with additional logic as mapper ROM and condition-code multiplexer. The microprogram memory is 2048 words deep with a non-encoded horizontal microinstruction of 64 bits. The micromemory is implemented as a writable control store and uses 74HC574 octal registers for pipeline. The pipeline, on the output of the micromemory, is optional, but permits overlapping of fetch and execute cycles, thus increasing throughput. The 2k x 8 6116 CMOS RAM chips require an 11-bit address input from the sequencer. An 11-bit field in the microword format is dedicated as a next-address field and enabled from the sequencer's $\overline{PL}$ output. Under three-state control, either the next-address field or the output of the mapper ROMs will provide the data input to the sequencer. The main memory is also implemented with 2k x 8 memory chips for a 16-bit data format. Then, by adding a memory address register, instruction register, data in/out registers, clock and timing logic, and using a scratchpad register as program counter, the computer becomes complete and operational.

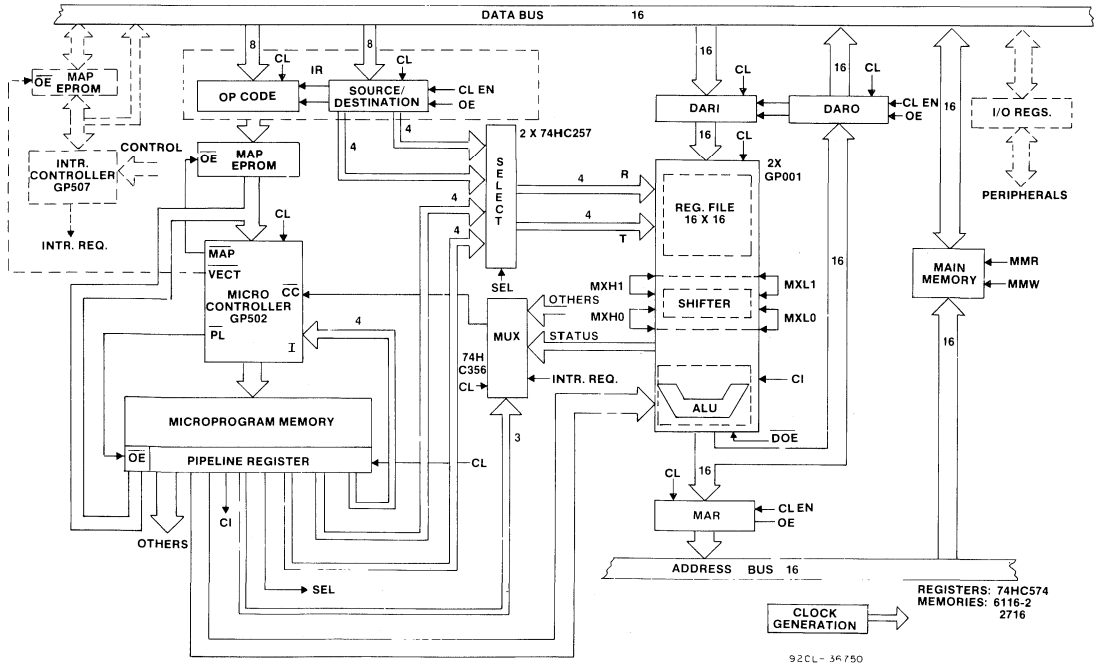


Fig. 10 - A 16-bit microprogrammable bit-slice microcomputer.

TYPICAL OPERATING MODE

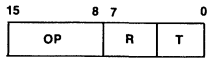
In one typical operating mode, the micromemory initiates a fetch of a macroinstruction from main memory; i.e., the pipeline register instructs the CPU to output the contents of the PC to the MAR and enables MAR to the address bus. The instruction is read and loaded into IR over the data bus. The opcode is next decoded by the controller, which outputs an address for the entry point of a microroutine that executes the fetched macroinstruction. The opcode is translated by the mapper ROM to the proper entry-point address. The content of the addressed micromemory location loads the pipeline register. The bits in the micromemory direct the CPU to execute the desired instruction, and provide necessary timing pulses to memory, registers, or other system components. A sample instruction is: add the operands from two scratchpad registers and load the result back into one of them; this is done in one microcycle. However, some macroinstructions may require more than one cycle, depending upon the nature of the instruction and the sophistication of the architecture.

The architecture shown provides two ways of addressing the register file in the CPU. The operand part of the instruction may contain the R and T address or the addresses may come directly from the microcode. A bit in the microword selects one of the two sources.

Most of the 16 control instructions for the sequencer are conditional and depend on the input at pin $\overline{CC}$. Status signals from the CPU, such as carry-out, overflow, all zero detect, and other system flags, are input to a multiplexer whose selected output is tested by the sequencer at pin $\overline{CC}$.

The operation of this simple computer is further illustrated by two instruction formats for the ADD operation.

Example 1 — A register-to-register instruction format, for instance, can consist of an 8-bit opcode and two 4-bit source operand specifiers, Fig. 11. Assume that the operands



(R) ← (R) + (T)

REG-REG ADD

MICROINSTRUCTION OPERATION	MICROCYCLE						
	T-1	T	T+1	T+2	T+3	T+4	
MAR ← ADDRESS BUS; READ INSTRUCTION	A		B		C		
DECODE; PC → MAR; PC +1 → PC		A		B		C	
(R) +(T) → (R)			A		B		

A, B, C DENOTE MACHINE INSTRUCTIONS

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Fig. 11 - A register-to-register ADD instruction.

are found in two internal scratchpad registers which have already been loaded. The macroinstruction ADD that is to be executed is defined as (R) + (T) → (R). As shown in Fig. 11, the execution of a stand-alone instruction takes three microcycles.

Assume that, at startup, MAR already holds the PC for instruction A. During the first microcyle, a bit in the microword enables the contents of the MAR onto the address bus while another control bit enables a read of the macroinstruction from main memory. A third control bit has enabled the IR, so that at the end of the clock cycle, the instruction is latched in the IR. During the next microcycle, the opcode portion of the instruction is decoded by the mapper ROM and sequencer, and the microcontroller outputs an address for the microword that executes the fetched macroinstruction. At the end of the second microstep, the contents of the addressed micromemory location load the pipeline register. A portion of the microword dictates execution of the desired ADD instruction in the third cycle. A 4-bit field, R, denotes source of operand number one and destination of result. The T field points to the source of operand number two. The contents of the registers are read with P1B and P2B in a slave mode with respect to the register file. The operands are added with carry, and the ALU's output is written back into the destination register, all in the same step. If a carry-out is generated, it is available at a separate pin.

Note that in the third cycle, a control bit is assigned to enable the content of MAR to the address bus and read the next instruction, B. In the decode cycle, the CPU, otherwise idle, is used to increment the old PC and load MAR in readiness for the next instruction fetch. Therefore, the fetch and execution parts of a macroinstruction are overlapped, resulting in increased speed.

At the cost of increased microprogramming complexity, the pipeline technique used to increase throughput can be carried out at one or more additional levels.

Example 2 — Another example of an instruction format for the demonstration computer involves a register IMMEDIATE ADD instruction, (R) + DATA → (R). The instruction format has a 16-bit operand as immediate data to be added to the contents of the register addressed by R. The result is returned to the same scratchpad register, as shown in Fig. 12.

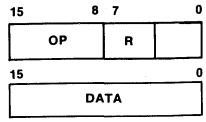
The microcode sequence is similar to example 1, but has one extra microcycle since another fetch is done to get the immediate data. The word is temporarily stored in the data-in register. The last step is the execution phase. Port buffer P1B is slave to register (R) while P2B follows data in, which is enabled from the register DARI (data register in). As in example 1, the execution phase overlaps the first fetch cycle, and the output of the ALU is written back into register (R).

The computer can, of course, be modified or expanded from this basic kernel to greater sophistication and higher speed. For example, an interrupt controller GP507 can be added. The interrupt output line simply connects to one of the condition code multiplexer inputs, and a map PROM is enabled from the $\overline{VECT}$ output of the sequencer. A hardware multiplier, built from GP503 8 x 8-bit slices, can be interfaced to the data bus to increase throughput during multiplication instructions. The interfacing of pheripherals to the data bus, both for serial and parallel I/O devices, follows standard practice.

ADVANTAGES, LIMITATIONS, AND APPLICATIONS

The substitution of simple memory structures for complex hardwired control circuits yields two main advantages: it makes the control system easier to understand and build, and easier to modify. A mistake in a microprogrammed control system can be corrected simply by changing the content of the memory.

Perhaps the greatest advantage of a microprogrammed architecture is the ease of structuring the control sequence. A bit or a group of bits in the microprogram memory is



(R) ← (R) + DATA

REG-IMMED ADD

MICROINSTRUCTION OPERATION	MICROCYCLE								
	T-1	T	T+1	T+2	T+3	T+4	T+5	T+6	
MAR ← ADDRESS BUS; READ INSTRUCTION	A			B			C		
DECODE; PC ← MAR; PC + 1 → PC		A			B			C	
READ OPERAND; DATA → DARI; PC → MAR; PC + 1 → PC			A			B			
(R) + DATA → (R)				A			B		

A, B, C DENOTE MACHINE INSTRUCTIONS

92CS-36893

Fig. 12 - A register-immediate ADD instruction.

allocated to control a certain function (i.e., ALU function, ALU source-register selection, next address calculation selection, status selection, MAR enable, etc.). For each microstep, the appropriate state (low - high) of these bits is written into the memory field. Such a structured implementation makes testing, debugging, and documentation easier. Special macroinstructions that provide in-line checking of software operation can be included.

With the microprogrammed approach, very complex macroinstruction sets can be implemented as sequences of relatively primitive microinstructions. And special microcode can provide substantial speed improvement. For certain aerospace applications, dynamically reconfigurable systems are desirable. Such a system can respond to a fault and reconfigure the system to bypass the faulty element until it is replaced.

The use of parallelism, using bit-slices and pipeline registers, along with the added capability of defining processor wordlength, has tremendously increased effective processing speed and system flexibility. Note that the microprogramming technique is also effective in non-CPU applications. Today's LSI memories are fast and inexpensive, making it practical to use microprogramming techniques in a wide range of complex digital systems.

Perhaps the most exciting feature of user microprogramming is the ability to emulate other machines. By altering the microroutines or substituting another microprogram memory, the functional complexity of the machine is changed. It behaves in an entirely new fashion; i.e., it executes a completely different set of macroinstructions, has a different architecture, and can be tailored to specific applications.

From a designer's viewpoint, the microprogrammable bit-slice approach has an advantage in that the same processor components may be used to define various products. The design of a new system simply means the development of a new microprogram, rather than the repetition of a lengthy overall system design cycle. For some applications, the bit-sliced microprogrammable approach provides the only practical means of achieving special features and high throughput rates. Some notable application areas include signal processing (image processing, digital filtering, FFT (fast Fourier transform)), on-line systems, data communications, process control, high-speed controllers for disks, video and graphic displays, and emulation. Some of the instruction sets that the EPIC chip set has emulated in designed equipment include the 1750A, AN/UYK-20, and PDP-11.

The advantages to microprogramming and bit-slice architecture are not without cost, however. Working with bit-slice microprocessors is more difficult and time consuming than working with single-chip processors. There are at least two levels of control and two levels of programming to consider: the macro level and the micro level. The designer is concerned both with definition of the macroinstruction set and its implementation as a set of microprograms.

Design and software supports, while they exist, are less extensive than those available for single-chip processors. (Commercial design aids available offer emulation of micromemory with trace capability, and include a meta-assembler through which a user can define his own mnemonics.) It is also true that multichip designs are less reliable than single-chip processors because of the increased number of interconnections required. However, despite these limitations, microprogrammable bit-slice architectures are finding increased use in sophisticated, high-speed applications.

REFERENCES AND BIBLIOGRAPHY

1. Wilkes, M.U., "The Best Way to Design an Automatic Calculating Machine," Manchester University Computer Inaugural Conference, Manchester, England, July 1951, p. 16.
2. RCA Solid State publications on the EPIC (Emulation and Programmable IC Family) CMOS/SOS chips:
   - GP001ADL, CMOS 8-Bit General Processor Unit, File No. 1324.
   - GP502ADL, Objective Data Sheet.
   - GP503ADL, 8-Bit by 8-Bit Multiplier, File No. 1323.
   - GP507ADL, Interrupt Control Unit, High Reliablity Integrated Circuit Databook Series, SSD-230.
3. "An Introduction to the Use of the General Processor Unit, GP001," K. Karstad, RCA Solid State Application Note ICAN-7202.
4. Alexandridis, N.A., "Bit-Sliced Microprocessor Architecture," Computer, June 1978, p. 56.
5. Mick, J. and Brick, T., Bit-Slice Microprocessor Design, McGraw-Hill Book Company, N.Y., 1980.

APPENDIX
GLOSSARY OF TERMS

A	2-bit ALC function field
ALU	Arithmetic logic unit
AZO	All-zero output
C	3-bit boundary and connect control field
CC	Condition code
CCEN	Condition-code enable
CCU	Computer control unit
CI	Carry in
CL	Clock
CLEN	Clock enable
CO	Carry out
CP	Clock Pulse
CPU	Central processor unit
D	3-bit data type select field
DARI	Data register in
DARO	Data register out
DI	Direct input data
DOE	Data output enable
FP	Floating point
FULL	Status: stack full
I	4-bit input field
IR	Instruction register
LC	Load clock
LDTS	Left data type selector
M	3-bit destination select field
MAP	Signal that enables a PROM that maps the macroinstruction to a microinstruction starting address
MAR	Memory address register
MMR	Main memory read
MMW	Main memory write
MSB	Most significant bit
MXH(N)	Most significant shift bit
MXL(N)	Least significant shift bit
OE	Output enable
OVF	Overflow
P1B	Port 1 buffer register
P2B	Port 2 buffer register
PC	Program counter
PL	Signal that enables the next address field of a pipeline register
PLA	Programmable logic array
R	4-bit address field for port 1
R(N)	Control of register file addressed by N
RALU	Register arithmetic logic unit
RDTS	Right data type selector
RLD	Register load
S	2-bit source select field
T	4-bit address field for port 2
TS	Temporary storage flip-flop
VECT	Signal that enables the vector output of an interrupt controller
Y_i	Output of sequencer

A 16-BIT MICROPROGRAMMABLE BIT-SLICE COMPUTER DESIGN USING THE GP001 CPU AND GP502 CONTROLLER FROM THE EPIC FAMILY

by K. Karstad

The primary objective of this Application Note is to give designers a feel for the practical implementation of microprogramming and bit-slice architecture using parts of the EPIC (Emulation and Programmable IC) family.*,[1] The 16-bit microprogrammable bit-slice computer design presented indicates the importance of development aids for software and hardware debugging. The approach shows what can be done with simple means to develop and debug software; however, for larger programs, a professional bit-slice development system with special software is a necessity.

This Note concentrates mainly on the hardware design, but also shows how to write the sequences of microcode that execute user-defined macroinstructions. The design example does not include I/O features, interrupt logic or memory management circuits, although these enhancements can be added to the existing bus structure. Nevertheless, the design example can emulate a great number of instructions in existing 16-bit microprocessors, including the instruction set of MIL-STD-1750A. (A glossary of terms used in the text and figures is given in Appendix A.)

SYSTEM HARDWARE

System hardware is logically divided into two separate but interacting areas: the 16-bit computer itself and the logic that permits the user to interact with it for development and debugging purposes. The computer uses the 8-bit slice GP001[2] and the Sequencer GP502, but otherwise readily available CMOS RAMs and 74HC CMOS latches and registers to interconnect key system parts. For maximum speed, the EPIC chips should be operated at 10 volts, but since this rating conflicts with that of the 74HC logic family, and since speed in not a primary factor in this design, the system is run at 5 volts. This voltage level is satisfactory for demonstrating concepts and for evaluation, and avoids the need for voltage-level converters.

The Computer

The 16-bit computer configuration is shown in Fig. 1 in block form. (Complete logic drawings are contained in Appendix B.) The processing section contains two concatenated GP001 8-bit slices. The control section in Fig. 1 consists of a microprogram memory and the GP502 sequencer with additional logic as mapper ROM and condition-code multiplexer. (In the final hardware design, the mapper ROM was eliminated for reasons which are explained below.) The micromemory is 256 words deep, with a nonencoded horizontal microinstruction length of 64 bits. Horizontal microprogramming provides dedicated control lines for each micro-operation, and therefore a maximum number of operations are performed in parallel in one microcycle. The micromemory is implemented as a writable control store, WCS, and uses 74HC574 octal registers for the pipeline. The pipeline, which is on the output of the micromemory, is optional, but permits overlapping of fetch and execute cycles, thus increasing throughput. The 2k x 8 CDM6116 CMOS RAM chips can accommodate an 11-bit address input from the sequencer. However, only an 8-bit address is used. An 8-bit field in the microword format is dedicated as a next-address field and enabled from the sequencer's pipeline register output, PL. Under 3-state control, the data input to the sequencer is provided by either the next-address field or the output of the mapper ROM.

The main memory is also implemented with 2k x 8 memory chips, for a 16-bit data format. Only the low byte of the 16-bit address bus addresses the main memory, so that the design is restricted to an effective memory of 256 words by 16 bits, which is sufficient for the demonstration of short application programs.

The addition of memory address registers, instruction registers, data in/out registers, clock and timing logic, and a scratchpad register for use as program counter, PC, completes the computer.

The architecture shown provides two ways of addressing the register file in the central processor unit, CPU. The operand part of the instruction may contain either the R or T address (4-bit address fields for ports 1 and 2, respectively), or the address may come directly from the microcode. A bit in the microword selects one of the two sources.

Most of the 16 control instructions for the sequencer are conditional, and depend on the input at the condition-code pin, $\overline{CC}$. Status signals from the CPU, such as carry-out, overflow, sign, all-zero-detect, and other system flags, are input to a multiplexer whose selected output is tested by the sequencer at pin $\overline{CC}$.

A typical mode of operation for the computer is as follows: The micromemory initiates a fetch of a macroinstruction from main memory (i.e., the pipeline register instructs the CPU to output the content of the PC to the memory address register, MAR, and enables MAR to the address bus). The instruction is read and loaded into the IR over the data bus.

*This Note illustrates and reduces to practice basic concepts outlined in ICAN-7226, "A Primer on Microprogramming and Bit-Slice Architecture Exemplified in Systems Using Members of the EPIC CMOS/SOS Family."

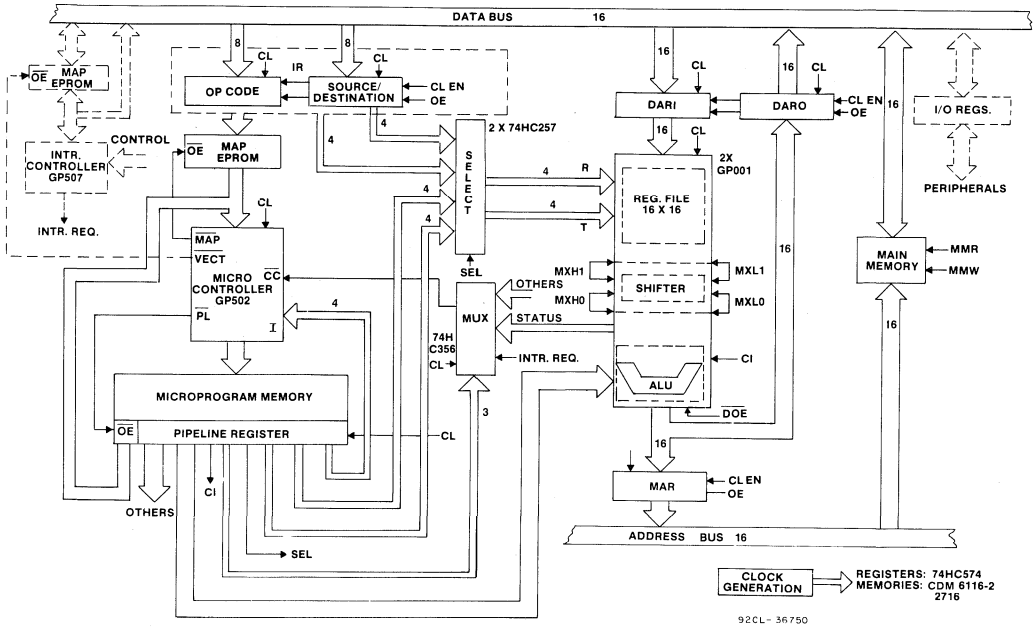


Fig. 1 - Block diagram of the 16-bit microprogrammable bit-slice microcomputer.

The opcode is next decoded by the controller, which outputs an address for the entry point of a microroutine that executes the fetched macroinstruction. The opcode is translated by the mapper ROM to the proper entry-point address. The content of the addressed micromemory location loads the pipeline register. The bits in the micromemory direct the CPU to execute the instruction and provide the necessary timing pulses to memory, registers, or other system components.

Development Aids

It is clear that some way must be found to access the inner workings of a design such as the one discussed so that its operation can be verified or modified, tested or debugged. In the absence of a dedicated bit-slice development system, it is still possible to develop software for small application programs and to do a fair amount of in-circuit emulation. The approach is to use a standard microprocessor development system and to design into the target system the necessary interface logic for user interaction. Fig. 2 shows how RCA's computer development system, CDS, for the CDP1800 microprocessor family is configured and used for developing hardware and software in a bit-slice target system. The CDS system itself, with floppy disks and terminal, can create, edit, and assemble files. The target system is run by a CDP1802-based microcomputer board, the CDP18S602,[3] and is interfaced through a board that supplies CDP1802 buses and control lines to the target system. The details of how the buses are interfaced into the bit-slice system are described in the sections that follow.

The CDP18S030 micromonitor[4] provides the in-circuit-emulation capabilities and runs under its operating system, MOPS,[5] called from CDOS (the operating system of CDS).[6] With these capabilities, the user can, from the system terminal, create or modify an object file and download into the target system's micromemory and main memory. He can verify or modify memory and read its contents on the machine's address and data buses during single stepping. Finally, a program can be uploaded back on disk for storage or modification.

The CPU

Two GP001 8-bit slices are concatenated to make up a 16-bit CPU. Most of the control fields operate on the bit-slices in parallel. An exception is the 3-bit field, C, the boundary and connect control field. For some CPU operations, the most significant and least significant C-fields must be controlled independently. The shift pins are cascaded so that the most significant shift bit leads, MXH, are connected directly to the least significant shift bit leads, MXL, of the next more significant slice. Note that the most significant leads, MXH, are looped back to the least significant leads, MXL, through links. This arrangement allows ring-shift operation with no external parts. The shift pins, MXH/MXL, together with separate carry-out and all-zero-detect leads, provide status information about the arithmetic logic unit, ALU. The status word consists of overflow, sign, carry-out, and accumulator-equal-zero bits. The bits are under microword control and are clocked into a multiplexer, 74HC356. The status bits are selected and tested at the $\overline{CC}$ input of the microcontroller by a 3-bit select field supplied to the multiplexer from the microword. Note that the AZ0 leads, which are bused together, require a pull-up resistor. Overflow of the ALU is indicated on the MXH1 line, which is timeshared.

The address fields R and T for the register file can be derived from one of two sources. One bit in the microword (μ39) selects either the pipeline register or the operand part of the instruction register as source.

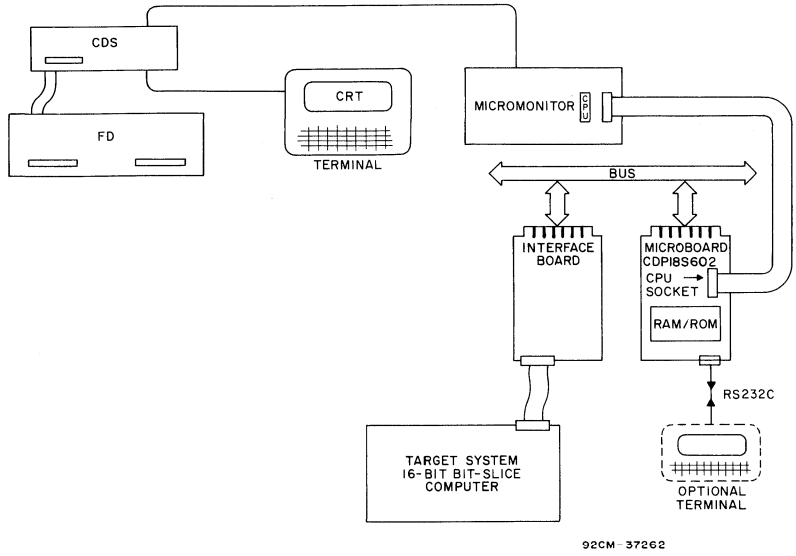


Fig. 2 - System configuration for development and in-circuit emulation.

The Microcontroller

The main purpose of any microcontroller is to present an address to the microprogram memory so that a microinstruction is fetched and executed. Controllers or sequencers without branching capabilities may be implemented for simple sequential control circuits. In the simplest form of sequencer, only an address counter is required for stepping through the microinstructions. The address of the next microinstruction is selected by incrementing the address counter by one on each clock cycle. This feature is included in the design example; it allows simple debugging of the CPU section without concern for proper operation of a complex controller. Fig. 3 and Appendix Fig. B-1 show the use of the CD4520 as a simple 8-bit address counter. The working controller in this

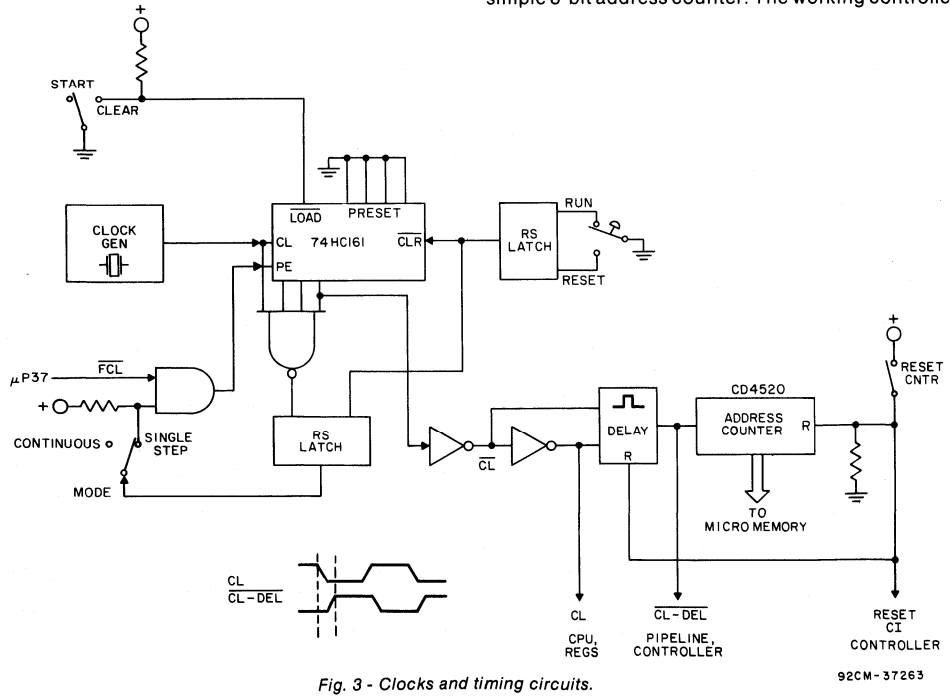


Fig. 3 - Clocks and timing circuits.

design is, however, the GP502, which, like the GP001, is fabricated in CMOS/SOS technology. The GP502 is functionally and pin equivalent to the popular industry standard AM2910. Although the part allows addressing of up to 4k words of microprogram, only 8-bit input and output fields are wired.

The $\overline{MAP}$ line (see Appendix A) is only active during a JMAP (Jump Map) instruction, and normally enables the mapper ROM to the controller's input. In this design, for simplicity, the mapper ROM is eliminated, and the MAP line is used to enable the IR directly to the input of the controller.

The register load, $\overline{RLD}$, and the condition-code enable, $\overline{CCEN}$, inputs are under pipeline control, but a linking arrangement permits the inputs to be hardwired. The $\overline{FULL}$ pin, which indicates a stack full status, is wired to the multiplexer input (U43) and becomes part of the status word.

When the carry-in, CI, to the controller is high, the microprogram counter is loaded on the next clock cycle with the current output word plus one. Sequential microinstructions are thus executed. When the CI is low, the incrementer passes the output word unmodified, so that the microprogram counter is reloaded with the same word on the next clock cycle. The same microinstruction is thus executed any number of times. This feature is used in this computer to set a breakpoint in program execution. Pipeline bit μ32 halts execution by setting a flip-flop.

Micromemory

The microprogram memory is a writable control store, WCS, and is organized as 256 words by 64 bits, although the CDM6116 RAM chip, with an access time of 120 nanoseconds, allows expansion to 2k words, as shown in Fig. 4. Octal edge-triggered registers on the positive-going clock edge are used for the pipeline. Eight bits in the pipeline are output enabled by the $\overline{PL}$ line from the controller, and used as a branch address to the input of the controller, μ63 - μ56.

The CDP1802-based CDS system has access to the micromemory through its data and address buses. The data bus is isolated by bidirectional 3-state buffers, 74HC245, and the address bus by a CDP1874 buffer.

The micromemory, decoded, occupies memory space F000-F7FF in the CDS system, and has eight chip-select outputs for writing or reading data. Microword 0 is loaded from address locations F000-F007 in the CDS system, microword 1 is loaded from F008-F00F, and so on. When the CDS system is selected from the micromemory, all 64 bits in one word are read in parallel.

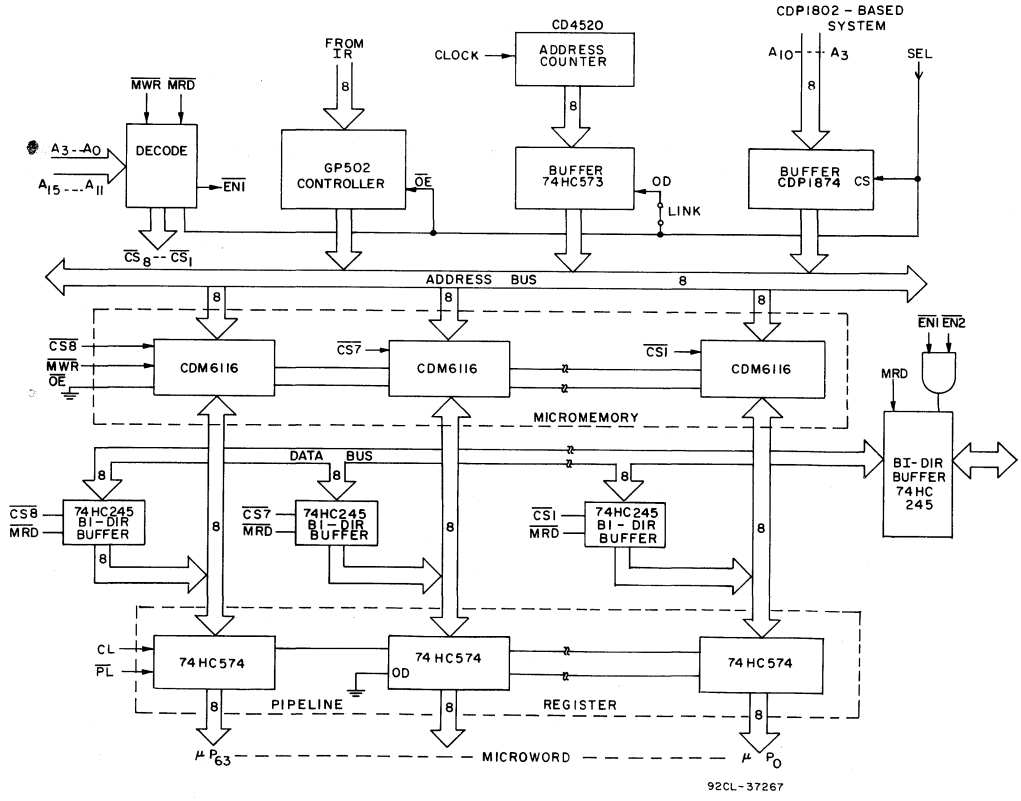


Fig. 4 - Micromemory with control circuits and address sequencers.

Main Memory

Main memory is organized as 256 words by 16 bits, also using the CDM6116 RAM chip. When writing to or reading from the chips, they are considered to occupy memory space E000 - E1FF in the CDS system. Fig. 5 shows that address bit A0 selects one RAM chip for even addresses and the other one for odd addresses. Hence, main-memory word 0 is loaded from E000 - E001, word 1 from E002 - E003 and so on. Note that the memory is restricted to 256 words only because the low byte of the 16-bit address from the bit-slice computer is wired.

Main memory is accessed from the CDS system similarly as described for the micromemory by using octal 3-state buffers. Main memory is written to or read from in the bit-slice computer by pipeline control bits μ30 (MEMW) and μ29 (MEMR).

Timing, Running and Single Stepping

All timing in the computer is derived from a 4-MHz crystal oscillator, as shown in Fig. 3. With switches in the Start and Continuous positions, the 74HC161 acts as a simple counter and generates a steady clock signal. The pipeline and the controllers are clocked on the positive-going edge of $\overline{\text{CL-DEL}}$ (delayed clock). When the microword instruction becomes valid a few nanoseconds later, previous write operations in the CPU on the negative-going edge must be complete, hence the slight delay between the two clock edges.

For single stepping, the mode switch is simply moved from Continuous to Single Step. The 74HC161 counter is held disabled with the run/reset switch in the Run position. When the switch is moved to Reset, the counter is held reset, but the input latch is cleared. The counter, which stays reset until the switch is released to the Run position, counts up until the decoder gate generates a pulse to set the input latch and disable the counter. The result is a single pulse, always generated in the same phase.

Two means are provided for stopping execution on a specific address. Bit 37 in the pipeline freezes the clock if it is low; bit 32 clocks a flip-flop and sets CI low at the controller, which has the effect of executing the same instruction over and over.

When using the run mode, the start switch is first switched to Clear. This resets the counter (clock pulse, CP, reset is 0), thus ensuring that the clock always starts in the same phase.

Debugging with the CDS System

The interface board shown in Fig. 2, with the logic in Fig. B-4, Appendix B, extends the host computer's data and address bus, contained on the CDP18S602 Microboard, into the 16-bit bit-slice computer. Additionally, the card provides five select lines, SEL-2 through SEL-6, which are required for interactive control. These select lines follow the convention for CDP1802 two-level I/O control; a board select command must be given to activate them. The command is OUT1:DC F0, which designates the group select address at F0.

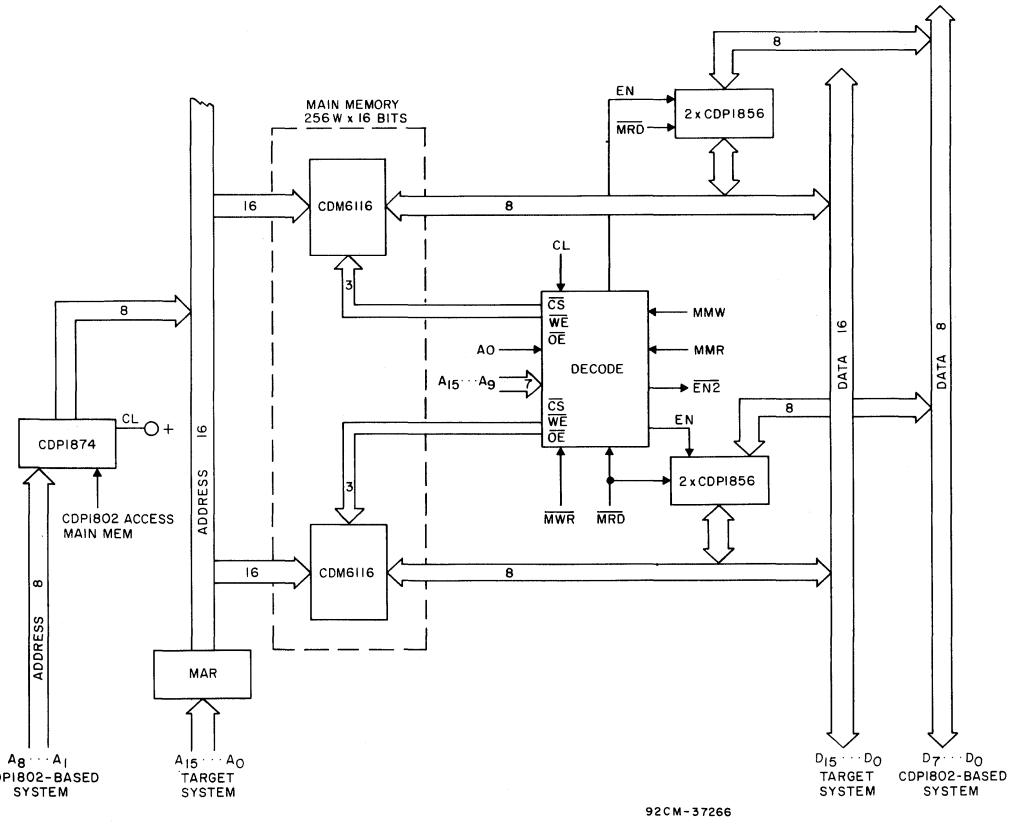


Fig. 5 - Main memory with control circuits.

To write into or read from micromemory, the I/O command OUT2;DC 01 is given at the keyboard. This command enables the CDP1802 address bus onto the micromemory's address bus and at the same time isolates the address counter (U24) or the other controller (GP502) from the bus. A link selects either the address counter or the GP502 as the controller. When the link is out, the GP502 can be activated by closing the output disable switch. The OUT command also primes the chip selects for the memory, since only one byte at a time can be read or written.

The main memory is selected with the command OUT2;DC 02, provided the board select line is already active. Main memory is then under control of the CDS system. To relinquish control, in order to run the target system, the command OUT2;DC 00 is given.

The contents of the 16-bit address and data buses can be read at any time while single stepping to verify what is happening in the machine. The contents are obtained, from the keyboard, by the input commands INP3 through INP6.

PROGRAMMING OF MICROCODE

The programmer is always concerned with two levels of programming; the macrolevel and the microlevel. One of the major advantages of microprogramming is that an existing instruction set can be emulated or an optimum instruction set constructed for a specific application. To demonstrate the general approach, and how the machine works, a few typical macroinstructions (machine level) are defined below. The coding of sequences of micro-instructions which define the macroinstructions is also given.

Instruction Format

Fig. 6 shows six different macroinstructions and their formats. The eight most significant bits in each comprise the operational code, OP; the following eight bits are operand source designators. The T and the R designate address fields for the CPU's two-port register file. The first instruction word may be followed by another operand word which is either data or an address. Fig. 7 shows the assembly listing of a short demonstration program loaded into main memory. The instructions are defined as follows:

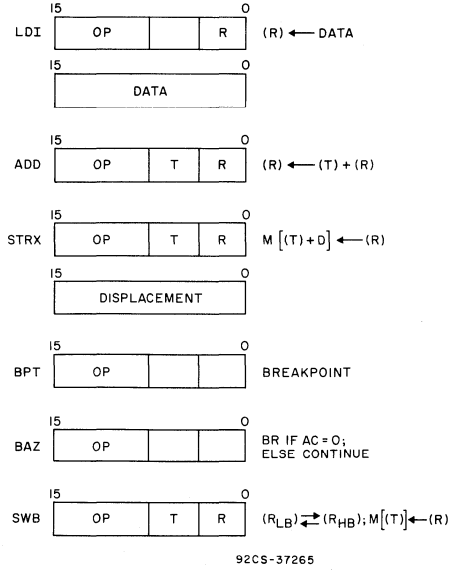


Fig. 6 - Macroinstruction formats.

LDI: Load immediate instruction, loads immediate data into the register addressed by the R field.

ADD: A register-to-register add instruction. It adds the contents of the register addressed by R to the contents addressed by T and stores the result into the register addressed by R.

STRX: A store instruction with indexed addressing. The contents of the register addressed by R are stored into a memory location whose address is computed. The effective address is the sum of the displacement plus the contents of the memory location addressed by the register designated by T.

BPT: A breakpoint trap; i.e., execution stops.

BAZ: A conditional branch instruction. If the accumulator, AC, is zero, the program branches, otherwise it continues.

SWB: A swap byte and store instruction. The two bytes in the register addressed by R are swapped and the result is stored in the memory location addressed by the content of the register designated by T.

These instructions are loaded into main memory in a short demonstration program, whose assembly listing may look like the one in Fig. 7.

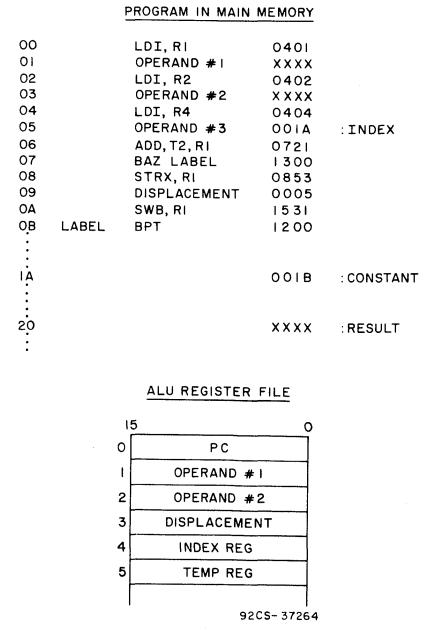


Fig. 7 - Assembly listing and register assignments.

The program of Fig. 7 loads immediate data into registers 1, 2, and 4. The contents of registers 1 and 2 are added and the result written back into register 1. Next, a test is done on the ALU's accumulator. If it is zero, the program branches and stops; otherwise it continues with the STRX instruction. This instruction first finds the effective address 20_H by adding the displacement 5 to the contents of the memory location addressed by the index register. The contents of register 1 are then stored into the computed memory location. Finally the two bytes in register 1 are swapped, and the result stored into the previously computed memory location. The program then halts.

Examples of Microroutines

The sequences of microinstructions in this section define the macroinstructions described just above. A printout of the microcode for the example of Fig. 7 is given in Fig. 8. The addresses in Fig. 8 refer to address space in the CDS system. Note the order in which the bytes are loaded: Word 0 consists of pipeline bits μ7-0, μ15-8, μ23-16, μ31-24, and so on. The other two printouts in Fig. 8 show the contents of main memory.

```
FILE: ADDX. H7                DISK: BSLICE

!M
F000  7800 C91D E08E 0000  F000 891F E88E 0000;
F010  0000 493C F08E 0000  0000 C91C E082 0000;
F020  F000 891F E88E 0000  0000 493C E28E 0000;
F030  0100 C910 6087 0001  5000 D19D 6087 0001;
F040  F000 891F E88E 0000  0000 493C E28E 0000;
F050  0103 C910 E08E 0000  4C40 891C E88E 0000;
F060  0000 493C E28E 0000  0105 C910 E08E 0000;
F070  5000 C91D 608E 0000  7C03 891C E88E 0000;
F080  7C01 891C E48E 0000  0000 494C E087 0001;
F090  0000 C91C E183 0012  0000 C91C E003 0001;
F0A0  0000 C91C E087 0012  0000 C91C E08C 0003;
F0B0  0000 C91C E08E 0003  7C00 C91B 6089 0017;
F0C0  4C30 891C 688E 0000  7C01 891C 648E 0000;
F0D0  0000 494C E087 0001  0000 0000 0000 0000;
F0E0  FF
```

MICRO PROGRAM

```
FILE: ADDXR. H8               DISK: BSLICE

!M
E000  0401 FFFF 0402 0001  0404 001A 0721 1300;
E010  0853 0005 1531 1200  0000 FFFF 0810 FEFC;
E020  0684 ED5B 0000 FFFF  0000 FFFF 010E F4FC;
E030  5200 FFED 001B FFFF  0000 FFFF EA20 F0F4
E040  0000 F375 0000 FFFF  0000 FFFF 00A0 F6EC;
E050  98
```

MAIN MEMORY – AC = 0

```
FILE: ADDXR. H7               DISK: BSLICE

!M
E000  0401 1234 0402 3124  0404 001A 0721 1300;
E010  0853 0005 1531 1200  0000 FFFF 0810 FEFC;
E020  0684 ED5B 0000 FFFF  0000 FFFF 010E F4FC;
E030  5200 FFED 001B FFFF  0000 FFFF EA20 F0F4;
E040  5843 F375 0000 FFFF  0000 FFFF 00A0 F6EC;
E050  98
```

MAIN MEMORY – AC ≠ 0

92CS-37259

Fig. 8 - Object code in micro and main memories.

The first run was made with the two operands, 1234 and 3124, which add up to 4358. Since the result is not equal to zero, the program continues and loads location 20_H with the bytes swapped, 5843. In the next example, the operands were FFFF and 0001, which generate an accumulator equal to zero. Hence, the program stops without storing the result. (The 0000 content in location 20_H was random data at start-up.)

Refer to the coding table, Appendix C, when going through this example. The table headings contain labels, numbers, and functions of the pipeline bits. Note that bits 48 through 55 are not used. They are spares, but their location must be considered when loading physical micromemory. This discussion concentrates only on those bits which are relevant. Most are don't cares, but are coded as zeroes since binary logic does not handle don't-care symbols.

Initialization - The microprogram counter must be initialized to start at zero. There are several ways to do this. In this design, pull-ups on the micromemory address bus force the output of the controller into the 3-state. The control instruction JZ (μ43 - μ40) is then loaded into location FF. JZ specifies that the next microinstruction is at location 0. Note that registers DAO (Data Out), DAI (Data In), and MAR are disabled at address FF. By single-stepping once, bus contention is avoided and main memory can be loaded from the CDS system. The next word at address 00 sets the main-memory program counter to zero. The ALU function AND is selected, with the right data type set equal to zero. The result, a zero from the accumulator, is written back into register 0, which is assigned as the main-program counter. Outputs from the DAO, DAI, MAR, and the CPU are disabled. The instruction to the GP502 is E, which means continue to the next microinstruction.

Fetch - The fetch instruction has three microcycles, which are shared by all macroinstructions. At address 01, the MAR is loaded with the contents of the PC and the PC is updated. The ALU function ADD is selected, with the right data type set equal to zero (D is 111). The contents of the PC (register 0) are read and enabled out by the data output enable, DOE, (μ22) being low. Since the clock enable (μ35) for the MAR is high, the MAR is loaded on the positive-going edge of the clock. During the same microcycle, the carry-in is 1, so that the contents of the PC are incremented. M is 111, and the incremented output of the PC is written back into the PC. The instruction to the GP502 is, again, E, or continue to the next instruction.

At address 02, the MAR is enabled to the bus and the opcode is read from main memory and loaded into the IR. Bit μ23 is low, which enables the output from MAR. At the same time, μ29 (MEMR) is high, and the memory is read. As IR CLEN (Clock Enable) (μ36) is high, the opcode is clocked into the IR during this same cycle. Note that the M field for the ALU is 100, which inhibits the writing of data into the register file during this cycle. The GP502 instruction is, once again, continue to the next instruction.

Address 03 simply decodes the opcode. The GP502 instruction is JMAP, which sets the $\overline{\text{MAP}}$ output of the controller low. This line is normally used to enable the mapper ROM to the controller's input. In this design, the $\overline{\text{MAP}}$ signal enables the IR to the controller directly. Once more, the writing of data into the CPU's register file is inhibited.

LDI - Execution of this instruction starts at micromemory address 04. Since it is an immediate instruction, the PC is first programmed to fetch the operand. The instruction is, therefore, identical to the one at location 01. At address 05, the operand is read as at address 02, but data is clocked into DAI instead of IR. The program continues (I (a 4-bit input field) = E) until the last step, when the operand is written into register 1 in the file. The CPU fields M = 000 and S = 01 designate the source of write data, the direct input data input, DI, of the CPU. As bit μ27 is low, DAI is enabled as the data input source. Note also that μ39 is low. This bit selects the operand part of the IR as the source for the T and R address fields. The GP502 instruction is JPR (I = 7). This is a conditional jump instruction which is here forced to pass with $\overline{\text{CCEN}}$ (μ47) equal to 1. The next address is the branch address in the pipeline, 01, which commands the program to fetch another instruction.

ADD - The ADD opcode starts at location 07, and only one microcycle is required. The ALU function A = 01 is ADD, and with M = 101, the output of the ALU is the write source for the register addressed by R. Note that RTSEL (RT Select) (μ39) is 0, so that the source for the address fields T and R is the low byte of the IR; T = 2 and R = 1 is contained in the macroinstruction format. I is 7, which brings the microprogram counter back to 01 and another fetch operation.

STRX - This is a relatively complex instruction because of the indexed addressing mode. The steps at locations 08 and 09 are identical to the ones at 04 and 05. The instruction fetches an operand, here displacement. At location 0A, the displacement previously clocked into DAI is enabled as a write source for input to register R3. Next, the contents of the index register, R4, are loaded into the MAR. Another fetch is performed in 0C, and in 0D the read data is stored in register R5, which is used as a temporary register. The microcycle at address 0E adds the two fetched numbers and stores the result, the formulated address, in R3. Since the RTSEL bit (μ39) is 0, the T and R fields are derived from the IR register. In 0F, the new address is clocked into the MAR. The data to be stored in memory is found in R1. The contents of location 10 are read and clocked into theDAO. Note that DOE is 0, and that DAO CLEN is 1. Finally, at address 11, the write operation takes place. MAR and DAO are enabled and the write command is issued, MEMW = 1. The last microcycle also contains the JRP instruction for another fetch.

BAZ - Following execution of the ADD instruction in the assembly program, Fig. 7, the contents of the accumulator are tested for zero. The microinstruction ADD at address 07 also updates the status word. The all-zero output, AZO, is bit 0 in the status word, which is updated in the multiplexer's register (U43) during each microcycle, provided μ31 enables the clock input. Note also that in address 07, the CPU boundary control field for the most significant slice is C = 010. These C-bits provide overflow status on line MXH1, which is assigned as bit 2 in the status word. In microword 13, the AZO bit in the condition-code multiplexer is selected with μ46 - μ44 = 000. By setting $\overline{\text{CCEN}}$ to 0 (μ47) and I to 3 (CJP (Conditional Jump Pipeline)), the conditional test fails if AZO is 1, and the microprogram controller is incremented to 14. The JRP instruction is placed at address 14 with $\overline{\text{CCEN}}$ high. This condition forces a jump to the branch address 12, where the breakpoint instruction is located. If the test passes, i.e., AC is not 0, the program branches to the pipeline address 01, which starts another fetch.

BPT - Bit μ32 in the BPT instruction clocks a flip-flop that sets the CI to the controller low. The microprogram controller cannot increment, and the effect is to execute the same instruction over and over or, essentially, to branch an instruction to itself.

SWB - The opcode for the SWB instruction provides the start address at 15. The swapping of the two bytes in a word is easily done by rotating the contents right four times, two bits at a time. The first microcycle sets up a loop counter in the controller with a number one less than the count. At address 17, M is 011, which programs a shift right and rotate of two bits with C = 001, the standard interconnect control. Note that the two CPU slices are interconnected for a ring shift. The ALU function is an OR with the right data type operand set to 0. The output of the shifter is the write source for data to be loaded back into a register. Register address R1 is contained in the macroinstruction.

The three last steps write the result back into memory, similarly to the steps in addresses 0F, 10, and 11. The effective address was computed earlier and is in R3. The byte-swapped word is in R1.

CONCLUSIONS

This Note describes a complete design for a 16-bit bit-slice microprogrammable computer, such as the one shown in Fig. 9, using two key building blocks from EPIC family (the GP001 and GP502), and demonstrates the fundamental principles involved. The design can be expanded to meet specific performance goals.

Typically, the system can easily accommodate an interrupt controller, such as the GP507. The interrupt request is simply another input to the condition-code multiplexer. The interrupt could be handled at microlevel by modifying the fetch routine so that it always tests for interrupt.

Parallel I/O ports or UARTs can be added to the bus structure and controlled by additional pipeline signals.

To increase throughput during multiplication, a hardware multiplier, the 8 x 8-bit expandable unit GP503,[7] can be inserted between the CPU and the data bus.

For a more compact, lower-parts-count design, EPIC family members such as the register select unit, RSU, GP505 may be used. Typically, the RSU provides registers for selecting CPU address fields, generating bit masks, or expanding literal and byte data formats.

It should be clear from the sample program that the microprogramming technique provides the programmer with a very versatile tool. Note in the fetch routine in Appendix C, that during the microcycle at address 03, the ALU is idle. A considerable speed-up in run time can be obtained by using approach below.

```
FETCH:  MAR → BUS;  M(MAR) → IR;  CONT.
.....
FETCH + 1:  PC → MAR;  PC + 1 →PC;  JMAP

ADD:  R1 ← T2 + R1;  MAR → BUS;  M(MAR) → IR;  JPL
  (Go to Fetch + 1)
```

During the decode part of the fetch (FETCH + 1), the ALU is used to update the memory address register and the program counter. The Jump MAP instruction for the GP502 controller provides the start address for the execution part, for example, ADD. During this step, not only is the addition done, but the next macroinstruction is read from memory and clocked into the instruction register. The GP502's Jump Pipeline instruction branches back to FETCH + 1 for another update and decode of a new macroinstruction. In other words, the first part of the macroinstruction FETCH (the memory-read cycle) is overlapped with the last step in the execution routine for the previous macroinstruction. The execution routines must be written to conform with this technique.

Fig. 9 - 16-bit bit-slice target system connected to development aids for software/hardware development and in-circuit emulation.

ACKNOWLEDGMENT

The author gratefully acknowledges the help and contributions of Zachary Stern in implementing the design and debugging hardware and microcode.

REFERENCES and BIBLIOGRAPHY

1. **EPIC (Emulation and Programmable IC) Family** RCA Solid State Data Sheets:
   GP001 - 8-Bit General Processor Unit (GPU) - File No. 1324
   GP502 - Preliminary Data
   GP503 - 8-Bit by 8-Bit Multiplier - File No. 1323
   GP505 - Objective Data
   GP507 - Objective Data
2. **"An Introduction to the Use of the General Processor Unit, GP001,"** RCA Solid State Application Note ICAN-7202.
3. **"RCA COSMAC Microboard Computer, CDP18S602,"** RCA Solid State publication MB-602.
4. **"Instruction Manual for the RCA COSMAC Micromonitor CDP18S030,"** RCA Solid State publication MPM-218.
5. **"Micromonitor Operating System (MOPS) CDP18S831 User's Guide,"** RCA Solid State publication MPM-231.
6. **"Operator Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007,"** RCA Solid State publication MPM-232.
7. **"Applying the 8 x 8 CMOS/SOS Multiplier, GP503,"** RCA Solid State Application Note ICAN-7211.

Appendix A - Glossary of Terms

μ(n)	Micromemory bit (output of pipeline register)
A(n)-P	Address bit
AC	Accumulator
ALU	Arithmetic logic unit
AZO	All-zero output
BIU	Bus interface unit
BSEL	Board select
C	3-bit boundary and connect control field
CC	Condition code
CCEN	Condition-code enable
CDOS	Computer development system operating system
CDS	Computer development system
CI	Carry in
CJP	Conditional Jump Pipeline instruction
CL	Clock
CL-DEL	Clock delayed
CL-NDEL	Clock delayed negative
CL-P	Clock positive
CLEN	Clock enable
CLR	Clear
CO	Carry out
CP	Clock pulse
CPU	Central processor unit
CS	Chip select
D(n)	Data type operand field
DAI	Data in register
DAO	Data out register
DB(n)-P	Data bit
DI	Direct input data
DIR	Direction
DO	Direct output data
DOE	Data output enable
EN	Enable
EPIC	Emulation and programmable IC
FCL	Freeze clock
FULL	Status: stack full
I	4-bit input field (GP502)
INP(n)	Input commands (Micromonitor)
IR	Instruction register
IR CLEN	IR clock enable
JMAP	Jump Map instruction
JPR	Conditional Jump instruction
JRP	Conditional Jump R/PL instruction
JZ	Jump Zero instruction
LE	Latch enable
M	3-bit destination select field
MAP	Signal that enables a PROM that maps the macroinstruction to a microinstruction starting address
MAR	Memory address register
MEMR	Memory read
MEMW	Memory write
MMR	Main memory read
MMW	Main memory write
MOPS	Micromonitor operating system
MRD	Memory read (CDP1802)
MWR	Memory write (CDP1802)
MXH(n)	Most significant shift bit
MXL(n)	Least significant shift bit
M(n)	3-bit source select field
N(n)-P	3-bit I/O select field (CDP1802)
OE	Output enable
OP	Operation code
PC	Program counter
PL	Signal that enables the next address field of a pipeline register
R	4-bit address field for port 1
RLD	Register load
RSU	Register select unit
RTSEL	RT select
SEL-(n)	Select lines 1 through 5
S(n)	2-bit source select field
T	4-bit address field for port 2
TPA-P	Timing pulse A
TPB-P	Timing pulse B
UARTs	Universal asynchronous receiver transmitter
U(n)	IC device number
VECT	Signal that enables the vector output of an interrupt controller
WCS	Writable control store
WE	Write enable

Appendix B - System Logic Drawings

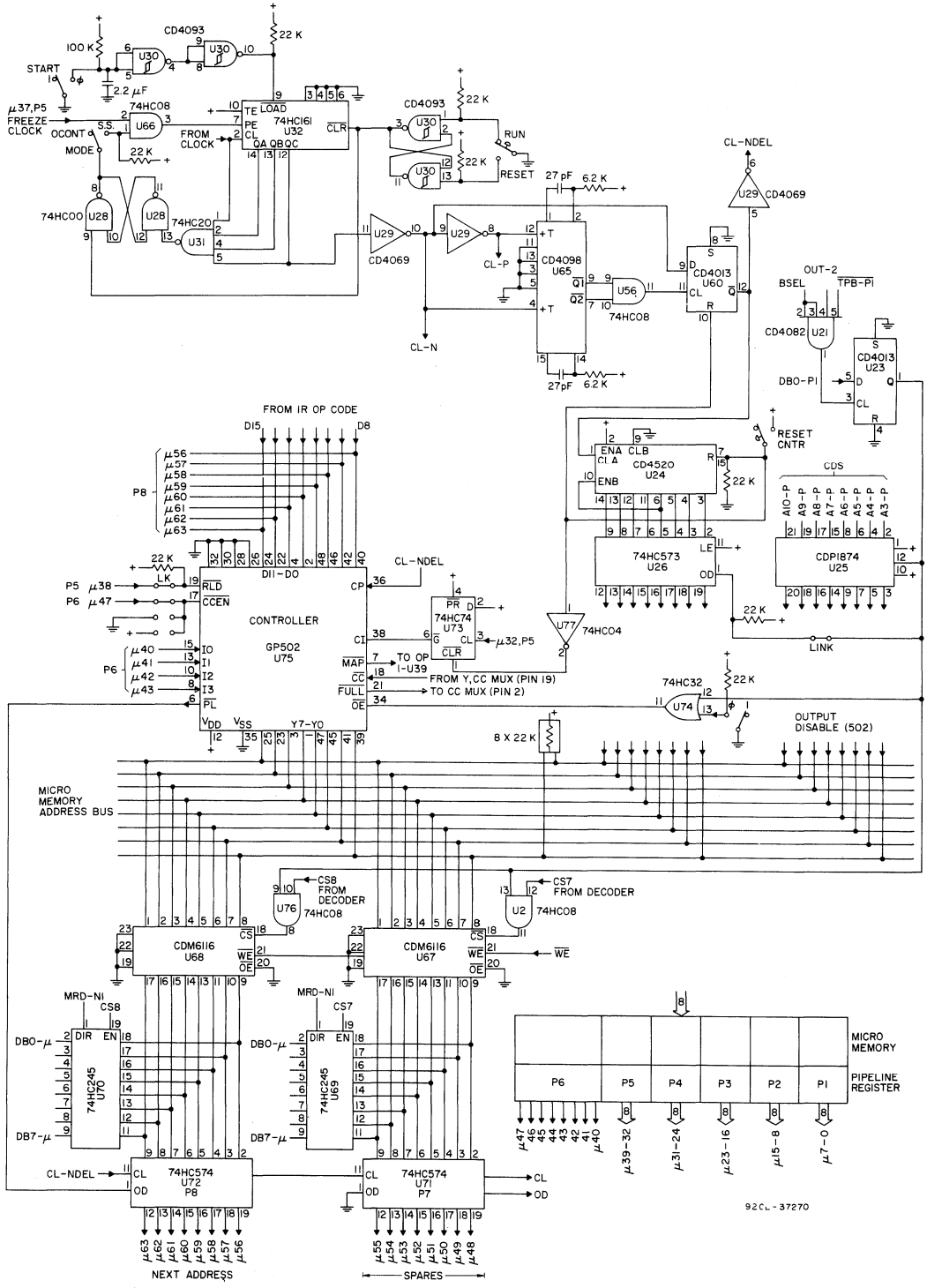


Fig. B-1 - Computer control section.

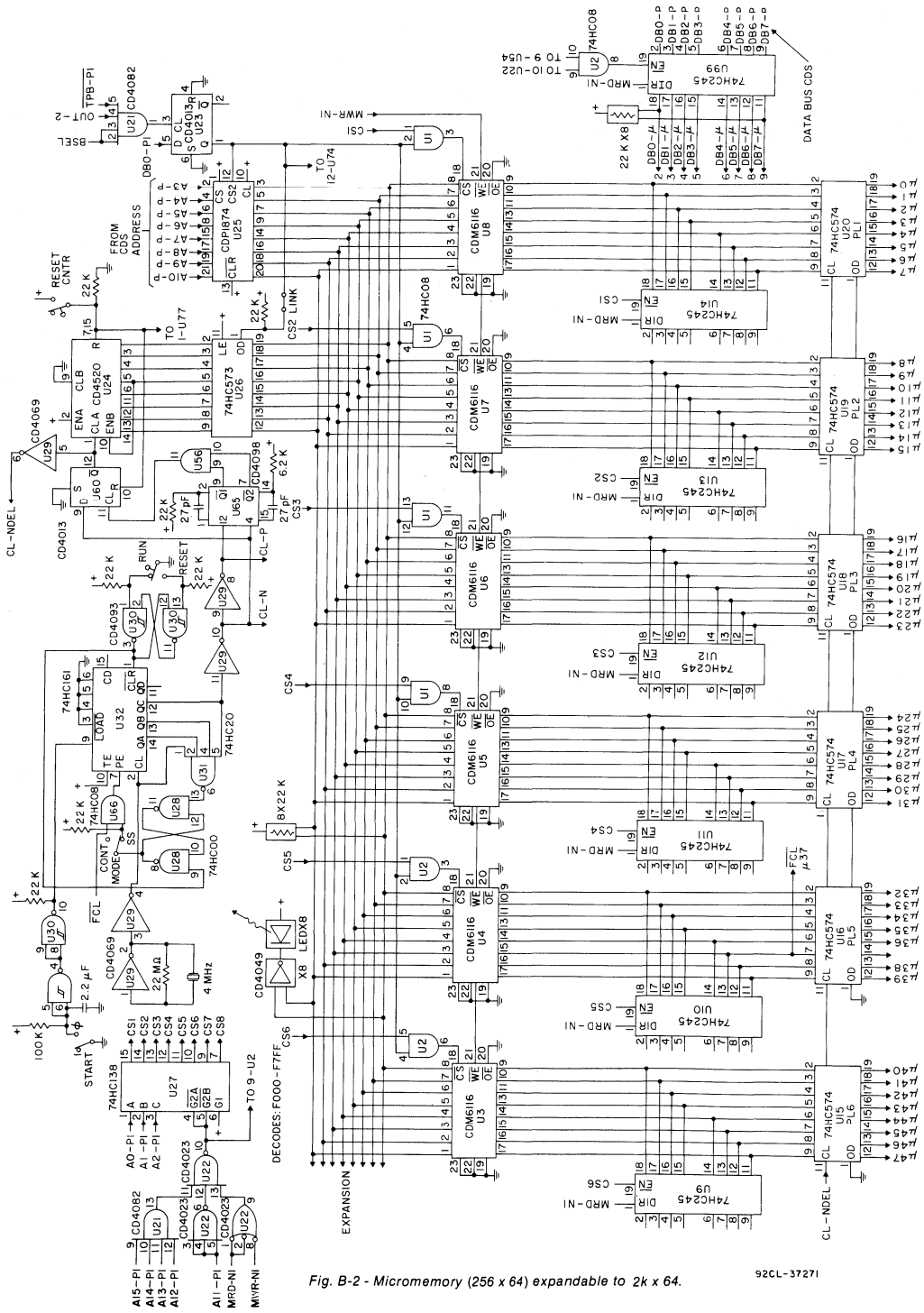


Fig. B-2 - Micromemory (256 x 64) expandable to 2k x 64.

ICAN-7241

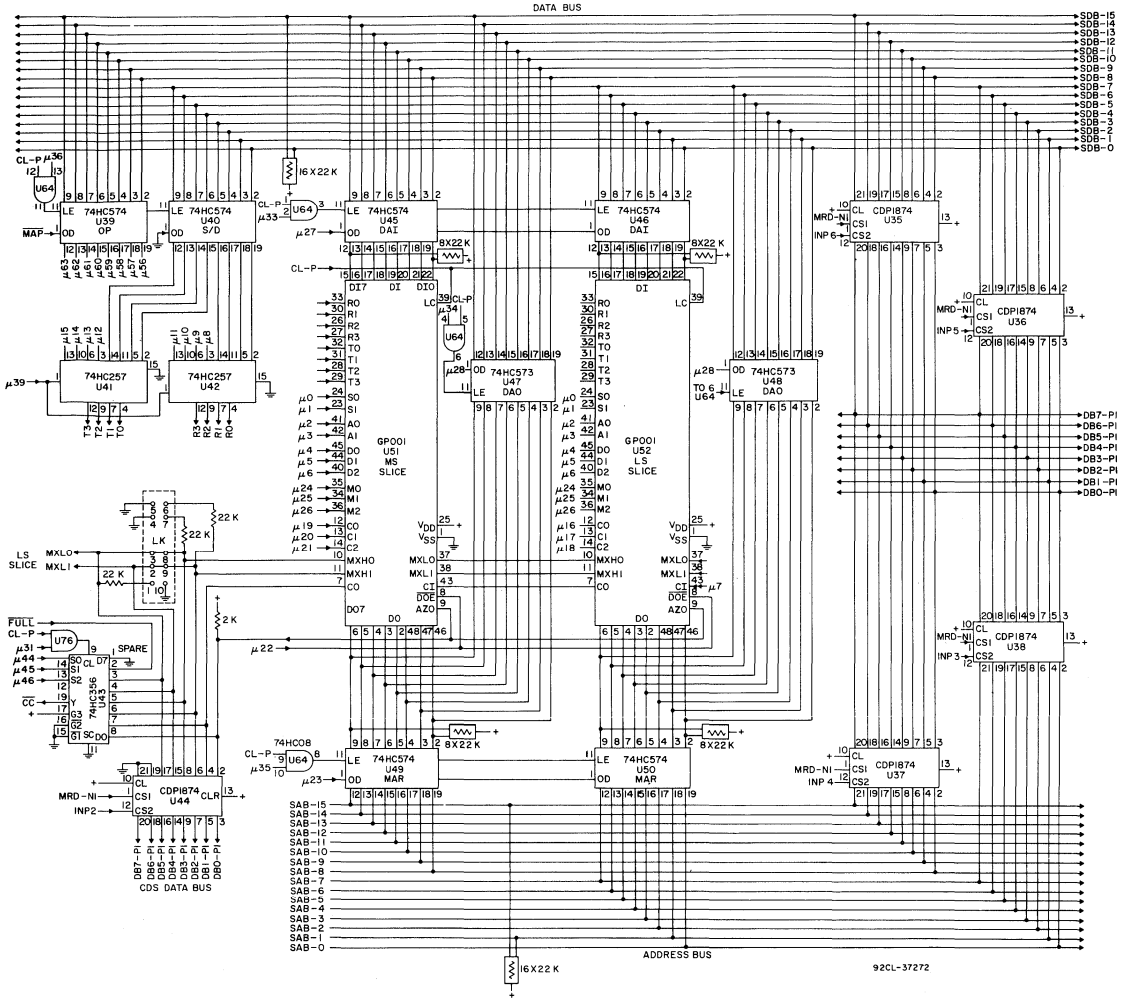


Fig. B-3 - 16-bit bit-slice central-processor-unit section.

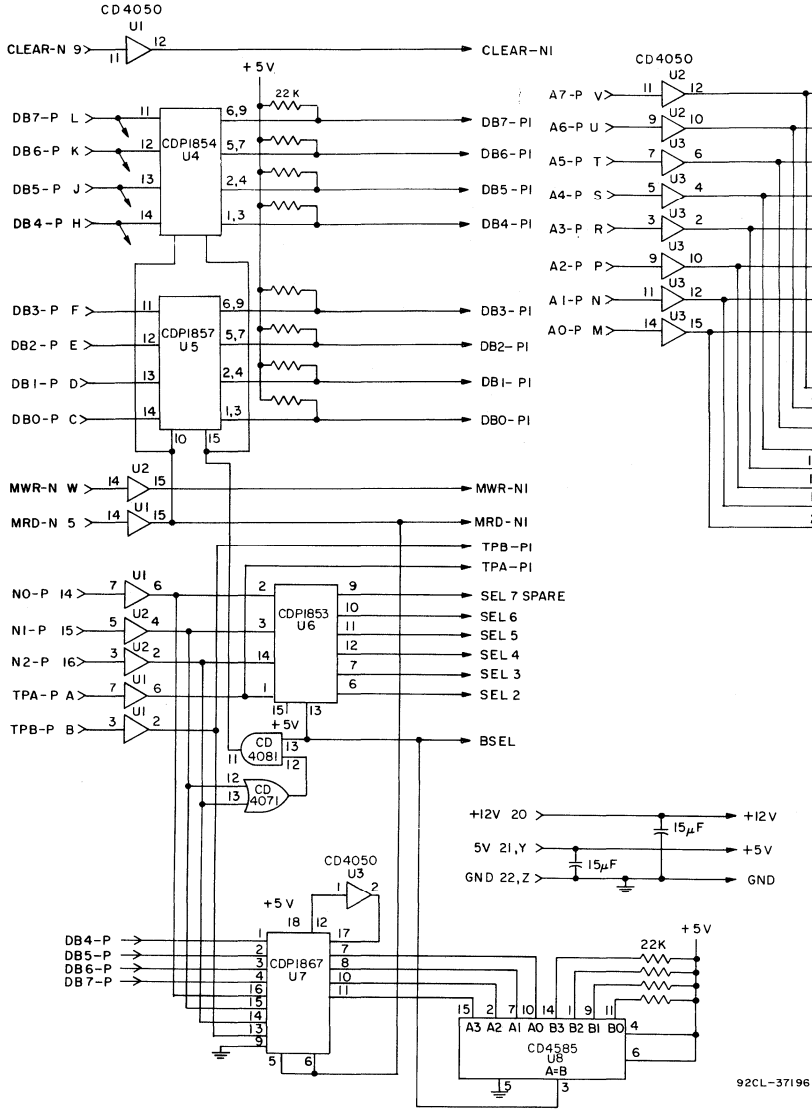


Fig. B-4 - Interface card CDS system to target system.

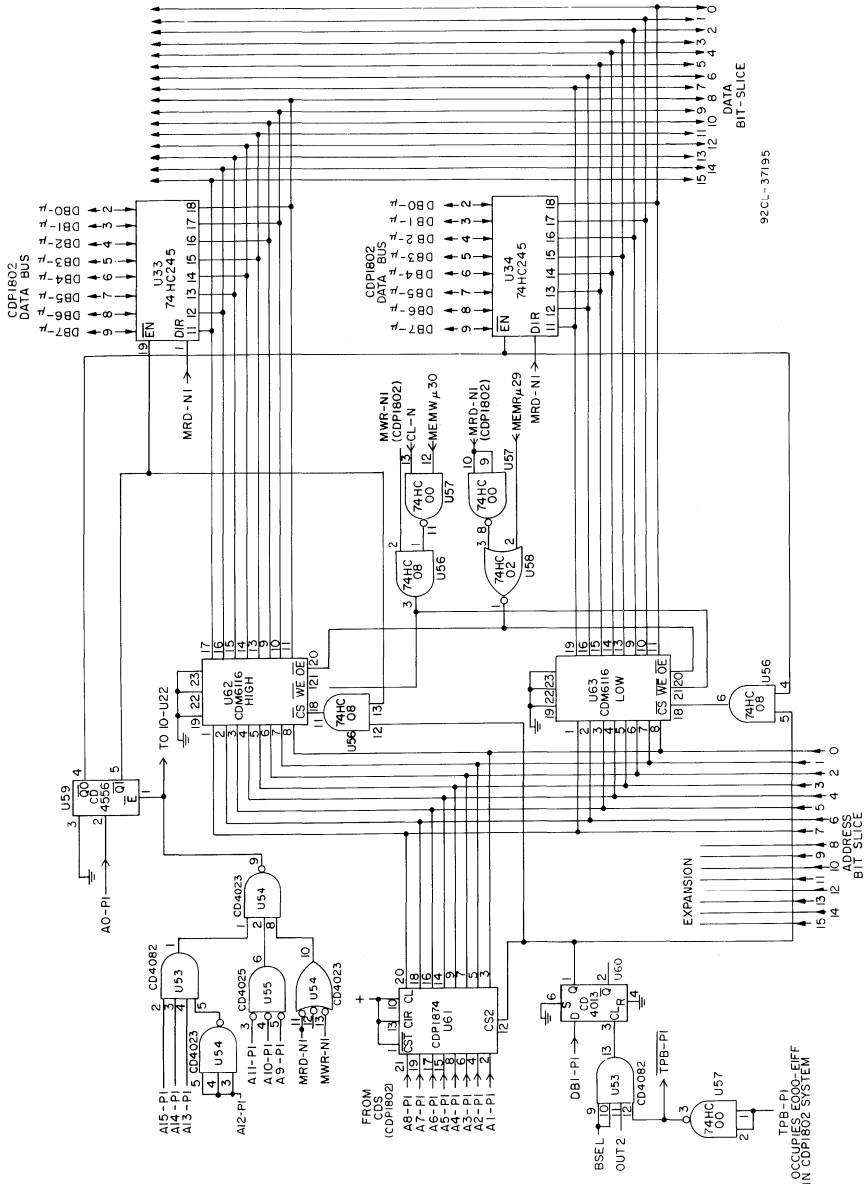


Fig. B-5 - System main memory (256 x 16) expandable to 2k x 16.

Appendix C - Coding Table

CODING TABLE

PIPELINE BITS	ADDR	63	62	61	60	59	58	57	56	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		NEXT ADDRESS								GP502 CCEN	CC SEL			GP502 CONTROL INSTRUCTION				RT SEL	GP502													GP001																			GP001								
											CCS2	CCS1	CCS0	I3	I2	I1	I0		RLD	FCL	IR CLKEN	MAR CLKEN	DAO CLKEN	DAI CLKEN	CICL	CC MUX EN	MEM W	MEM R	DAO OD	DAI OD	DEST CONTROL M2	DEST CONTROL M1	DEST CONTROL M0	MAR OD	DOE	MS SLICE C2	MS SLICE C1	MS SLICE C0	LS SLICE C2	LS SLICE C1	LS SLICE C0	T ADDRESS T3	T ADDRESS T2	T ADDRESS T1	T ADDRESS T0	R ADDRESS R3	R ADDRESS R2	R ADDRESS R1	R ADDRESS R0	CARRY IN C1	DATA SEL D2	DATA SEL D1	DATA SEL D0	ALU FUNC A1	ALU FUNC A0	SOURCE SEL S1	SOURCE SEL S0
INIT																																																											
CONTR 502 : 00→ μPC	FF	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPU 001 : 00→ PC	00	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
FETCH																																																										
PC→MAR : PC + 1→ PC	01	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	1	1	0	1	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
MAR→BUS ; M(MAR)→ IR	02	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
DECODE : JMAP	03	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
LDI																																																										
PC→MAR : PC + 1→ PC	04	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	1	1	0	1	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1
MAR→BUS ; M(MAR)→ DAI	05	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1
DAI→R1	06	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1
ADD																																																										
R1 ← T2 + R1 ; STATUS→CC MUX	07	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	1	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
STRX																																																										
PC→MAR ; PC + 1→ PC	08	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	1	1	1	0	1	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
MAR→BUS ; M(MAR)→ DAI	09	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	1	1	0	0	0	1	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1
DAI→R3	0A	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1
INDEX→ MAR	0B	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
MAR→BUS ; M(MAR)→ DAI	0C	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	1	1	0	0	0	1	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1
DAI→R5	0D	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1
R3 ← T5 + R3	0E	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1
FORM. ADDRESS→ MAR	0F	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
WORD→ DAO	10	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1
MAR→BUS ; M(MAR)←DAO	11	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
BPT																																																										
STOP ; Y→ μPC	12	0	0	0	1	0	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	1	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BAZ																																																									
TEST AZO	13	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
STOP	14	0	0	0	1	0	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	1	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SWB																																																									
COUNT→ REG/CNTR	15	0	0	0	0	0	0	1	1	1	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DO	16	0	0	0	0	0	1	1	1	1	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SHR. 2 BITS ; DEC CNTR	17	0	0	0	1	0	1	1	1	1	0	0	0	1	1	0	0	1	0	1	1	0	0	0	0	1	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FORM. ADDRESS→ MAR	18	0	0	0	1	0	0	0	1	1	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
WORD→ DAO	19	0	0	0	1	0	0	0	1	1	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MAR→BUS ; M(MAR)←DAO	1A	0	0	0	1	0	0	0	1	1	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

92CS-37258

Fig. C-1 - Coding table.

ICAN-7259

A Guide to the Emulating Microprogram Controller GP501—With Programming Examples

by K. Karstad

This Application Note introduces the Emulating Microcontroller (EMC) GP501, and surveys its physical characteristics and operational features. The emphasis is on describing the operation codes, or opcodes, and their use through a number of programming examples. The GP501 Microcontroller, fabricated in CMOS/SOS technology and having all the advantages associated with that technology, including high radiation tolerance, is relatively complex, with many sophisticated features, and has a flexibility and capabilities not found in other controllers. It is significantly different from other commercial controllers, such as the industry's workhorse, the AM2910; much of the external support required in an AM2900 design (condition-code register, mapping ROM, interrupt-vector ROM, multiplexers, latches, etc.) is not required in a similar EMC design. The system architecture for the EMC is shown in Fig. 1.

By providing a large number of internal registers for dedicated and semidedicated storage, a large number of single-bit I/O pins (here called discretes), a data bus port, a variety of ways to reduce and combine these data sources, and a variety of ways to alter the microcode program counter according to the status of the discrete inputs and/or other data values, the EMC incorporates into one part many of the subsystems and capabilities required in the control section of a bit-slice CPU.

Some features of the EMC, including speed characteristics, facilitate interfacing to the GP001, an 8-bit bit-slice CPU in the same EPIC (Emulation and Programmable IC) family.[1,2] However, these features do not affect efficient use of the EMC with any other bit-slice CPU.

Although this Note brings together in perspective all important features that a user needs to evaluate the EMC, no serious programming should be attempted without reference to the detailed user's guide.[3]

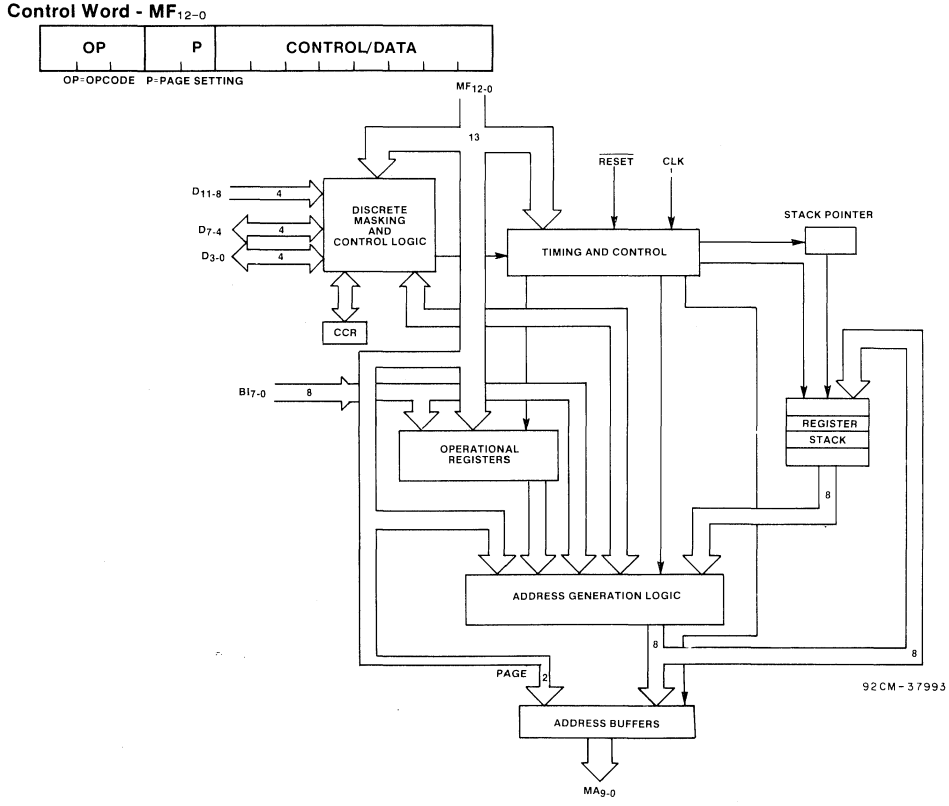


Fig. 1 - System architecture of the emulating microcontroller, GP501.

THE PHYSICAL INTERFACE

Fig. 2 shows a typical computer-control section using the GP501 EMC.

A 13-bit control word, MF, normally supplied from the pipeline register, contains a 3-bit opcode, a 2-bit page address and an 8-bit control/data field. The treatment of the control/data field varies with the opcode, and is covered below in detail. Four 256-byte pages are possible. The page field is normally passed through to the Memory Address Output field or lines, MA.

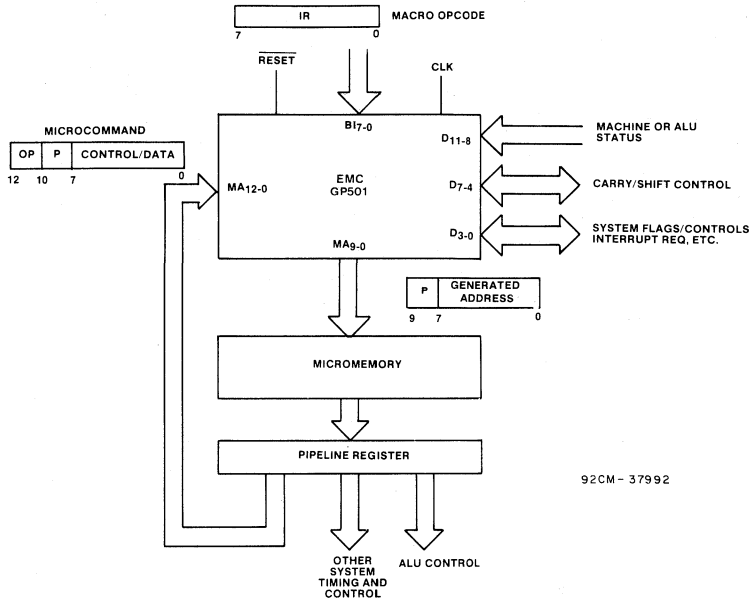


Fig. 2 - Typical control section using the GP501.

Memory Address Out MA_{9-0}

The Memory Address Output field is a 10-bit output field to micromemory. The two MSB's (most significant bits) are copied from the 2-bit page field in the control word input. The lower eight bits are generated from the EMC. The details of address formulation are found below under each operation code, or opcode, description.

Bus In BI_{7-0}

Eight bits of data can be latched into internal storage for subsequent use. A typical source is a macroinstruction opcode and extended bytes of the macroinstruction format.

Discrete Interface D_{11-0}

The Discrete Interface is divided into three four-bit groups:

D_{11-8} are always inputs to the EMC. A programmable XOR mask is applied internally to these bits; therefore, low-true or high-true data can be applied without external hardware or microcode provisions.

D_{7-4} are bidirectional but normally in the input mode.

D_{3-0} are independently alterable as inputs or outputs. From a functional viewpoint, these bits appear to the EMC to be four dual-ported, single-bit, data ports/latches.

Clock

A low-to-high transition denotes the beginning of a microcycle. Internally, both positive and negative clock edges are used to latch data presented to the EMC. In general, inputs should be stable prior to and during the time the clock is at a high level.

Reset

$\overline{\text{Reset}}$ is low true and does the following when active:

Clears all internal counter flags.
Clears Conditional Discrete Active flag
Sets the stack pointer to 0.
Forces the Memory Address Output to all zeros.

Note: The addressed stack register is not initialized to zero, and the load command (Opcode 4) is still active.

OPERATIONAL FEATURES

A large number of registers and latches are implemented on the GP50I chip; these are listed and summarized in Appendix Table A-1. Where and how the registers are used is covered primarily under the description of the opcodes. The registers fall generally into two groups; one group is under explicit program control, the other is not.

Stack Registers/Program Counter

The currently active stack register, the one of four pointed to by the stack pointer, is the program counter (PC). Normally, the PC is adjusted during the current microcycle so that it points to the next address at all times. The four stack registers permit three levels of microcode subroutines. The stack pointer wraps around in either direction, and there is no "stack full" status indication. The user can control the stack pointer only via the Reset input and through pushing or popping.

Branching and Sequence Control

Explicit Unconditional Branch and Unconditional Branch and Link instructions provide for single, direct-sequence control. In addition, the EMC offers a rich variety of sequence-control options that are available for use in conjunction with counters and the Conditional Discrete features. The options are listed below and detailed further in Appendix Table A-2.

Same address
Next address
Branch via branch register 0(R0 Branch)
Branch via branch register 1(R1 Branch)
Link
Branch and Link via branch register 1(R1 Branch and Link)
Return
Return and Link
Map (LSB [least significant bit] of address set according to Discrete Interface values)

Counting/Iteration

Two 8-bit counters may be used either to count clock cycles while following normal program flow (sequential counting) or to dwell on a particular instruction while counting clock cycles (iteration counting). The two counters may be nested.

Conditional Discrete Feature

The Conditional Discrete feature provides a means by which Discrete Interface bits may be tested and the results used in combination with branching options to provide a conditional two-way branching capability.

Mapping

The mapping feature allows values sampled at the Bus Interface (for example, a portion of the macroinstruction register) to be masked and merged with other values (stored internally) to generate the new Memory Address Output. This feature eliminates the need, as with an AM2910 implementation, for external mapping and/or interrupt vector ROMs/PLAs. The EMC's mapping feature provides a 256-way branch.

Translation

Translation is similar to mapping. Values at the Discrete Data Latch or at one of the four-bit-wide Discrete Interface groups, which typically reflect machine or ALU status, can be masked and merged with the current PC. The feature provides for a 16-way relative branch based upon current machine state.

Discrete Interface/CCR

The Discrete Interface architecture provides for completion of carry/shift paths between ALU slices, combining of and operation upon ALU flags, and the recording of discrete input states to an internal data latch. This discrete interface data latch can be used as a machine Condition Code Register (CCR). The content of the CCR may also be gated out to the Discrete Interface for use by the ALU, etc. Conditional two-way branches can be set up and tested directly without external circuitry.

INSTRUCTIONS FOR THE EMC

There are eight basic operation codes, or opcodes, but encoding of the 8-bit control/data field in the 13-bit microcommand provides for an unusually rich and powerful instruction set. For example, Opcode 7 offers sixteen different suboperations, or subops, and for many of these there are no less than 32 variants.

The 13-bit control word can be broken into four fields. The three MSBs define the opcode. The next two bits (MF9-MF8) are page bits that are generally passed through the controller. MF7-MF4 designate either a branch address or a control field. The four LSBs (MF3-MF0) can be a branch

address, a mask, a subcommand, or data to be loaded into a register-half or a counter-half.

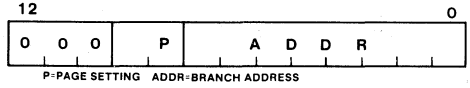
Appendix Table A-3 summarizes the eight basic instructions. It shows, for each opcode, the fields in the 13-bit control word (MF) and the result on the 10-bit Memory Address Output (MA) lines that address the micromemory. The actual use of some of these instructions may seem complex at first, but for a summary overview it is sufficient to keep in mind the purpose of any controller: to generate a next microprogram address.

In the two first instructions the 8-bit field is an Immediate Address field which is directly reflected on the output. In the remaining cases, the output is an address which is formulated or computed from the content of the eight LSBs in the control word. The result is generally a combination of bits derived from the interface (BI7-0, D11-0) and/or bits stored in internal operational registers and modified by an immediate mask in the control word. In some cases, internal logic operations are part of the process. Thus, in general, for the EMC, all inputs that affect the microcode sequencing are presented directly to the device (no additional hardware is required), and the next microprogram address is internally computed and presented at the MA output pins.

(The concluding section of this Note, Notes on the Use of Registers and Instructions, provides additional information on some of the material in this section.)

Opcode 0 - Unconditional Branch

Format



Operation

MA_{9-0} ← P:ADDR;

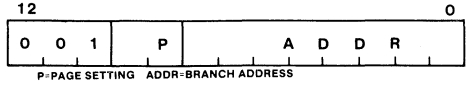
SR (SP) ← MA_{7-0} + 1;

Description

The 10-bit address specified by the page setting and control/data field (ADDR) becomes the Memory Address Output. The value of the lower eight bits of the new address is incremented and stored in the currently active stack register.

Opcode 1 - Unconditional Branch and Link

Format



Operation

MA_{9-0} ← P:ADDR;

SP ← SP + 1;

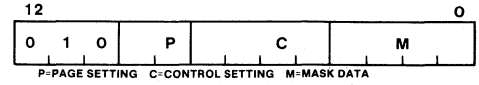
SR (SP) ← MA_{7-0} + 1;

Description

The 10-bit address specified by the page and address fields becomes the new Memory Address Output. The currently active stack register is not changed. The stack pointer is incremented (with wrap-around). The value of the lower eight bits of the new address is incremented and placed into the newly activated stack register.

Opcode 2 - Map

Format



Field	Information	
C - Control Setting	Address - High Nibble Formulation	Address - Low Nibble Formulation
0000	BI_{7-4} V Mask+	BI_{3-0}
0001	BI_{7-4} V Mask	$R3_{3-0}$
0010	$R3_{7-4}$ V Mask	BI_{3-0}
0011	$R3_{7-4}$ V Mask	$R3_{3-0}$
0100	BI_{7-4}	RJ (0, BI_{3-0}, Mask)*
0101	BI_{7-4}	RJ (0, $R3_{3-0}$, Mask)
0110	$R3_{7-4}$	RJ (0, BI_{3-0}, Mask)
0111	$R3_{7-4}$	RJ (0, $R3_{3-0}$, Mask)
1000	$R2_{3-0}$	RJ (0, BI_{3-0}, Mask)
1001	$R2_{3-0}$	RJ (0, $R3_{3-0}$, Mask)
1010	$R2_{3-0}$	RJ (0, BI_{7-4}, Mask)
1011	$R2_{3-0}$	RJ (0, $R3_{7-4}$, Mask)
1100	$R2_{7-4}$	RJ (0, BI_{3-0}, Mask)
1101	$R2_{7-4}$	RJ (0, $R3_{3-0}$, Mask)
1110	$R2_{7-4}$	RJ (0, BI_{7-4}, Mask)
1111	$R2_{7-4}$	RJ (0, $R3_{7-4}$, Mask)

+ - V = OR

* - RJ = Right Justify function (See Appendix Table A-4)

Operation

MA_{9-0} ← P: Formulated Address (see text);

SR (SP) ← MA_{7-0} + 1;

Description

The control and mask fields are used to formulate a new 8-bit address, as described below. This address is concatenated to the page setting to yield the new Memory Address Output. The 8-bit address is incremented and stored in the currently active stack register.

The new address is formulated from some combination of the value present at the bus interface, the value in operational register R3, and the content of the mapping register pair ($R2_{7-4}$, $R2_{3-0}$). The mask data is used as either a mask for the high nibble of the new address or as a bit selection map when applied to the low nibble through the Right Justify function. See Appendix Table A-4 for a description of the Right Justify function. Sixteen different address formulations are possible.

Example 1

C = 8, M = 4, R2 = $F1_H$

R3 = 23_H, SP = 2, SR2 = 35_H

BI = AF_H

Formulated Address (FA) = $R2_{3-0}$, RJ (0, BI_{3-0}, M)

= 0001, RJ (0, 1111, 0100)

= 00010001 = 11_H

SR2= 11 + 1 = 12_H

Example 2

C = 1, M = 9, R2 = $F1_H$

R3 = 51_H, SP=2, SR2 = $1A_H$

BI = $C1_H$

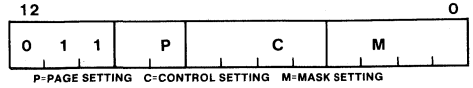
FA= BI_{7-4} VM, $R3_{3-0}$

= 1100 V 1001, 0001 = 11010001 = $D1_H$

SR2 = D1 + 1 = $D2_H$

Opcode 3 - Translate

Format



Field	Information	
C - Control Setting	Address - High Nibble Formulation	Address - Low Nibble Formulation
0000	$SR(SP)_{7-4}$	$RJ(SR(SP)_{3-0}, D_{3-0}, Mask)$*
0001	$SR(SP)_{7-4}$	$RJ(SR(SP)_{3-0}, D_{7-4}, Mask)$
0010	$SR(SP)_{7-4}$	$RJ(SR(SP)_{3-0}, D_{11-8}, Mask)$
0011	$SR(SP_{7-4}$	$RJ(SR(SP)_{3-0}, CCR_{3-0}, Mask)$
0100	$SR(SP)_{7-4}$ V Mask+	$RJ(SR(SP)_{3-0}, D_{3-0}, R4_{3-0})$
0101	$SR(SP)_{7-4}$ V Mask	$RJ(SR(SP)_{3-0}, D_{7-4}, R4_{3-0})$
0110	$SR(SP)_{7-4}$ V Mask	$RJ(SR(SP)_{3-0}, D_{11-8}, R4_{3-0})$
0111	$SR(SP)_{7-4}$ V Mask	$RJ(SR(SP)_{3-0}, CCR_{3-0}, R4_{3-0})$
1000	$SR(SP)_{7-4}$ V 0001	$RJ(SR(SP)_{3-0}, D_{3-0}, Mask)$
1001	$SR(SP)_{7-4}$ V 0001	$RJ(SR(SP)_{3-0}, D_{7-4}, Mask)$
1010	$SR(SP)_{7-4}$ V 0001	$RJ(SR(SP)_{3-0}, D_{11-8}, Mask)$
1011	$SR(SP)_{7-4}$ V 0001	$RJ(SR(SP)_{3-0}, CCR_{3-0}, Mask)$
1100	$SR(SP)_{7-4}$ V $R4_{7-4}$	$RJ(SR(SP)_{3-0}, D_{3-0}, Mask)$
1101	$SR(SP)_{7-4}$ V $R4_{7-4}$	$RJ(SR(SP)_{3-0}, D_{7-4}, Mask)$
1110	$SR(SP)_{7-4}$ V $R4_{7-4}$	$RJ(SR(SP)_{3-0}, D_{11-8}, Mask)$
1111	$SR(SP)_{7-4}$, V $R4_{7-4}$	$RJ(SR(SP)_{3-0}, CCR_{3-0}, Mask)$

+ - V = OR

* - RJ = Right Justify function (See Appendix Table A-4)

Operation

MA_{9-0} ← P: Formulated Address (see text);
If Control = 0,1,2,3,8,9,A,B, then $SR(SP) \leftarrow MA_{7-0} + 1$;

Description

The control and mask fields are used to formulate a new 8-bit address, as described below. This address is concatenated to the page setting to yield the new Memory Address Output. If the control setting is in the ranges 0-3 or 8-B, the formulated address is incremented and placed in the currently active stack register. No stack register update is performed for control settings of 4-7 or C-F.

The new address is formulated from the current program counter (value in the currently active stack register), values present at the Discrete Interface, and/or the content of the Condition Code Register. Certain control settings also specify use of the operational register R4 (the masking register) during address formulation. Mask values applied to low nibble derivation are used as bit maps in the Right Justify function. Sixteen address formulations are possible.

Example 1

C = 2, M = 7, R4 = 56_H

CCR = 3, SP = 1, SR1 = 19_H

D = $2A2_H$

FA = $SR(SP)_{7-4}$, $RJ(SR(SP)_{3-0}, D_{11-8}, M)$

= 0001, RJ(1001, 0010, 0111)

= 0001 1010 = $1A_H$

SR1 = 1A + 1 = $1B_H$

Example 2

C = 7, M = A_H, R4 = 12_H

CCR = 2, SP=1, SR1 = 25_H

D = 3 $1B_H$

FA = $SR(SP)_{7-4}VM$, $RJ(SR(SP)_{3-0}, CCR_{3-0}, R4_{3-0})$

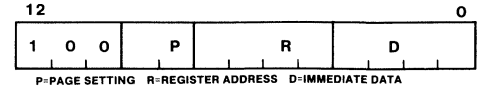
= 0010 V 1010, RJ(0101, 0010, 0010)

= 1010 0101 = $A5_H$

SR1 = 25_H

Opcode 4 - Load

Format



Field	Information
R - Register Selection	Register Selected
0000	$R0_{3-0}$
0001	$R0_{7-4}$
0010	$R1_{3-0}$
0011	$R1_{7-4}$
0100	$R2_{3-0}$
0101	$R2_{7-4}$
0110	$R3_{3-0}$
0111	$R3_{7-4}$
1000	$R4_{3-0}$
1001	$R4_{7-4}$
1010	D_{11-0} XOR Mask Register
1011	CCR_{3-0}
1100	Outer Counter Holding $Register_{3-0}$
1101	Outer Counter Holding $Register_{7-4}$
1110	Inner Counter Holding $Register_{3-0}$
1111	Inner Counter Holding $Register_{7-4}$

Operation

Selected Register ← Immediate Data (see text);

MA_{9-0} ← P: SR(SP);

SR(SP) ← SR(SP) + 1;

Description

The value in the Immediate Data field is placed into the register addressed by the R field. The value contained in the currently active stack register is first concatenated to the page selection to yield the Memory Address Output and then incremented.

Each 8-bit register occupies two addresses. The high nibble and low nibble of these registers must be loaded separately and may be accessed in any order.

Note: The Load opcode is functional regardless of the state of the Reset input.

Example

R = 0111, D = 1010, SR2 = 2F, SP = 2

P = 1

Then:

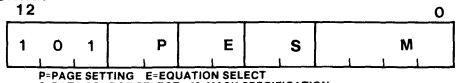
MA_{9-0} ← 0100101111

SR(2) = 30_H

1010 → $R3_{7-4}$

Opcode 5 - Conditional Discrete Set-Up

Format



Field — **Information**

E - Equation Select	Equation	Result: No Bits Selected	Result: One Bit Selected
00	OR	False	Bit Value
01	AND	True	Bit Value
10	XOR	False	Bit Value
11	XNOR	True	Not (Bit Value)

S - Data Source Select	Data Source
00	D_{3-0}
01	D_{7-4}
10	D_{11-8}
11	CCR_{3-0}

M - Mask Value	Mask Recorded
= 0000	Current pattern in CCR
≠ 0000	Mask value

Operation

E,S, and M fields recorded for subsequent use;
Conditional Discrete Active flag set:
$MA_{9-0} \leftarrow P: SR(SP)$;
$SR(SP) \leftarrow SR(SP) + 1$;

Description

The equation-select, data-source select, and mask specification are recorded as the new Conditional Discrete evaluation parameters, and the Conditional Discrete Active flag is set. The value in the currently active stack register is first concatenated to the page setting to yield the new Memory Address Output, then incremented.

The data-source select specifies either one of the three four-bit groups at the Discrete Interface (D_{11-8}, D_{7-4}, or D_{3-0}) or the Condition Code Register, CCR, as a source. The mask specifies either an immediate value or the pattern in the Condition Code Register as a bit selection map for entering source bits into the evaluation. If the CCR pattern is specified, it is recorded during Opcode 5 execution and may be changed on subsequent cycles without changing the Conditional Discrete evaluation equation. A mask value of all zeroes selects the CCR as the mask source. Finally, the equation select specifies what operation is to be performed between the selected bits:OR, AND, XOR, or XNOR.

The equation-selection options, data-select options, and mask specifications are listed. Also listed is the result of the binary functions (AND, OR, XOR, and XNOR) when the mask setting selects no bits or a single bit.

Once set up, the formula is evaluated on the current and subsequent microcycles (except as noted below), and the result is recorded and made available for testing on the next cycle(s). Testing is accomplished through Opcode 7, the Subop and Branch command. Testing causes the Conditional Discrete Active flag to be reset (unless the same address is branched to), thus disarming the capability until another invocation of Opcode 5.

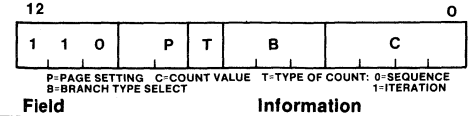
The conditional equation is not evaluated during the execution of Opcode 3, when the Discrete Interface is being used in address translation. Nor is it evaluated on the same cycle it is being tested on (during the execution of the Subop and Branch command) except when Subop F is specified (see documentation for Opcode 7).

If the CCR is the data source and the CCR is changed through the Load command (Opcode 4), the new CCR will be used in the evaluation on that cycle.

The Conditional Discrete formula may be changed at any time.

Opcode 6 - Immediate Count Commands

Format



Field — **Information**

B - Branch Select	Branch for Type = 0 (Sequence)	Branch for Type = 1 (Iterate)
000	R1 Branch	R1 Branch
001	Next Address	Next Address
010	Map	Same Address
011	Return	Return
100	R1 Branch and Link	R1 Branch
101	R0 Branch	R0 Branch
110	Link	Return
111	Return and Link	Return and Link

Description

The Immediate Count command causes the count value to be placed into the holding and working registers for one of the two counters, and a count of the type specified to be initiated. The specified branch type is also recorded. The effects on the stack pointer and/or currently active stack register vary with branch type and count type and are discussed separately below.

The two counters are designated "inner" and "outer." If no counters are active, the outer counter is started. If the outer counter alone is active, it is suspended (put into hold), and the inner counter is activated. If both are active, an "error" condition exists. In such a case, both counters are deactivated and the branch condition associated with the outer counter is taken. An error condition also occurs if an attempt is made to initiate a count on the same cycle during which one of the counters expires. Error processing in this case is identical to that described above.

The count value is zero-relative. That is, a count value of zero specifies one count, a value of one specifies two counts, etc.

The active counter is decremented on subsequent microcycles until the count is satisfied, at which time the action described below is taken. When the inner counter expires, the outer one is reactivated and continues counting on the next microcycle.

On a sequential count, normal program flow continues while microcycles are counted. When the count finally expires, the branch specified in the controlling Immediate Count command is taken. Any branch specified in the command being executed at the time is ignored; however, the page setting in the control word being executed is used in formulating the new Memory Address Output.

When an iteration count is specified, the branch is taken immediately. The memory address formulated by concatenating the address specified by the branch select to the page setting is then repeated for the number of microcycles specified by the count value. When the

count expires, execution continues with the next instruction in sequence following the one that was iterated upon.

The various combinations of counter modes are shown in Table I. The inner counter can be used only when the outer counter is in the sequential count mode. Other combinations are not achievable because they will cause an error condition through the mechanisms stated above.

Table I - Counter-Mode Combinations

		Inner		
		Inactive	Active (Sequence)	Active (Iterate)
Outer	Sequence	Yes	Yes	Yes
	Iterate	Yes	Not achievable	Not achievable

Example

Assume that control word MF_{12-0} = 1100011010011

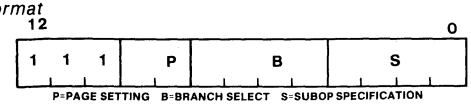
and R0 = 48_H, SP = 2

Then an immediate branch is done via register R0 to microword address 0001001000. The program iterates on this instruction four times (count = C + 1) and continues with the next instruction in sequence:

SR(2) = 49_H, on page 0.

Opcode 7 - Subop and Branch Command

Format



Field	Information	
B - Branch Select Option 2	Conditional Discrete Active Flag Reset or Conditional Discrete Evaluates to "True"	Conditional Discrete Active and Evaluates to "False"
0000	R1 Branch	Next Address
0001	Next Address	Same Address
0010	Map	Next Address
0011	Return	Next Address
0100	R1 Branch and Link	Next Address
0101	R0 Branch	Next Address
0110	Link	Next Address
0111	Return and Link	Next Address
1000	R1 Branch	R0 Branch
1001	Next Address	Return and Link
1010	Same Address	Next Address
1011	Return	R1 Branch and Link
1100	R1 Branch	Same Address
1101	R0 Branch	Return and Link
1110	Return	Same Address
1111	Return and Link	Map

Field	Information
S - Subop Specification	Action
0000	CCR_{3-0} ← D11: D10: D1: D0
0001	CCR_{3-0} ← D11: D10: D1: (D1 XOR DO)
0010	CCR_{3-0} ← D11: D10: ((D1 XOR DO) OR CCR_2): D0
0011	CCR_{3-0} ← D_{7-4}
0100	D_{7-4} ← CCR_{3-0}
0101	D_2 ← D1 XNOR D0
0110	D1: D0 ← D3: D2
0111	D3 ← D0
1000	Reload Sequential Count
1001	Enable Sequential Count
1010	No-operation
1011	R3 ← BI_{7-0}
1100	Stop All Counters
1101	Enable Iteration Count
1110	Stop Current Count
1111	Evaluate Conditional Discrete Equation

The sequence counter branch options specified by Opcode 7 are shown below.

Field	Information
B - Branch Option 1	Specified Branch (Refer to Appendix Table A-2)
0000	R1 Branch
0001	Next Address
0010	Map
0011	Return
0100	R1 Branch and Link
0101	R0 Branch
0110	Link
0111	Return and Link
1000	R1 Branch
1001	Next Address
1010	Same Address
1011	Return
1100	R1 Branch
1101	R0 Branch
1110	Return
1111	Return and Link

Description

The Subop and Branch command combines two semi-independent operations within one command. The suboperation, or subop, described below specifies a utility function within the EMC (e.g., Discrete Interface operation or counter operation). The branch operation is the means by which the Conditional Discrete equation is sampled. The suboperations are described below:

Suboperations 0 through 7 provide a variety of ways to load the Condition Code Register from the Discrete Interface and drive the Discrete Interface from either the Condition Code Register or from itself. All bits in the group D_{3-0} not explicitly set remain unaltered.

Subop 8 causes the currently active counter to be restarted by reloading its working register from its holding register. The branch option associated with the counter is also redefined to that specified by the attendant branch field. Shown are the branch options that can be specified through the use of this subop (Branch Option 1). If no counter is active, none is started by the action of this subop.

Subop 9 causes a sequential count to be initiated. The rules determining counter nesting, etc., during the execution of Opcode 6 (Immediate Count) apply with the exception that the initial value placed in the newly started counter's working register is taken from its associated holding register. The branch option recorded has the functionality shown under Branch Option 1.

Subop D causes an iteration count to be initiated. As with Subop 9, rules governing counter nesting follow those set down for Opcode 6 (Count Immediate), and the newly initiated counter's working register is initialized with the value in its associated holding register. Consistent with Opcode 6 functionality, the branch is taken immediately. The branch taken is subject to the same criteria as all other Opcode 7 branches (Conditional Discrete influences) and is described in greater detail below. Consistent with counter operation via Opcode 6, the execution of Subops 8, 9, and D on the same cycle as when an active counter expires is an error condition that causes all counters to be stopped and the branch option associated with the outer counter to be taken.

Subops C and E stop all counts and the currently active counter, respectively. Neither of the branch conditions specified when the counter(s) were initiated is taken; rather, execution continues in sequence from the current instruction. Execution of either subop on the same cycle as when an active counter expires does not inhibit normal counter operation; that is, the branch associated with the counter is taken. Execution of Subop E on the same cycle as when the inner counter expires does not cause the outer counter to be stopped.

Subop B causes the data present at the Bus Interface to be latched into R3 (Operational Register 3).

Subop F directs the EMC to evaluate the Conditional Discrete equation (if active) on the current microcycle prior to the resolution of the branch portion of Opcode 7. (The conditional discrete equation is not evaluated for all other Opcode 7 suboperations due to potential data-path conflicts related to the Discrete Interface.)

Finally, **Subop A** provides a no-operation, or no-op, code.

The branch option specifies one of sixteen possibilities, or one of thirty-two when coupled with the Conditional Discrete evaluation feature. Branch Option 2, above, shows the 32 possibilities; their operations are explained in Appendix Table A-2.

When no Conditional Discrete is pending, the branch is resolved by substituting a "true" evaluation. Otherwise, the previously latched sample value (or current sample value if Subop F is specified) is used to resolve the branch. The various true/false pairs allow a number of conditional branches/returns and/or two-way branches. The branch is overridden when Suboperations 8 or 9 are used (reload active counter, initiate sequence counter, respectively). In these two exceptions, the branch pattern is recorded for later use (upon counter expiration) and execution continues with the next address.

The execution of Opcode 7 has the effect of resetting the Conditional Discrete Active flag in all cases except when the branch resolves to the "same address," in which case the state of the Conditional Discrete Active flag is not altered. This feature allows the EMC to dwell on a particular microinstruction until a certain condition is met.

Note that the value of the Conditional Discrete sample (if active) enters into the branch resolution for Subop D (enable iteration count), but not Subops 8, 9 (reload count, initiate sequence count). However, the Condition Discrete Active flag is reset by all three of these suboperations.

Example 1

Assume that control word MF_{12-0} = 1110111001111 and SP = 1, R1 = 11_H, SR1 = 62_H

Subop F specifies: Evaluate Conditional Discrete equation; Branch Option C specifies a branch via R1 if the Conditional Discrete evaluates to true, or same address if it evaluates to false. Subop F directs the EMC to evaluate the Conditional Discrete equation (if active) on the current microcycle prior to the resolution of the branch portion of Opcode 7. It is assumed that an earlier set-up of the Conditional Discrete set the Conditional Discrete Active flag.

If Conditional Discrete equation is true: $MA_{9-0} \leftarrow$ 0100010001

$SR(1) \leftarrow 12_H$

If Conditional Discrete equation is false: $MA_{9-0} \leftarrow$ same address

This operation is useful if the program must dwell until a condition is met. Testing of the Conditional Discrete equation resets the Conditional Discrete Active flag, unless the branch is to the same address.

Example 2

Assume that control word MF_{12-0} = 1110010001001 and SP = 2, R1 = 21_H, SR2 = 45_H

Subop 9 specifies: Enable sequential count. Presumably, a sequential count was loaded earlier. Normal program flow continues for the number of cycles specified in the count. When the count expires, a branch is made via R1.

$MA_{7-0} = 21_H$

$SR(2) = 22_H$

PROGRAMMING EXAMPLES

The following examples of microcode listings show how the instructions explained above are applied in typical and useful situations. The instructions used are defined by macros, as described below. The 8-bit control/data field in the control word of the opcodes provides for a large number of variants for most of the eight basic opcodes. This encoding of the opcodes is most easily handled in macro-assembly language. (A reading of the concluding section of this Note, Notes on the Use of Registers and Instructions, should add to the value of these examples.)

Macro Definitions

The following Macros are used in the examples in this section. The field definitions have the relationships shown to EMC pins:

OPCODE = MF12-MF10
ADDIN = MF9-MF0
PAGE = MF9-MF8
CONTROL = MF7-MF4
MASK = MF3-MF0
SUBOP = MF3-MF0
MF7 = MF7
OP6BR = MF6-MF4

The construct "#(number)" indicates substitution of actual parameters. These parameters are positional. Thus, #(0) denotes the first parameter, #(1) the second, and #(2) the third.

Unconditional Branch

```
Define Macro BR;
    OPCODE=0,ADDIN=#(0);
ENDMACRO;
```

Unconditional Branch and Link

```
Define Macro BAL;
    OPCODE=1,ADDIN=#0;
ENDMACRO;
```

Map Instruction (Opcode 2)

```
Define Macro MAP;
    OPCODE=2, PAGE=#(0), CONTROL=#(1), MASK=#(2);
ENDMACRO;
```

Translate Instruction (Opcode 3)

```
Define Macro XLT;
    OPCODE=3, PAGE=#(0), CONTROL=#(1), MASK=#(2);
ENDMACRO;
```

Load Instruction (Opcode 4)

```
Define Macro LD;
    OPCODE=4, PAGE=#(0), CONTROL=#(1), MASK=#(2);
ENDMACRO;
```

Conditional Discrete Set-Up Instruction (Opcode 5)

```
Define Macro CD;
    OPCODE=5, PAGE=#(0), CONTROL=#(1), MASK=#(2);
ENDMACRO;
```

Count (Opcode 6)

```
Define Macro CNT;
    OPCODE=6, PAGE=#(0), OP6BR=#(1), MASK=#(2),
      MF=0;
ENDMACRO;
```

Iterate (Opcode 6)

```
Define Macro ITR;
    OPCODE=6, PAGE=#(0), OP6BR=#(1), MASK=#(2),
      MF7=1;
ENDMACRO;
```

Subop and Branch Instruction (Opcode 7)

```
Define Macro SUB;
    OPCODE=7, PAGE#(0), CONTROL=#(1), SUBOP=#(2);
ENDMACRO;
```

Next Address Macro (Opcode 3)

This control-word pattern generates the next microcode address and is commonly used as an EMC no-op.

```
Define Macro NEXTADD;
PAGE=#(0), OPCODE=3, CONTROL=0, MASK=0;
ENDMACRO;
```

Example 1

Demonstrates

Initialization of the EMC.

Opcodes Used

0 - BR
4 - LD
7 - SUB

Description

The Reset control (Reset) sets the MA0 and the stack pointer, but not the stack register, to zero. The first location must, therefore, initialize the PC. An unconditional branch sets the PC to 0001. Next, some of the operational registers are initialized. The chosen data are arbitrary. In location 1, zeros are loaded into the true/complement mask for discrete interface bits D11-D8. A zero bit within the register signifies that the corresponding bit passes directly to the rest of the EMC logic (without inversion). The power-up value of the CCR is arbitrarily binary 1000. Operational register 0 is a branching register. It is used here to hold the address of the microinstruction fetch routine.

Microcode sequences that define macroinstructions generally terminate with a Subop and Branch instruction that loads the CCR and branches via R0 to the macroinstruction fetch routine. R0 is loaded in instructions 3 and 4. The second parameter in the Load instruction designates a register select in the opcode format.

The next four instructions initialize the mapping register, R2, and the masking register, R4, with some arbitrary values. In an actual design, these values could depend on machine/macroinstruction architecture, etc.

At location 9, the first macroinstruction is fetched through an R0 branch. Subop A is a no-op.

Microcode Fields

Address	EMC GP501	Comments
	ORG (0000)	
0000	BR (0001)	Initialize SR(0); 0+1 → SR(0)
0001	LD (0, A, 0)	0 → D_{11-8} T/C mask
0002	LD (0, B, 8)	8 → CCR
0003	LD (0, 0, LOW(IFETCH))	Low → R0
0004	LD (0, 1, HIGH(IFETCH))	High → R0 R0 now has address of IFETCH
0005	LD (0, 4, 6)	6 → R2 low
0006	LD (0, 5, 7)	7 → R2 high Map register now contains 76
0007	LD (0, 8, 7)	7 → R4 low
0008	LD (0, 9, E)	E → R4 high Mask register now contains E7
0009	SUB (0, 5, A)	branch via R0 to fetch a macroinstruction

Example 2

Demonstrates

Mapping directly from BUS inputs.

Opcodes Used

0 - BR
2 - MAP
3 - XLT
7 - SUB

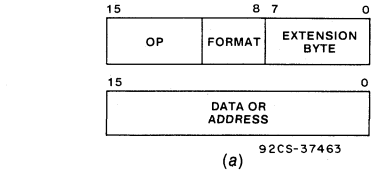
Description

A hypothetical machine is assumed with a macroinstruction modeled after the AN/YUK-20. As shown in Fig. 3, the macroinstruction comprises a 6-bit opcode and a 2-bit format field, and is followed by an extension byte, which may contain general register specifications, etc. Additional bytes, supplying address or immediate data, may follow.

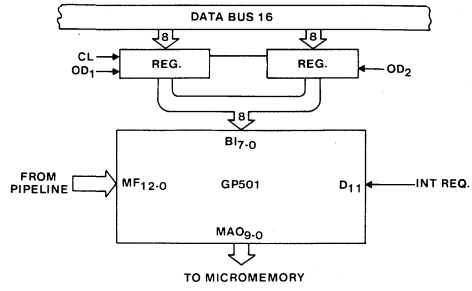
The Opcode/Format byte is available at the Bus Interface. Discrete Interface bit 11 is assigned for the interrupt request input. Assume that the request is qualified with the interrupt-enable status, and that the true/complement mask for this bit is set, so that this status is "low true" to the EMC. This masked interrupt request is sampled at the beginning of the fetch sequence.

In this example, the Translate instruction at 001F tests for an interrupt request. With control = 2 and mask = 8, the new formulated address takes the form:

MA_{7-0} = $SR(SP)_{7-4}$, $RJ(SR(SP)_{3-0}, D_{11-8}$, Mask)



(a)



(b)

Fig. 3 - Macroinstruction format (a) and mapping configuration (b).

Since SR(SP) = 20 before execution:

MA_{7-0} becomes 2, RJ(0, D_{11}, 1000)

that is,

MA_{7-0} = 20 if interrupt is pending
= 21 if no interrupt is pending

In other words, the control/mask combination selects D11 as the LSB of MA, and the program branches to microcode address 0020 if there is a pending interrupt, or to 0021 if there is not.

The branch option at address 0021 is Branch and Link via R1, and A is a no-op suboperation. The net result is the fetch of a byte by invoking a subroutine whose address is in R1.

At address 0022, the byte is now at the Bus interface, and Subop B specifies that the Bus Interface is latched into R3. At this point, the first byte is in R3 and the second one is at the Bus Interface. Secondary instruction decoding resides on page 1 and is not shown.

The Map instruction at 0023 computes the next microcode address from the 6 Opcode bits in R3.

With the parameters control = 7 and mask = C, the formulated new address is:

FA = $R3_{7-4}$, RJ (0, $R3_{3-0}$, MASK)

and

MA_{9-0} = 01XXXX00XX

where the X's represent the 6 opcode bits; the page is set to 1. R3 high is selected for the upper nibble and R3 low for the lower nibble. Mask specifies the most significant 2 bits of R3 low according to the Right Justify function.

Microcode Fields

Address	EMC GP50I	Comments
	ORG (001F)	
001F	XLT (0,2,8)	Test D_{11} for interrupt request
0020	BR(ISERVICE)	Branch to routine if interrupt is pending, else ...
0021	SUB (0,4,A)	Go to Fetch routine via R1; fetch first byte to bus interface
0022	SUB (0,4,B)	Latch byte → R3; fetch next byte to bus interface
0023	MAP (1,7,C)	New address is 01XXXX00XX, where X's are the opcode
XXXX	ISERVICE:	Interrupt service routine

Example 3

Demonstrates

Interaction of the Conditional Discrete, CD, feature and the Same Address type branch.

Opcodes Used

5 - CD
6 - ITR
7 - SUB

Description

When the Sub command is processed and the next microcode command is the Same Address, the EMC does not reset the CD active state. This circumstance can occur when an iteration count is in progress, or when the Opcode 7 branch taken resolves into the Same Address type.

Suppose an operation is to be performed a fixed number of times, as in a shift, for example, and an action is to be taken after the last iteration if Carry is set. The first instruction sets up a CD evaluation: The content of D3-0 is to be ANDed with the mask 0111 and the result evaluated. The active CD flag is set. (The CD values chosen are arbitrary.) The instruction at 00B1 initializes a count of four. The type of count is iterative, and the specified branch is Next Address, which is taken immediately. At address 00B2, the instruction is repeated four times. A branch is taken on the fourth count via R0 if the CD evaluation is true, otherwise execution continues with the next microcode instruction.

Microcode Fields

Address	EMC GP501	Comments
	ORG (00B0)	
00B0	CD (0,4,7)	Initialize Conditional Discrete setup. Equation and data select arbitrary
00B1	ITR (0,1,3)	Set iteration count = 4. Branch immediate to next address
00B2	SUB (0, 5, F)	Iterate here. On fourth count, if CD evaluation is true, BR via R0, else continue with next instruction

Example 4

Demonstrates

Interaction of the Conditional Discrete, CD, feature and the Same Address type branch.

Opcodes Used

5 - CD
7 - SUB

Description

Assume that the program must wait for some asynchronous event to occur. An example would be if one were waiting for a memory busy condition to end. Two instructions will accomplish this task. The first instruction sets up the CD, similarly to example 3, with arbitrary

values. The suboperation in 00B9 specifies evaluations of the CD. Note that Subop F of Opcode 7 is the only one that evaluates the CD. If the evaluation is true (memory is busy) the branch is to the Same Address. If the evaluation is false (memory is not busy), the branch is to the Next Address.

Microcode Fields

Address	EMC GP501	Comments
	ORG (00B8)	
00B8	CD (0,4,1)	Initialize Conditional Discrete setup. Equation and data select arbitrary
00B9	SUB (0, A, F)	Wait until evaluation is false, then continue with next instruction

Example 5

Demonstrates

Management of Page and Same Address Branch resolution.

Opcodes Used

4 - LD
5 - CD
6 - ITR
7 - SUB

Description

The Page memory address is normally passed through the EMC from the control word input to the Memory Address Output. The first section of code at 0123 generates a Branch and Link via R1 to a subroutine at address 03AA, i.e., page 3. The Return instruction residing on page 3 must specify page 1 for a proper return.

The next part of this example shows how the EMC ignores the page setting in the control word input when the next microcode address is the Same Address. At address 0312 a count of four is set on page 3. The branch specified is Next Address. The program iterates four times at address 0313 and ignores the page setting of 0 until the fourth cycle. Then the page setting is concatenated to the value in R0 to generate the next microcode address, i.e., branch to macroinstruction fetch. The Subop loads CCR from D7-D4.

The last part of this example (0320) first sets up the CD. The Subop specifies evaluate CD. As long as the evaluation is false, the Same Address (on page 3) is generated. When the evaluation is true, a branch is made via R1 to page 2.

Microcode Fields

Address	EMC GP501	Comments
	ORG (0123)	
0123	LD (1,2,A)	Page = 1, A → R1 low
0124	LD (1,3,A)	Page = 1, A → R1 high
0125	SUB (3,4,A)	Page = 3, Branch and Link via R1, Subop = no-op
		Return, on page 3, must specify page = 1
	ORG (0312)	
0312	ITR (3,1,3)	Set count =4. Branch to next address. Page = 3
0313	SUB (0,5,3)	Iterate four times on this address. Then branch via R0 to page 0. D7-D4 → CCR
	ORG (0320)	
0320	CR (3,4,5)	Set up CD. Arbitrary values
0321	SUB (2,C,F)	Evaluate CD. Branch to same address if false. If true, branch via R1 to page 2.

Example 6

Demonstrates

Use of nested counters.

Opcodes Used

1 - BAL
3 - XLT
6 - CNT
6 - ITR

Description

When following the program listing for this example, refer also to Fig. 4, which shows how the contents of the two counters change during execution. The example might be a common exit routine for a group of similar macroinstructions. The macroinstruction fetch routine is assumed to be on page 0, as specified by the content of R0. The outer counter effects a branch to macroinstruction fetch after the last instruction of the common routine has been executed. Within the range of this count, the inner counter is used in both the sequential and iterative modes.

At address 03B0, the outer counter is loaded with a sequential count of four. The instruction specifies that

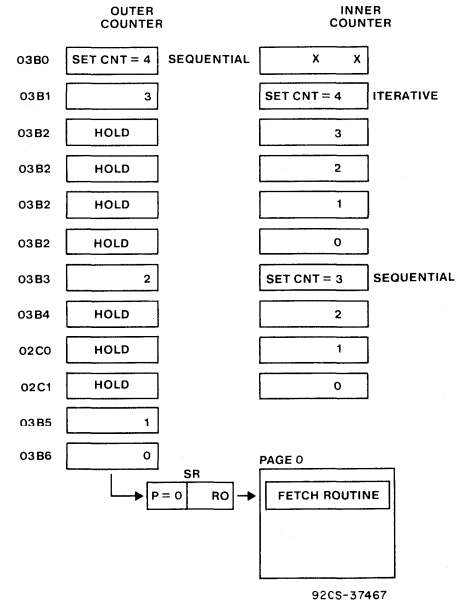


Fig. 4 - Example 6: Contents of counters during execution.

when the count expires, a branch should take place via R0. At 03B1 an iterative count of four is set on the inner counter. This instruction counts 1 on the outer counter. The iterative type count branches immediately, and here Next Address is specified. The instruction in 03B2 is repeated four times, when the inner counter started, the outer one was put on hold. At 03B3 a sequential count of 3 is loaded into the inner counter, and since it expired, the outer counter resumed its count of 1. The last count instruction also specifies a return type branch after the count expires. Next the subroutine is called. The call and the two subroutine words exhaust the inner counter. During this process the outer counter was again on hold. Since the inner counter expires at 02C1, its branch (Return) is coupled with the page selection, and control returns to 03B5. The outer counter is now free to resume counting during the following two instructions, after which the outer counter expires. The page is specified as 0 in 03B6 and concatenated with the content of R0 to yield the next microcode address, i.e., a fetch operation.

Note that the Next Address action of 03B6 is overridden by the counter action.

In general, the branch-after-count nature of the sequential type of count makes it useful in the construction of shared microcode routines. The branch-before-count nature of the iterative-type count makes it useful for repeating in-line instructions.

Microcode Fields

Address	EMC GP501	Comments
	ORG (03B0)	
	COMEX:	
03B0	CNT (3,5,3)	Set sequence count = 4 (outer); branch via R0 after 4 counts
03B1	ITR (3,1,3,)	Set iterate count = 4. BR to Next Address
03B2	NEXTADD(3)	Repeat 4 times
03B3	CNT (3,3,2)	Set sequence count = 3; return branch is specified
03B4	BAL (SUB)	Call subroutine
03B5	NEXT ADD (3)	Return here after subroutine; branch to Next Address
03B6	NEXT ADD (0)	Page 0 with R0 is next address. Outer count of 4 is expired
	ORG (02C0)	
	SUB:	
02C0	NEXT ADD (2)	Go to next address, page 2
02C1	NEXT ADD (3)	Inner counter expires; branch type return is coupled with page = 3

Example 7

Demonstrates

Use of Translate instruction and sequential count.

Opcodes Used

3 - XLT
4 - LD
7 - SUB

Description

This example describes a memory or I/O transfer subroutine. Assume that the processor has an asynchronous bus and that the handshaking signals are available at Discrete Interface bits D11-D8. Then a number of machine cycles can be allotted to complete a transfer before declaring a timeout. This procedure prevents a peripheral or a memory board that does not respond from hanging up the processor.

The address of the bus timeout procedure is assumed to be in R1. A sequence counter is used to count machine cycles. If and when that count expires, a branch via R1 is made to the timeout handler.

The first instruction (006C) simply loads 0's into the high nibble of R4. R4 is ORed with the high address nibble in the Translate instruction used later. The outer timer (in 006D and 006E) is loaded with the count 40H. (The actual count will be 41H or 65 decimal).

The instruction in 006F enables a sequential count and specifies an R1 branch. By normal action of this instruction, the stack register is updated and the address 0070 generated. The translate commands from 0070-007F inhibit updating of the stack register; the least significant nibble of the generated Next Address is derived from the Discrete Interface bits D11-D8.

XLT (0, E, F) specifies a formulated address:

$$FA = SR(SP)_{7-4} \vee R4_{7-4}, RJ(SR(SP)_{3-0}, D_{11-8}, 1111)$$
$$= SR(SP)_{7-4}, D_{11-8}, \text{since } R4 = 0$$

The overall result is that the instructions will reference each other within the block without updating the active stack register. Control remains within the block until either the counter expires or the "cycle complete" state is generated. This state is here arbitrarily set to 1000.

This example shows a state machine for which the "next state" is computed from the values of the bus handshake lines read at the Discrete Interface.

The instruction in 0078 specifies a Return from the subroutine and stop the counter.

Microcode Fields

Address	EMC GP501	Comments
	BAL (BUS TRAN)	Call transfer routine
	ORG (006C)	
	BUSTRAN:	
006C	LD (0,9,0)	0 → R4 high
006D	LD (0,D,4)	4 → Counter H. Register high
006E	LD (0,C,0)	0 → Counter H. Register low Count = 40H
006F	SUB (0,0,9)	Enable sequential count R1 = branch register
0070	XLT (0,E,F)	State 0000
0071	XLT (0,E,F)	0001
0072	XLT (0,E,F)	0010
0073	XLT (0,E,F)	0011
0074	XLT (0,E,F)	0100
0075	XLT (0,E,F)	0101
0076	XLT (0,E,F)	0110
0077	XLT (0,E,F)	0111
0078	SUB (0,3,E)	1000 - Return and
0079	XLT (0,E,F)	1001 stop counter
007A	XLT (0,E,F)	1010
007B	XLT (0,E,F)	1011
007C	XLT (0,E,F)	1100
007D	XLT (0,E,F)	1101
007E	XLT (0,E,F)	1110
007F	XLT (0,E,F)	1111

NOTES ON USE OF REGISTERS AND INSTRUCTIONS

This section reviews some of the application information used in the examples and also highlights some additional material relevant to practical application of the EMC. Again, it is impossible to cover all situations in this Application Note, and the reader is again referred to the user's guide for the EMC for details and the more complex aspects of the device.[3]

Reset

While the Reset input control forces MA_{9-0} to zeroes and sets the stack pointer to zero, it does not initialize SR0. The first instruction in micromemory must therefore be an unconditional branch so that stack register 0 is initialized. Note that while the Reset is active, the Control Word command is inhibited with the exception of the Load command. It is possible to load all addressable internal registers with the Reset input active, i.e., to complete initialization of the EMC while a device reset condition exists.

Load

The Load command is the means by which the EMC's operational registers are set. Among the addressable registers, only R3, the CCR, and the counter holding registers are altered by the action of other commands. Generally, the registers will be set once during initialization. After that, the Load command is most frequently used in loading counter holding registers, the CCR, and managing the controls of the branching registers R0 and R1.

BR and BAL

The BR and BAL commands provide direct control over microcode address generation. They are the only instructions for which Control Word data is passed directly to the address output.

The Branch and Link (BAL) command is the simplest means of invoking subroutines, and is typically used to execute commonly used pieces of microcode.

Map

The Map command provides the ability to generate branch addresses according to values present at or recorded from the Bus port. Examples are macroinstruction data, data from the data bus, and interrupt-vector data. Hence, mapping ROMs and vector ROMs are not required in the EMC system. Typical use of the Map command is in the generation of microcode entry points for macrocode instruction execution and interrupt service.

The ability to latch Bus data in R3 allows the same piece of data to be referenced many times. The Map command can be used for vectoring, but not for relative branching.

Translate

The Translate command is similar to the Map command in that program flow is modified according to values generated external to the EMC. However, in contrast to the Map command, the stack-register value is used in the address formulation. Thus, relative branches are possible based upon values present at the Discrete Interface.

The Translate command is frequently used, especially in implementing such routines as divide or normalization, where current machine status (carry, zero, etc) determines the next action. Processor flags and other status indicators are normally interfaced to the Discrete pins.

There are two broad groups of Translate commands. The first type updates the currently active stack register and effects a one-time n-way relative branch. The other type does not update the stack register, and is useful in tight iterative routines, when one of N functions is executed until some event occurs. One of the Translate commands degenerates into a no-op instruction with the next microcode address. This control word is defined in some of the examples as NEXTAD.

Conditional Discrete Set-Up

Opcode 7, Subop and Branch, provides for a number of branch options. Opcode 5, Conditional Discrete Set-Up, is the means by which the conditional branches are armed.

Counters

The EMC provides two counters: outer and inner. In the unnested mode, the outer counter is used. If, during the range of sequential count, another count is invoked, the outer counter is held and the inner counter is started. This is the nested mode. When the inner counter expires, the outer count is resumed. The outer/inner counter combinations are:

sequence/none
iteration/none
sequence/sequence
sequence/iteration

The branch-after-count nature of the sequential type of count makes it useful in construction of shared-microcode routines. The branch-before-count nature of the iteration type makes it useful for repeating in-line instructions.

Immediate Count

The simplest way to use the two counters, inner and outer, is through the Immediate Count command. But with this command, count is limited to 16. Sometimes Opcode 7 cannot be used for branching because of an armed Conditional Discrete evaluation. However, by using the Immediate Count command, sequence control can be generated without using Opcode 7 or affecting the state of the Conditional Discrete Active flag.

Subop and Branch

Opcode 7 (Subop and Branch) specifies two generally independent operations within the EMC: a branch and a data/utility function.

When the Conditional Discrete feature is not armed, this command can be used to generate any of the various branches listed under the branch options for Opcode 7. A return from subroutine, for example, is conveniently generated in this mode.

Registers

The counter holding registers, CCR and R3, are dynamic in nature. Their contents will change during the course of microcode execution. In contrast, the remaining addressable registers within the EMC are static in nature; their contents do not normally change. The branching registers R0 and R1 contain addresses of commonly used routines; the Discrete Interface XOR mask contains a pattern appropriate for the data generated at D_{11-8}; the mapping register, R_2, contains a pattern determined by the macroinstruction set to be decoded; etc. Most of the addressable registers are altered infrequently, if at all, after initialization.

The user should adopt a convention for the use of the branching registers R0 and R1. Both of these register can be used for an indirect branch, but only R1 can be the source for an indirect branch and link.

For further details concerning the use of registers and instructions, especially Opcode 7, refer to the EMC user's guide.[3]

REFERENCES AND BIBLIOGRAPHY

1. "CMOS 8-Bit General Processor Unit (GPU)," GP001ADL, RCA Solid State Data Sheet, File No. 1324.
2. "An Introduction to the Use of the General Processor Unit, GP001," K. Karstad, RCA Solid State Application Note, ICAN-7202.
3. "Emulating Controller (GP501ADL) User's Guide," RCA Solid State Publication, ECG-750.
4. "The GP501—A Flexible and Powerful Microprogram Controller for Emulation in the Control Section of High-Performance Microcomputers," K. Karstad, RCA Solid State Application Note, ICAN-7281.
5. "A Comparison of EPIC CMOS/SOS Microprogram Controllers GP501 and GP502," K. Karstad, RCA Solid State Application Note, ICAN-7283.

APPENDIX

TABLE A-1 - EMC Registers and Latches

	Register Designation	No. of Bits	Explicit Program Control	Function	Comments
RO	Branch	8	Yes	Next Microprogram address source	Set from Opcode 4 - Load
R1	Branch	8	Yes	Next Microprogram address source	Set from Opcode 4 - Load
R2	Mapping	2 x 4	Yes	Either source of high nibble for address output	H or L nibble set by Opcode 4
R3	Maskable addr.	8	Yes	Use with OPC2-Map	Set from Opcode 4 - Load or Bus. Interface
R4	Masking	2 x 4	Yes	Use with OPC3-Trans	H or L nibble set by Opcode 4
	CCR	4	Yes	Machine condition code register	Set from Opcode 4 or Discrete Interface. Can output to Discrete Interface.
	True/Compl.	4	Yes	Pass or invert Bits D11-D8	Set from Opcode 4 - Load
	Working	8	No	Outer counter	Set from Opcode 4 or altered through Opcode 6 - Immediate count
	Holding	8	Yes	Outer counter	
	Working	8	No	Inner counter	Set from Opcode 4 or altered through Opcode 6 - Immediate count
	Holding	8	Yes	Inner counter	
SR	Stack	4 x 8	No	Currently active is microprogram counter	Three levels of subroutines
SP	Stack Pointer	2	No	Addresses register stack	Wraps around, no full/empty status. User action: reset, pop/push
	CD Control/Mask	8	No	Records set-up values	For subsequent use
	CD Active Flag	1	No	Set by Opcode 5	Reset through Opcode 7 when tested
	CD Sample Latch	1	No	Store result of evaluated formula	
	Active Flag Counter	2	No		
	Branch Select Counter	2 x 4	No	Reload branch option	

TABLE A-2 - EMC SEQUENCE CONTROLS

Branch Options	μMem Address (MA_{9-0})	Stack Register (SR(SP))	Stack Pointer (SP)	Comments
Same Address	MA_{9-0}	NC	NC	
Next Address	P:SR(SP)	SR(SP+1)	NC	
RO Branch	P:RO	RO+1	NC	NC in RO
R1 Branch	P:R1	R1+1	NC	NC in R1
Link	P:SR(SP)	MA_{7-0} +1	SP+1	*
R1 Branch and Link	P:R1	R1+1	SP+1	NC in R1. *
Return	P:SR(SP)	SR(SP)+1	SP-1	*
Return and Link	P:SR(SP)	MA_{7-0}+1	SP-1 SP+1	*
Map	P:SR(SP)$_{7-1}$: D1 ¥D0			NC in SR & SP Discrete Interface Bits

NC - No change
P - Page setting
R0, R1 - Operational registers
*Stack pointer can wrap around
¥Exclusive OR

TABLE A-3 - SUMMARY OF INSTRUCTIONS

COMMAND	CONTROL WORD MF_{12-0}				RESULT				
	12 10	9 8	7 0						
	OP CODE	PAGE	ADDRESS, MASK, CONTROL, REG, SUBOP, etc.		MEMORY OUT (MA_{9-0})	STACK REG. (SR)	STACK PTR. (SP)	SELECTED REG.	FLAG
Uncond. Branch	000	P	Addr		P: Addr	MA_{7-0} + 1	N.C.		
Uncond. Branch & Link[a]	001	P	Addr		P: Addr	MA_{7-0} + 1	SP + 1		
Map[b]	010	P	Control	Mask	P: Formulated Addr	MA_{7-0} + 1	N.C.		
Translate[c]	011	P	Control	Mask	P: Formulated Addr	MA_{7-0} + 1	N.C.		
Load[d]	100	P	Reg.	Data	P: SR	SR + 1	N.C.	Data	
Cond. Discrete Set Up[e]	101	P	E S	Mask	P: SR	SR + 1	N.C.		C.D. Set
Immed. Count[f]	110	P	T Branch	Count	Branch option selected by branch Field	Depends on branch	Depends on branch		
Sub-op and Branch[g]	111	P	Branch	Subop	Branch option selected by branch Field	Depends on branch	Depends on branch		C. D. Reset

COMMENTS

[a] Currently active.
SR is not changed.

[b] FORM. Address from same combination, selected by control value of Bus In, Reg RA, Reg R3 and Immediate mask M.

[c] FORM. Address from same combination, selected by control value of current SR, value at Discrete Interface, Reg R4, CCR and Immediate mask M. No SR update if C = 4-7 and C-F

[d] Active also during reset.

[e] Equation select (E), Data Source Select (S) and Mask are recorded. Data source is Discrete Interface or CCR. testing via Opcode 7.

[f] T = 0, sequence; T = 1, iterate

[g] Subop specifies one of several Discrete Interface operations or counter operations. Subop F tests Condition Discrete set up.

TABLE A-4 - RIGHT JUSTIFY FUNCTION

RJ (Backfill, Source, Mask)
Backfill = B3:B2:B1:B0 (Binary)
Source = S3:S2:S1:S0 (Binary)

MASK (Binary)	RESULT (Binary)
0000	B3:B2:B1:B0
0001	B3:B2:B1:S0
0010	B3:B2:B1:S1
0011	B3:B2:S1:S0
0100	B3:B2:B1:S2
0101	B3:B2:S2:S0
0110	B3:B2:S2:S1
0111	B3:S2:S1:S0
1000	B3:B2:B1:S3
1001	B3:B2:S3:S0
1010	B3:B2:S3:S1
1011	B3:S3:S1:S0
1100	B3:B2:S3:S2
1101	B3:S3:S2:S0
1110	B3:S3:S2:S1
1111	S3:S2:S1:S0

The GP501 - A Flexible and Powerful Microprogram Controller for Emulation in the Control Section of High-Performance Microcomputers

By K. Karstad

This Note describes the Emulating Microcontroller (EMC), GP501,[1] a powerful microprogram controller for use in the control section of computers. The GP501 is essentially a small microprocessor in its own right with its own instruction set. It offers flexibility and features beyond most other available LSI controllers, such as the popular AM2910 bipolar controller. It is one building block of a family of CMOS/SOS LSI circuits called emulation and programmable ICs (EPIC) that were developed to emulate any computer architecture and instruction set, thus making it possible for users to upgrade older computer hardware and to take advantage of LSI CMOS/SOS features while preserving existing software.

MICROCOMPUTER FUNDAMENTALS

Microcomputers fall generally into two classes: single-chip microprocessor designs and microprogrammable bit-slice machines. Single-chip processors have a predefined and unchangeable word-length architecture, and a fixed instruction set.

The opposite holds true for microprogrammable bit-sliced microprocessors. They can be configured to provide a wide variety of digital system architectures with various word lengths and instruction-set capabilities. For some applications, the bit-sliced microprogrammable approach provides the only practical means of achieving special features and high throughput rates.

Perhaps the most exciting feature of user microprogramming is the ability it provides to emulate other machines. By altering the microroutines or substituting another microprogram memory, the functional complexity of the machine is changed. It behaves in an entirely new way; i.e., it executes a completely different set of macroinstructions, has a different architecture, and can be tailored to specific applications.

The control section of a microcomputer gives the machine its "personality." To what degree emulation is easy or practical will to a large extent depend upon the microcontroller or sequencer in the control section. The two main parts of the control section are the microprogram memory, which holds the microinstructions, and the microprogram sequencer. The main purpose of any sequencer is to present an address to the microprogram memory so that a microinstruction is fetched and executed.

Fig. 1 shows the basic elements of a microprogrammable and bit-slice type architecture. The processing section, where data is manipulated and computed, is made up of a number of identical bit-slices. Each bit-slice represents a functional slice through the ALU and register-file functions of a CPU. The bit-slices may be concatenated to form any desired word length in multiples of the basic unit's bit-length. A macroinstruction is read from main memory and decoded in the controller. The controller

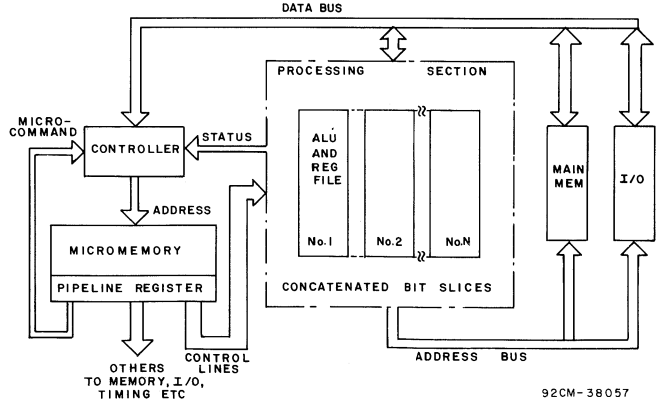


Fig. 1 - Basic elements of a microprogrammable bit-slice-type computer architecture.

generates the entry point in micromemory for the specific routine interpreting the fetched macroinstruction's opcode. The micromemory in turn outputs all the control signals required by the system to execute the macroinstruction, generate the next micromemory address, interact with main memory and I/O, etc.

Controllers may be implemented for simple sequential control circuits that do not have branching capabilities. In the simplest form of sequencer, only an address counter is required for stepping through the microinstruction. The address of the next microinstruction is selected by incrementing the address counter by one on each clock cycle. The counter technique permits only sequential control; neither conditional nor unconditional flow is possible. An improvement would be to load the address register with the next address from a field in the microinstruction. This configuration adds unconditional jumps in a program, but no conditional change in the flow of control. Logic and features could be added until a flexible LSI controller resulted.

GP501 Philosophy

There are two main thoughts behind the design of the GP501 EMC device. First, it is intended to minimize and in most cases eliminate additional control circuitry. Generally, the controller contains all the functions that are required, together with microprogram memory, to implement the control section of a computer.

Secondly, the EMC design emphasizes efficient use of micromemory. Generally, there is a trade-off in systems between execution speed and size of micromemory. The faster the machine, the larger the micromemory tends to be since it is desirable not to waste time in linking common microcode. The GP501 is designed with low overhead in mind for subroutine linkage. A fast machine also implies horizontal encoding of the microword; i.e., many bits in each word. It is a fact that in an LSI system; the number of micromemory chips has a dominating effect on cost. This is an additional incentive for a controller that uses micromemory efficiently.

ARCHITECTURE, PHYSICAL INTERFACE, AND OPERATIONAL FEATURES

Fig. 2 shows a block diagram of the GP501 EMC. The GP501 incorporates into one part many of the subsystems and capabilities required to emulate the control section of a bit-slice CPU. Some features of the EMC facilitate easy interfacing to the GP001,[2] an 8-bit bit-slice RALU in the same EPIC family, also implemented in CMOS/SOS

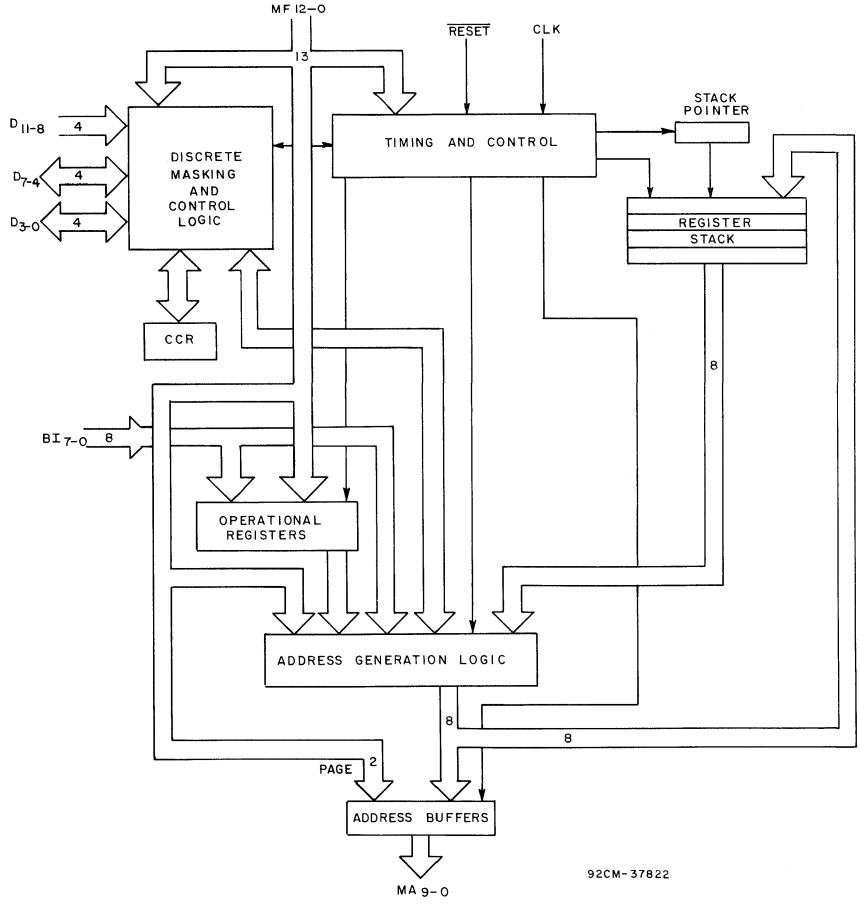


Fig. 2 - Internal logic structure of the emulating microcontroller.

technology. However, this does not preclude efficient use of the EMC with any other bit-slice GPU. A large number of registers, latches and counters are implemented on the chip. Most of these are under explicit program control.

Five operation registers (R4-R0) are dedicated to specific functions, such as masking, mapping, or the saving of common re-entry points. R0 and R1 are pointers to re-entry points that can be given control directly or conditionally. R2 is a pair of 4-bit mapping registers that can be used to transfer execution to one of sixteen micromemory locations, depending on other conditions, for example, external inputs. R4 is an address-masking register. R3 is a maskable address register that can be loaded from microcode or from the external bus.

Stack Registers/Program Counter

The currently active stack register, the one of four pointed to by the stack pointer, is the microprogram counter (PC). Normally, the PC is adjusted during the current microcycle so that it points to the next address at all times. The four stack registers permit three levels of microcode subroutines. The stack pointer wraps around in either direction. User control of the 2-bit stack pointer is through a reset input and pushing or popping the stack.

Branching and Sequence Control

Explicit unconditional branch and unconditional branch and link instructions provide for simple direct sequence control. In addition, the EMC offers a rich variety of other sequence control options, which are available for use in conjunction with counters and conditional-discrete features. The branch options are:

- Branch via branch register R0
- Branch via branch register R1
- Branch and link via branch register R1
- Return
- Return and link
- No-op (next address)
- Repeat (Same address)
- Map (LSB of address set according to discrete interface values)

Counting/Iteration

The 8-bit counters may be used to either count clock cycles while following normal program flow (sequential counting), or to dwell on a particular instruction while counting clock cycles (iterative counting). The two counters may be nested.

Conditional-Discrete Feature

The conditional discrete feature provides a means by which discrete interface bits may be tested and the result used in combination with branching options to provide a conditional two-way branching capability.

Mapping

The mapping feature allows values sampled at the bus interface (for example, a portion of the macroinstruction register) to be masked and merged with other values, stored internally, to generate the new memory address output, Fig. 3. This feature eliminates the need for the external mapping and/or interrupt vector ROMs/PLAs that would be required in an AM2910 implementation. The EMC's mapping feature provides a 256-way branch.

Translation

Translation is similar to mapping. Values at an internal data latch or at one of the 4-bit-wide discrete interface groups, which typically reflect machine or ALU status, can be masked and merged with the current PC. The feature provides for a 16-way relative branch based upon current machine state.

Discrete Interface/CCR

The discrete interface architecture provides for completion of carry-shift paths between ALU slices, combining of and operation upon ALU flags, and recording of discrete input states to an internal data latch. This data latch can be used as a machine Conditional Code Register (CCR). Group D11-D8 has a 4-bit XOR register associated with it. The register bits indicate whether D11-D8 is accepted in true or complement form. The content of the CCR may also be gated out to the discrete interface for use by the ALU, etc.

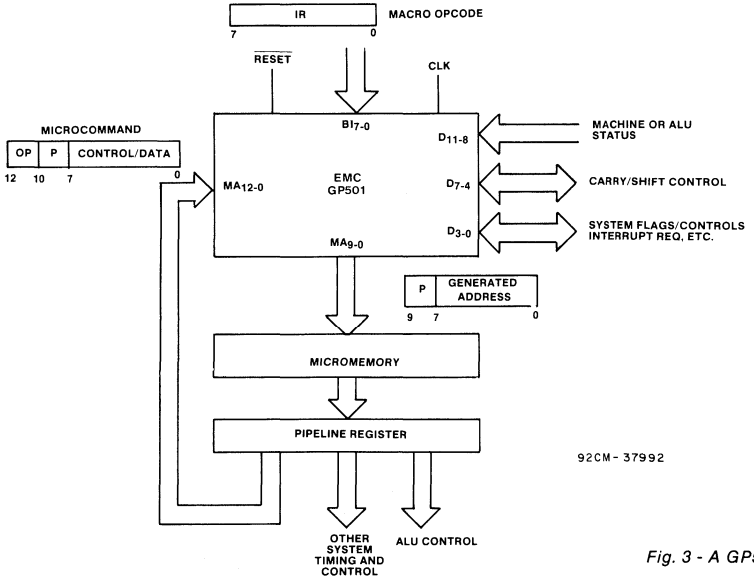


Fig. 3 - A GP501-based control section of a computer.

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INSTRUCTION SET

There are eight basic opcodes, but encoding of the 8-bit control/data field in the 13-bit microcommand provides for an unusually rich and powerful instruction set.

The 13-bit control word, Fig. 3, can be broken into four fields. The three MSBs are the opcode. The next two bits, MF9-MF8, are page bits that are generally passed through the controller. MF7-MF4 is either a branch address or a control field. The four LSBs, MF3-MF0, can be a branch address, a mask, a subcommand, or data to be loaded into a register-half or a counter-half.

Table A-1, Appendix A summarizes the eight basic instructions. For each opcode it shows the fields in the 13-bit control word, MF, and the generated result on the 10-bit memory-out lines, MA, which address the micromemory.

The use of some of these instructions may be unfamiliar to many programmers. But for a summary overview it is sufficient to keep in mind the purpose of any controller; i.e., to generate a next microprogram address. In the two first instructions, the 8-bit field is an immediate address field which is directly reflected on the output. In the remaining cases, the output is an address which is formulated or computed based on the content of the eight-LSBs in the control word. The result is generally a combination of bits derived from the interface (BI7-0, D11-0) and/or bits stored in internal operational registers. Sometimes the result is modified by an immediate mask in the control word, and in some cases internal logic operations are part of the process.

Thus, in general, for the EMC, all inputs needed in microcode sequencing are presented directly to the device (no additional hardware is required) and the next microprogram address is internally computed and presented at the MA output pins. A summary follows of the eight commands (also refer to Table A-1 Appendix A).

Opcode 0 is an unconditional branch. The lower 10 bits are the address of the next microinstruction. The lower 8-bit portion is incremented and loaded into the currently active stack register (SR).

Opcode 1 is an unconditional branch and link. The lower 10 bits are the next address as in command 0. However, the stack pointer (SP) is incremented prior to loading the incremented lower 8-bit portion of the microcommand into the SR. The net effect is to leave the previously active SR pointing to the location in micromemory just past the branch and link command. Execution continues using the new SR until a return is executed. A return causes the controller to pick the next address from the previously active SR.

Opcode 2 is the map command. The control and mask fields are used to formulate a new 8-bit address according to a table giving one of sixteen choices. The new address is made up from some combination of the value present at the bus interface (BI), the value in register R3, or the contents of the mapping register, R2. Immediate mask data is used either as a mask for the high nibble of the new address or as a bit selection map when applied to the low nibble by means of a right-justify function.

Opcode 3 is the translate command, Fig. 4. The new address is a formulated address determined by the control and mask fields. The control setting (one of sixteen) determines whether the currently active SR is updated or not. The new address is combined from the current PC, values at the discrete interface, DI, and/or the contents of the CCR. Some control settings also use the masking register R4 or immediate mask values applied as a bit map using a right-justify function.

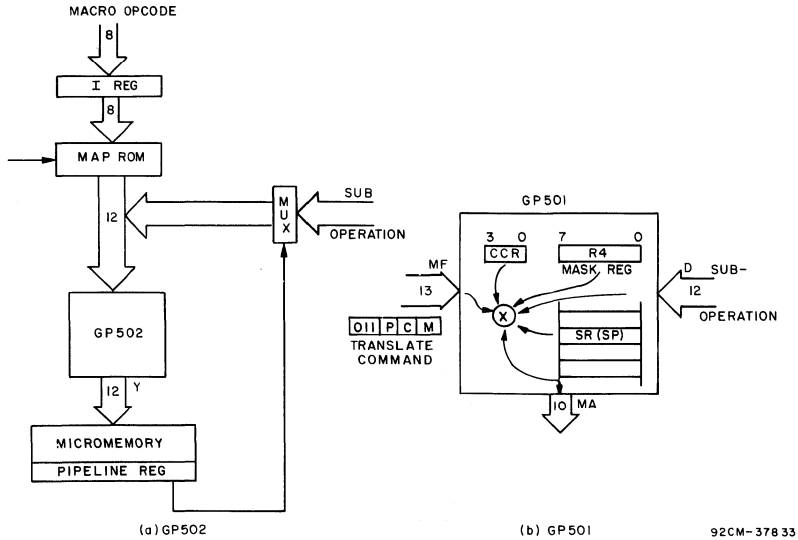

Fig. 4 - The translate command is similar to the map command, but in contrast also provides a 16-way relative branch. The two examples show how the address is generated from internal registers and/or external inputs.

Opcode 4 is the load command. This instruction allows the value in the immediate data field to be loaded into one of sixteen half registers. The next micromemory address comes from the current SR, which is then incremented.

Opcode 5 is the conditional-discrete set-up command. MF5-MF4 selects one of four sets of signals (the CCR, D11-8, D7-4, or D3-0) from the discrete interface to be examined. MF3-MF0 is a mask that determines which group of four signals selected by MF5-MF4 is to be examined. MF7-MF6 selects the logical operation to be performed on the selected inputs. If the mask is zero, the current CCR is used as a mask. Bits MF7-MF0 are all latched for later use. Once the command has set up a discrete operation, the result of the selected logical function is sampled during subsequent operations until a command 7 is executed. During command 7, the EMC examines the result of the latest discrete operation and branches according to the branch field in the command.

Opcode 6 is the immediate-count instruction. The command causes the count value to be placed into the holding and working registers for one of the two counters, and a count of the type specified to be initiated. If MF7 is zero, a sequential count starts. Execution continues in normal sequence until the count runs out. At count equals zero, a flag is set and the next instruction is determined by the branch instruction that was set up in the sequential-count subcommand.

In an iterative-type subcommand (MF7 = 1), the count is also loaded into an available counter. However, the branch condition determined by MF7-MF4 is taken immediately. The microcode instruction that results from the branch is repeated until the count runs out, and execution continues sequentially from the repeated microword.

Opcode 7 is the subop and branch command. It combines two semi-independent operations within one command. The suboperation specifies a utility function, for example, discrete-interface operation or counter operation. The branch operation is the means by which a conditional discrete equation (AND, OR, etc.) is sampled.

Some of the suboperations are various methods of loading the CCR. One subop is a no-op command, another loads register R3 from the bus interface, and another samples the discrete operation set up by opcode 5.

The branch option specifies one of sixteen possibilities when no discrete is pending, or one of thirty-two when coupled with the conditional-discrete evaluation feature.

USE OF REGISTERS AND INSTRUCTIONS

It is noteworthy that while the reset is active, the control word command is inhibited, with the exception of the load command. This arrangement makes it possible to load all addressable internal registers with the reset input active; i.e., complete initialization of the EMC while a device reset condition exists.

The load command is the means by which the EMC's operational registers are set. Among the addressable registers, only R3, the CCR, and the counter holding registers are altered by the action of other commands. Generally the registers will be set once during initialization. After that, the load command is most frequently used in loading counter-holding registers, the CCR, and managing the contents of the branching registers R0 and R1.

The branch (BR) and branch and link (BAL) commands provide direct control over microcode address generation. They are the only instructions for which control-word data is passed directly to the address output. The BAL command is the simplest means of invoking subroutine calls. It is typically used to execute frequently used sections of common code stored once, for example, a normalization routine used by all floating-point macroinstructions.

The map command provides the ability to generate branch addresses according to values present at or recorded earlier from the bus input port. Typical use is in the generation of microcode entry points for macrocode instruction execution and interrupt service.

The ability to latch bus data in register R3 allows the same piece of data to be referenced multiple times. Map cannot be used for relative branching, but can be used for vectoring.

The translate command is similar to the map command in that the program flow is modified according to values generated external to the EMC. However, in contrast to the map command, the stack register value is used in the address formulation. Thus, relative branches are possible based upon values present at the discrete interface. Processor flags and other status indicators are normally interfaced to the I/O pins.

There are basically two groups of translate commands. The first type updates the currently active stack register and causes a one-time n-way relative branch. The other type does not update the stack register, and is useful in tight iterative routines where one of N functions is executed until some event occurs. An example would be an asynchronous bus with I/O devices and handshake signals. A number of translate instructions could reference each other until the polled I/O device responds or a timeout occurs.

One of the translate commands degenerates into a no-op instruction with the next microcode address.

The conditional-discrete command is the most flexible of the conditional test operations. The command allows four logical operations, AND, OR, XOR, and XNOR, to be performed on any combination of input lines within a set (D11-8, D7-4, D3-0) or the CCR. The conditional-discrete command does not itself initiate a branch, but rather establishes the conditions under which a branch will or will not later be taken.

The EMC provides two counters called the outer and inner counters. In the non-nested mode, the outer counter is used. If, during the range of a sequential count, another count is invoked, the outer counter is held and the inner counter started. When the inner counter expires, the outer one resumes counting.

The simplest way to use the counters is through the immediate-count command. In the sequential type, the branch is taken when the count expires. The action is similar to "do loops," and nesting is possible. The command is useful in limiting sequences of microcode to a preset number of cycles without wasting time for in-line testing of limits. Typical uses would be multiply and divide macroinstructions where a known number of translate instructions are executed before exit.

The branch-before-count nature of the iterative type makes it useful for repeating in-line instructions. An example would be automatic repetition of a shift-one-bit instruction.

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The subop and branch command specifies two generally independent operations within the EMC: a branch and a data/utility function. Command 7 is the most powerful, but also the most complex command.

The data operation is used to load logic levels on input lines into the CCR, to transfer data between various lines, and to manipulate the count registers.

The branch directive field in the command specifies one of sixteen branch possibilities. If there is a conditional-discrete operation pending, each of these branch possibilities has a true/false option, raising the total to thirty-two possible branches.

Command 7 allows all microcode sequences emulating a macroinstruction to branch to the fetch routine and to load status into the CCR in one single instruction.

ADVANTAGES AND LIMITATIONS

The GP501 has several advantages over its companion EPIC IC, the Microprogram Sequencer GP502,[3] a CMOS/SOS version of the industry's popular sequencer, the AM2910. Fig. 5 shows that several MSI parts and extra logic are required to complete a GP502-implemented control section. For example, a mapping ROM is added in the GP502 section because there is never a one-to-one correspondence between the opcodes and the microprogram starting addresses that execute the macroinstructions. Similarly, a mapping ROM is required to decode the interrupt vectors to their interrupt-service-routine starting addresses.

In a GP502-based system, most decisions, testing, and storage functions are implemented by external circuitry, typically registers, latches, and multiplexers.

Some of the strong features and advantages of the GP501 may be illustrated with a real system. Many industry programs, both in preproduction stages and in current applications, employ the controller along with other EPIC chips. Applications include the NAVSTAR global-positioning system and emulation of both the Navy standard 16-bit minicomputer AN/UYK-20 and the MIL-STD-1750A instruction set.

Fig. 6 shows an implementation of a 1750A architecture in a simplified block diagram. The system provides the full processing capability of a large minicomputer, including floating point arithmetic, with both double precision and extended precision up to 48-bit-wide data manipulation. The main elements are two GP501 controllers, with concatenated 8-bit GPU slices (GP001) forming the general-processing section. The necessary interconnect logic to make up a working computer, in addition to micromemory, is integrated on a few LSI parts.

The dual controller approach allows efficient packing of microcode. It is based on the fact that most macroinstructions can be emulated with two sequences of microcode which can be independently shared with other macroinstructions. One class derives the operand, a register pair, an address, a memory word, etc. The other class executes generally an arithmetic or logical function: add, AND, complement, etc. Thus, the general processor is divided into two sections, or rather a computational section consisting of two 16-bit subsections that do 16-bit or 32-bit arithmetic when linked under microcontrol. A third 16-bit group primarily computes addresses and operands. For extended 48-bit precision, the three sections are concatenated. The micromemory is split in two halves. One bank controls primarily the execution processor, while the other one controls address generation, bus, and interrupt control.

Upon initiating a fetch cycle, a new macroinstruction enters the CPU through the bus-interface unit. The lower eight bits, which are operand specifiers or data, load the register-select unit. The upper eight-bits are the macro-

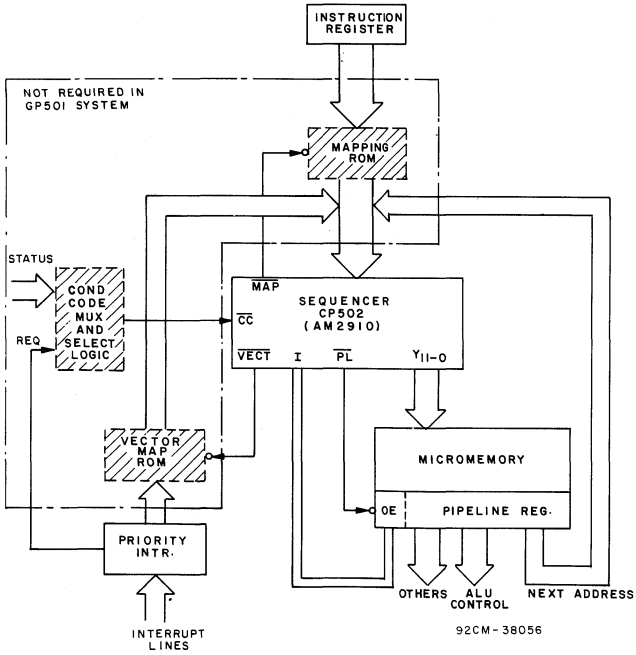

Fig. 5 - A GP502 implementation requires extensive external circuit support. A mapping function and conditional testing requires a minimum of three extra MSI parts.

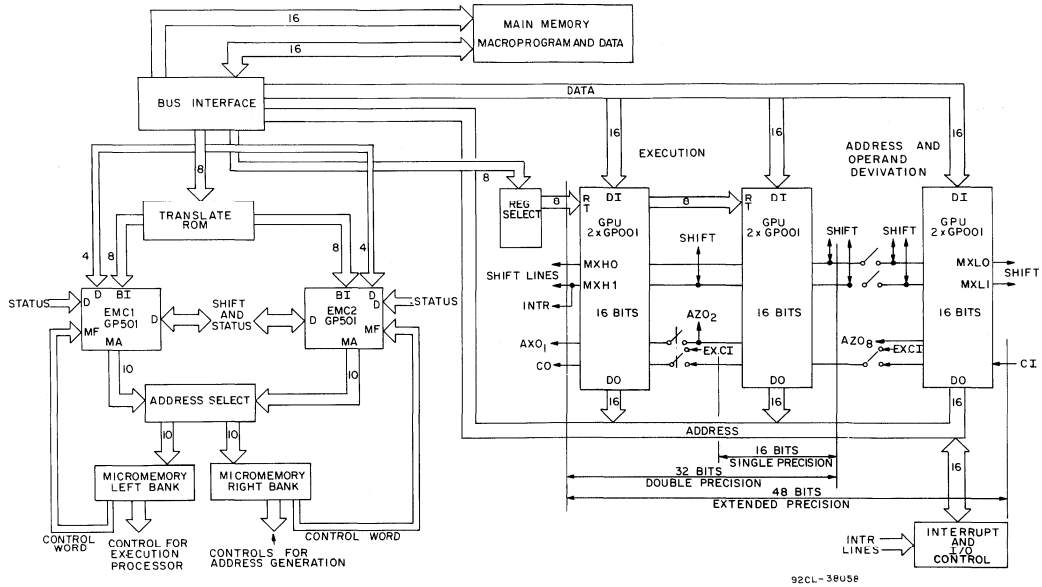

Fig. 6 - The control section of a 1750A computer uses two synchronized GP501 controllers to address micromemory. Concatenated 8-bit ALU slices form the general processing section, which comprises an execution part and an address and operand generation part. Operations can be performed on 16, 32 and 48-bit-wide data. A few LSI parts tie the whole system together.

opcode and address the translate ROM. This data is required to generate the entry points into the two microcontrollers. The control section uses the 8-bit addresses from the opcode-translate memory and microword bit fields to generate left and right address-selection data to the address-select unit. As discussed earlier, the controllers provide an extensive set of masking and data-manipulation functions that allow various combinations of external inputs to be mapped to new micromemory addresses. The address-select unit provides the means by which the two controllers synchronize the two halves of micromemory.

Arithmetic status (carry out (CO), accumulator zero (AZO), carry sign, and overflow on lines MXH0 and MXH1) is input directly to the execution controller and updates the internal CCR. The CCR can also output status and thereby build a machine-status word. EMC1 is used further to complete a ring-shift path for the MX shift lines of the execution processor. Testing of the output on the shift-lines in the same controller is used in multiply algorithms to decide when to add. subtract, or do nothing.

The design objectives for the GP501 have been met at the cost of some increased difficulty in understanding and complexity of application in comparison with the GP502 Microprogram Sequencer. Some of the GP501 instructions are a bit more complex than those of the GP502. Where micromemory requirements are large, the GP502 is the choice. And its operation is well documented and understood. However, despite these differences, programmers will find the effort and time required to exploit the powerful instruction set of the GP501 in a broad range of varied emulating designs worthwhile.

ACKNOWLEDGMENT

The parts in the EPIC CMOS/SOS family were developed under sponsorship of USAF, Air Force Materials Laboratory. The parts were designed by Tracor Aerospace Inc., and RCA Advanced Technology Laboratories.

REFERENCES

1. **GP501 Emulating Microcontroller (EMC),** RCA Solid State Preliminary Data Sheet.

   "A Guide to the Emulating Microprogram Controller GP501 - With Programming Examples," K. Karstad, RCA Solid State Application Note ICAN-7259.

   "Emulating Controller (GP501ADL) User's Guide," RCA Solid State Publication No. ECG-750.

2. **"An Introduction to the Use of the General-Processor Unit, GP001,"** K. Karstad, RCA Solid State Application Note ICAN-7202.

   "EPIC (Emulation and Programmable IC Family), CMOS 8-Bit Processor Unit (GPU)," RCA Solid State Data Sheet for the GP001, File No. 1324.

3. **GP502 Microprogram Sequencer,** RCA Solid State Preliminary Data Sheet.

   "A Comparison of EPIC CMOS/SOS Microprogram Controllers GP501 and GP502," K. Karstad, RCA Solid State Application Note ICAN-7283.

Appendix A

Table A-1 - Summary of Instructions

COMMAND	CONTROL WORD MF_{12-0}					RESULT				
	12 10	9 8	7 0							
	OP CODE	PAGE	ADDRESS, MASK, CONTROL, REG, SUBOP, etc.			MEMORY OUT (MA_{9-0})	STACK REG. (SR)	STACK PTR. (SP)	SELECTED REG.	FLAG
Uncond. Branch	000	P	Addr			P: Addr	MA_{7-0} + 1	N.C.		
Uncond. Branch & Link[a]	001	P	Addr			P: Addr	MA_{7-0} + 1	SP + 1		
Map[b]	010	P	Control		Mask	P: Formulated Addr	MA_{7-0} + 1	N.C.		
Translate[c]	011	P	Control		Mask	P: Formulated Addr	MA_{7-0} + 1	N.C.		
Load[d]	100	P	Reg.		Data	P: SR	SR + 1	N.C.	Data	
Cond. Discrete Set Up[e]	101	P	E	S	Mask	P: SR	SR + 1	N.C.		C.D. Set
Immed. Count[f]	110	P	T	Branch	Count	Branch option selected by branch Field	Depends on branch	Depends on branch		
Sub-op and Branch[g]	111	P	Branch		Subop	Branch option selected by branch Field	Depends on branch	Depends on branch		C. D. Reset

COMMENTS

[a] Currently active.
SR is not changed.

[b] FORM. Address from same combination, selected by control value of Bus In, Reg RA, Reg R3 and Immediate mask M.

[c] FORM. Address from same combination, selected by control value of current SR, value at Discrete Interface, Reg R4, CCR and Immediate mask M. No SR update if C = 4-7 and C-F

[d] Active also during reset.

[e] Equation select (E), Data Source Select (S) and Mask are recorded. Data source is Discrete Interface or CCR. testing via Opcode 7.

[f] T = 0, sequence; T = 1, iterate

[g] Subop specifies one of several Discrete Interface operations or counter operations. Subop F tests Condition Discrete set up.

A Comparison of EPIC CMOS/SOS Microprogram Controllers GP501 and GP502

by K. Karstad

The control section of a microprocessor gives the computer its "personality." The two main parts of the control section are the microprogram memory, which holds the micro-instructions, and the microprogram sequencer. The main purpose of any sequencer or controller is to present an address to the microprogram memory so that a micro-instruction is fetched and executed. This Application Note compares two such controllers or sequencers, EPIC family members GP501 and GP502,[1,2] from a functional and operational point of view. The GP502 is functionally and pin equivalent to the popular, bipolar, industry-standard AM2910, already well established in the industry; the GP501 is less known and understood. Both devices are implemented in CMOS/SOS technology. The addition of the SOS to the CMOS technology produces devices that offer excellent tolerance to radiation, an important factor in aerospace applications.

The GP501 Emulating Microcontroller, EMC, and the GP502 Microprogram Sequencer, which are essentially two small microprocessors with their own instruction sets, generate and transmit a "next address" to a micromemory or control store whose outputs are all the control bits required to manipulate the flow of data in the execution section of the processor. The controller may also be described as a "brain" that interprets the machine- or macro-instructions and orchestrates the interplay between the general processor, the I/O, and the main memory.

In this Note, the type of computer of which the GP501 and GP502 are a part is generally bit-slice organized and user-microprogrammable. Inherent in this architecture is high performance and the ability to emulate many instruction sets. In general, the power and sophistication of a computer depends to a large extent on the features of the controller.

In a GP502 (or functionally equivalent bipolar) based system, most decision, testing, and storage functions are implemented by external circuitry, typically registers, latches, and multiplexers. The GP501 EMC design minimizes, and in many cases eliminates, the need for additional control circuitry. Generally, the controller contains all the functions that are required, together with microprogram memory, to implement the control section of a computer.

The EMC design also emphasizes efficient use of micromemory. Generally, there is a trade-off in systems between execution speed and size of micromemory. The faster the machine, the larger the micromemory tends to be, since it is desirable not to waste time in linking common microcode. The GP501 is designed with low overhead in mind for subroutine linkage. A fast machine also implies horizontal encoding of the microwords, i.e., many bits in each word. It is a fact that, in an LSI system, the number of micromemory chips has a dominating effect on cost. This is an additional incentive for efficient use of micromemory.

At first glance it would seem that the design features of the GP501 have been included at some cost in simplicity of understanding and application. It is true that where micromemory requirements are large, the GP502 is the choice; however, where it is apparent that the special features of the GP501 will provide an advantage, users will find its evaluation very worthwhile.

THE GP501

Architecture

Fig. 1 shows a block diagram of the Emulating Microcontroller (EMC) GP501. This device incorporates into one part many of the subsystems and capabilities required in the control section of a bit-slice CPU. A large number of registers and latches are implemented on the chip; most are under explicit program control. Five operation register (R4-R0) are dedicated to specific functions, such as masking, mapping, or saving common re-entry points. R0 and R1 are pointers to re-entry points that can be given control directly or conditionally. R2 is a pair of 4-bit mapping registers that can be used to transfer execution to one of sixteen micromemory locations, depending on other conditions. R4 is an address-masking register. R3 is a maskable address register that can be loaded from microcode or from the external bus.

Refer to the system diagram in Fig. 2 while following the summary description of the GP501 given below.

Control Word - A 13-bit control word, normally supplied from the pipeline register, contains a 3-bit opcode, a 2-bit page address and an 8-bit control/data field. The treatment of the control/data field varies with the opcode, and is covered below in detail. Four 256-byte pages are possible. The page field is normally passed through to the memory address output field, MA.

Memory Address Out - The memory address output field is a 10-bit output field to micromemory. The two MSB's (most significant bits) are copied from the 2-bit page field in the control-word input. The lower eight bits are generated from the EMC. The details of address formulation are found below under the description of each operation code, or opcode.

Bus In - Eight bits of data can be latched into internal storage for subsequent use. A typical source is a macro-instruction opcode and extended bytes of the macroinstruction format.

Discrete Interface - The discrete interface is divided into three 4-bit groups: D11-8 are always inputs to the EMC. A programmable XOR mask is applied internally to these bits; therefore, low-true or high-true data can be applied without external hardware or microcode provisions. D_{7-4} are bidirectional, but normally in the input mode. D_{3-0} are independently alterable as inputs or outputs.

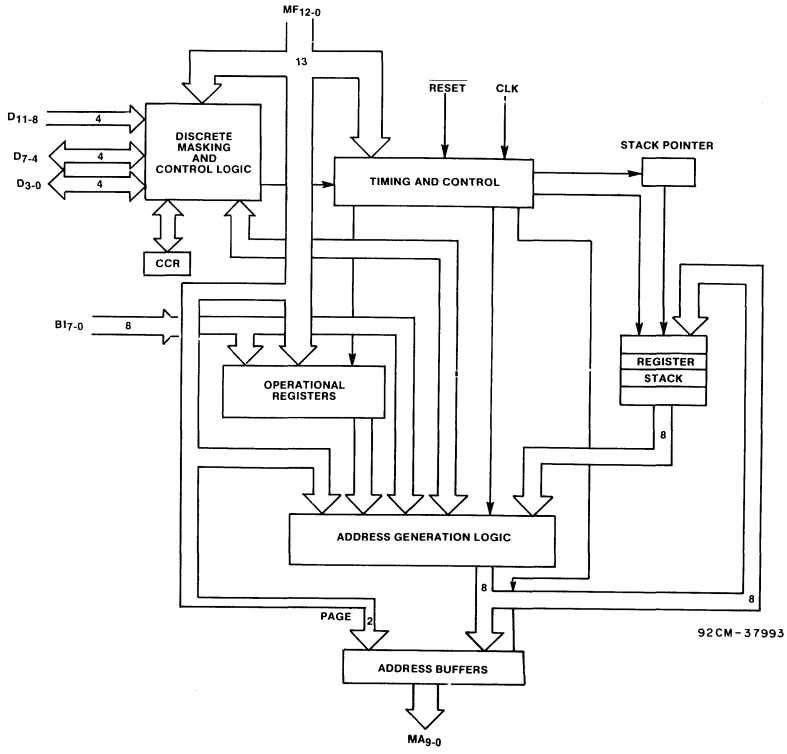

Fig. 1 - Architecture and logic of the microcontroller GP501.

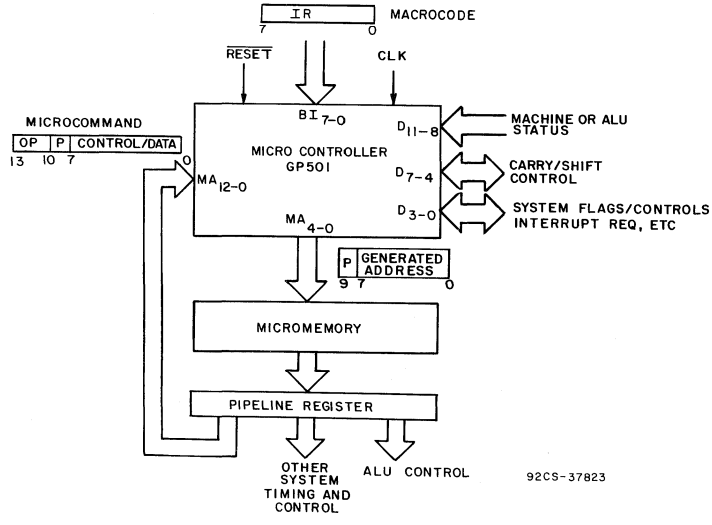

Fig. 2 - System operation of the GP501.

Clock - A low-to-high transition denotes the beginning of a microcycle. Internally, both positive and negative clock edges are used to latch data presented to the EMC. In general, inputs should be stable prior to and during the time the clock is at a high level.

Stack Registers/Program Counter - The currently active stack register, the one of four pointed to by the stack pointer, is the program counter (PC), Fig. 1. Normally, the PC is adjusted during the current microcycle so that it points to the next address at all times. The four stack registers permit three levels of microcode subroutines. The stack pointer wraps around in either direction. User control of the 2-bit stack pointer is only via the reset input and through pushing or popping the stack.

Reset - Reset is low-true and does the following when active: Clears all internal counter flags, clears conditional discrete active flag, sets the stack pointer to zero, and forces the memory address output to all zeros.

Instruction Set

There are eight basic operation codes, or opcodes, in the instruction set of the GP501, but encoding of the 8-bit control/data field in the 13-bit microcommand provides for an unusually rich and powerful instruction set. For example, opcode 7 offers sixteen different suboperations, or subops, and for many of these there are no less than thirty-two variants.

The 13-bit control word can be broken into four fields. The three MSBs define the opcode. The next two bits (MF9-MF8) are page bits that are generally passed through the controller. MF7-MF4 designate either a branch address or a control field. The four LSBs (MF3-MF0) can be a branch address, a mask, a subcommand, or data to be loaded into a register-half or a counter-half.

When a 4-bit instruction is applied to the GP502 sequencer, the memory address output (Y) is essentially determined by selecting one of several sources. The source can be the output from the mapping ROM, the pipeline register, the stack, and so on. In the case of the GP501 EMC, the control word includes, in addition to the 3-bit opcode, an 8-bit field that is interpreted by the controller in many ways. In the two first instructions, the 8-bit field is an immediate-address field which is directly reflected on the output. In the remaining cases, the output is an address that is formulated or computed from the contents of the eight LSBs in the control word. The result is generally a combination of bits that are input at the interface (BI_{7-0}, D_{11-0}), stored in internal operational resisters, and modified by an immediate mask in the control word. In some cases, internal-logic operations are part of the process. Thus, for some opcodes, there are up to sixteen, and sometimes thirty-two, sub-operations.

In general, for the GP501 EMC, all inputs needed for microcode sequencing are presented directly to the device (no additional hardware is required), and the next microprogram address is internally computed and presented at the MA output pins.

Below is a brief summary of the basic features of the instruction set of the GP501. Each opcode description is accompanied by an illustration that shows microprogram flow as various microprogram memory words are executed. Each dot in the illustration is a microword; the one currently being executed is encircled. The illustrations show how the next address is generated when a new microcommand is executed, and how the stack register (program counter) and stack pointer are updated.

Opcode 0, Fig. 3, is an unconditional branch. The lower ten bits are the address of the next microinstruction. The lower 8-bit portion is incremented and loaded into the currently active stack register (SR).

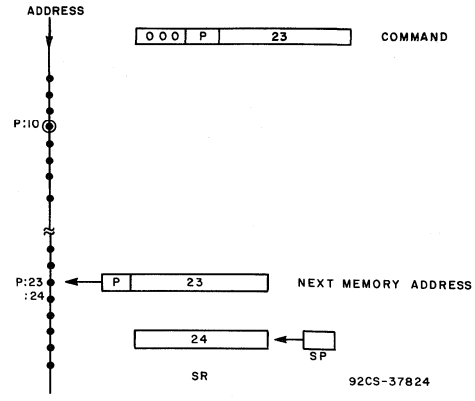

Fig. 3 - Opcode 0 - unconditional branch.

Opcode 1, Fig. 4, is an unconditional branch and link. The lower ten bits are the next address, as in command 0. However, the stack pointer (SP) is incremented prior to loading the incremented lower 8-bit portion of the microcommand into the SR. The net effect is to leave the previously active SR pointing to the location in micro-memory just past the branch and link command. Execution continues using the new SR until a return is executed. A return causes the controller to pick the next address from the previously active SR.

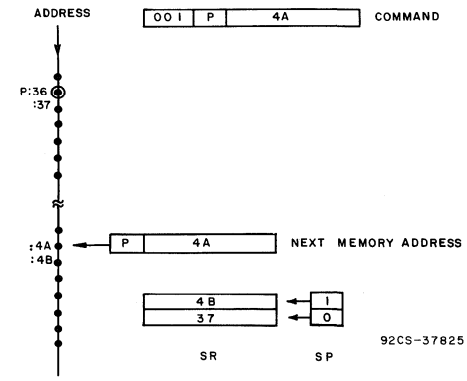

Fig. 4 - Opcode 1 - unconditional branch and link.

Opcode 2, Fig. 5, is the map command. The control and mask fields are used to formulate a new 8-bit address according to a table giving one of sixteen choices. The new address is formulated from some combination of the value present at the bus interface, the value in register R3, or the value in mapping-register R2. Mask data is used either as a mask for the high nibble of the new address or as a bit-selection map when applied to the low nibble through the use of a right-justify function.

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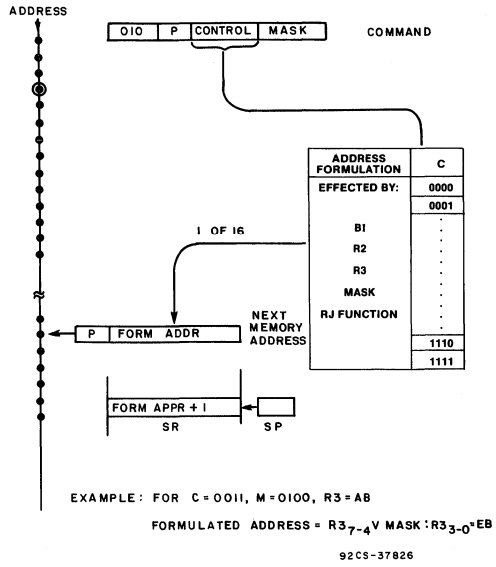

Fig. 5 - Opcode 2 - map.

Opcode 3, Fig. 6, is the translate command. The new address is a formulated address determined by the control and mask fields. The control setting (one of sixteen) determines whether the currently active SR is updated. The new address is formulated from the current PC, values at the discrete interface, and/or the contents of the condition-code register (CCR). Some control settings also use the masking register, R4, or mask values applied as a bit map using a right-justify function.

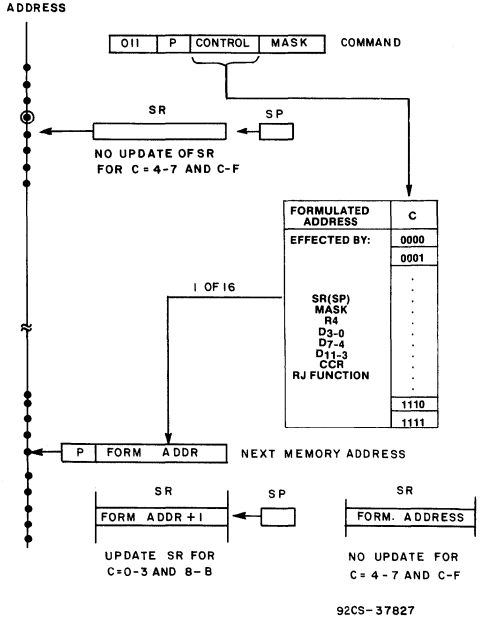

Fig. 6 - Opcode 3 - translate.

Opcode 4, Fig. 7, is the load command. This instruction allows the value in the immediate-data field to be loaded into one of sixteen half registers. The next micromemory address comes from the current SR, which is then incremented.

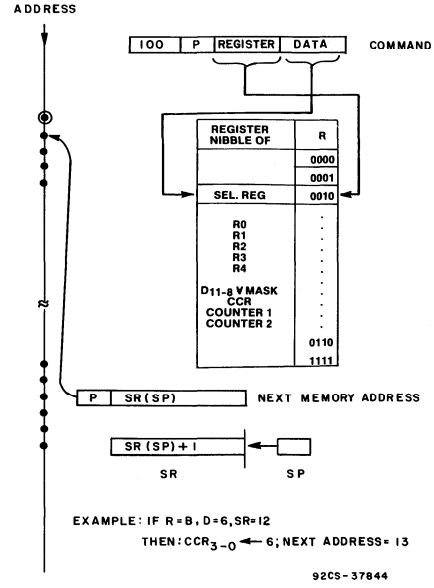

Fig. 7 - Opcode 4 - load.

Opcode 5, Fig. 8, is the conditional discrete set-up command. MF5-MF4 select one of four sets of four signals from the discrete interface to be examined. MF3-MF0 are a mask that determines which of the four signals selected by MF5-MF4 are to be examined. MF7-MF6 select the logical operation to be performed on the selected inputs. If the mask is zero, the current CCR is used as mask. Bits MF7-MF0 are all latched for later use.

Once the command has set up a discrete operation, the result of the selected logical function is sampled during subsequent operations until a command 7 is executed. During command 7, the MCU examines the latest discrete operation result and branches based on a portion of the command 7 code.

Opcode 6, Fig. 9, is the immediate-count instruction. The command causes the count value to be placed into the holding and working registers for one of the two counters, and a count of the type specified is initiated. If MF7 is zero, a sequential count is started. Execution then continues in normal sequence until the count runs out. When the count equals zero, a flag is set and the next address is determined by the branch instructions that were set up in the sequential-count subcommand.

In an iteration-count subcommand (MF7=1), the count is also loaded into an available counter. However, the branch condition determined by MF7-MF4 is taken immediately. The instruction that results from the branch is then repeated until the count runs out; execution continues sequentially from the instruction that was repeated.

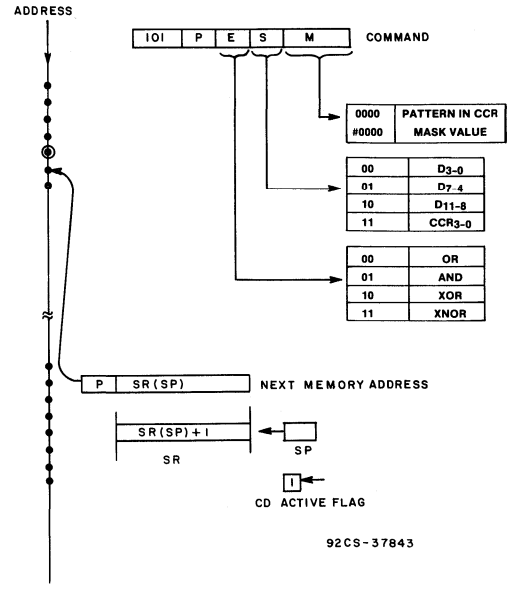

Fig. 8 - Opcode 5 - conditional discrete set-up.

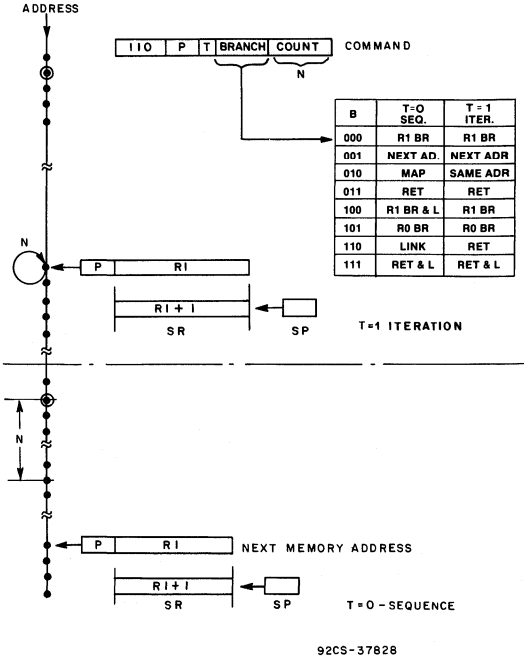

Fig. 9 - Opcode 6 - immediate count.

Opcode 7, Fig. 10, is the subop and branch command. The command combines two semi-independent operations within one command. The suboperation specifies a utility function (for example, discrete-interface operation or counter-operations). The branch operation is the means by which the conditional-discrete equation is sampled.

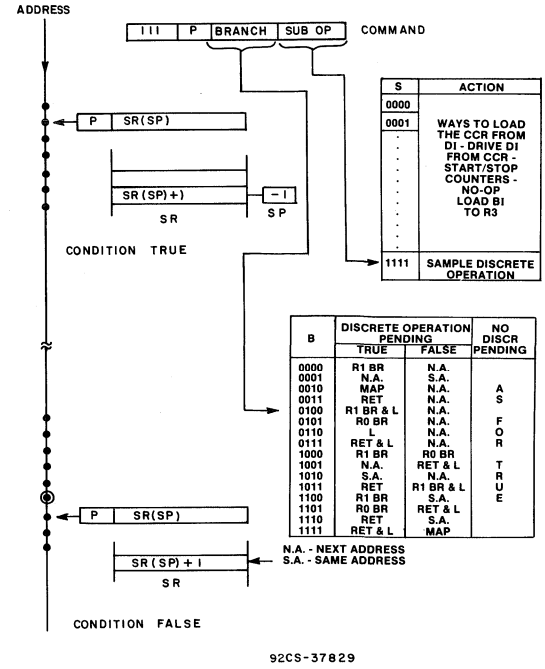

Fig. 10 - Opcode 7 - subop and branch.

Some of the suboperations are various methods of loading the CCR. One subop is a no-op command. Another loads register R3 from the bus interface. Subop F samples the discrete operation set up by opcode 5.

The branch option specifies one of sixteen possibilities when no discrete is pending, or one of thirty-two when coupled with the conditional-discrete evaluation feature.

THE GP502

Architecture

The GP502, shown in functional block form in Fig. 11, allows addressing of up to 4K words of microprogram. The controller contains a four-input multiplexer that is used to select either the register/counter direct input, microprogram counter, or stack as the source of the next microinstruction address.

The register/counter is the source when a load instruction is used and the $\overline{RLD}$ (register load) line is low. The counter is loaded from DI, the discrete interface, on a positive clock pulse. The second source for the multiplexer is the direct inputs. This source is used for branching. The GP502 contains a 12-bit microprogram counter and incrementer. When the carry-in to the incrementer is high, the microprogram register is loaded on the next clock cycle with the current output word plus one. Sequential

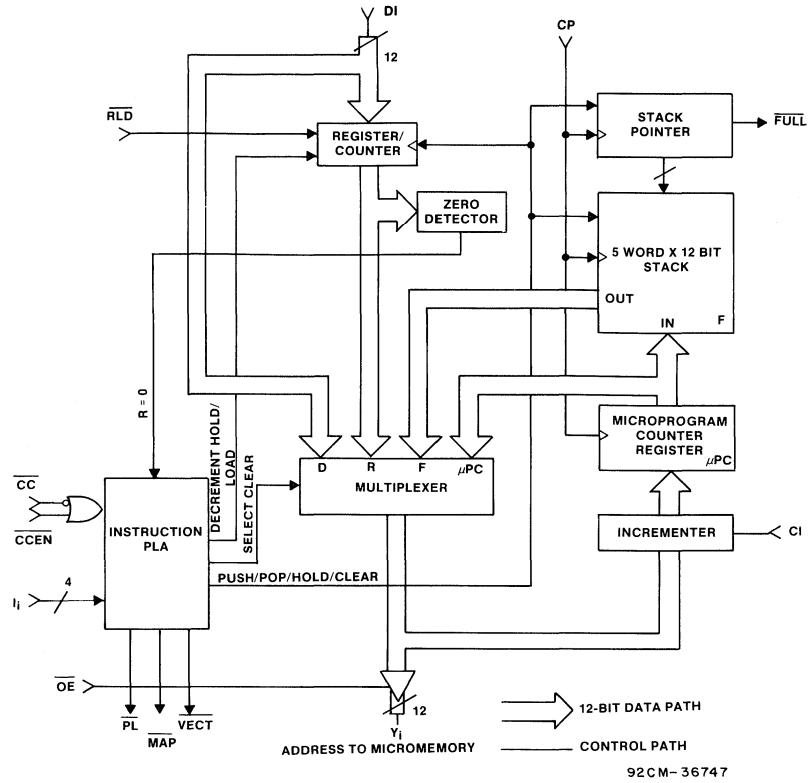

Fig. 11 - Block diagram of the microcontroller, GP502.

microinstructions are thus executed. When the carry-in is low, the incrementer passes the output word unmodified, so that the microprogram counter is reloaded with the same word on the next clock cycle. The same microinstruction is thus executed any number of times. The fourth source at the multiplexer is a 5-word by 12-bit stack used to provide return-address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer, which always points to the last file-word written.

Sixteen instructions are implemented in the GP502 by a 4-bit input field, I. The instructions control not only the source to the multiplexer, but also three enable signals: $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$. For each instruction, only one of these three outputs is active. They normally control three-state enable pins to the primary source for microprogram jumps. $\overline{PL}$ normally enables the next address field of a pipeline register. $\overline{MAP}$ enables a PROM, which maps the macroinstruction starting addresses. $\overline{VECT}$ enables a third source, usually the vector output of an interrupt controller. External parts must be added to the sequencer to obtain these features.

Instruction Set

Table I summarizes the sixteen instructions of the GP502 that select the address of the next microinstruction to be executed. The table shows the result of each instruction in controlling the multiplexer that determines the Y outputs, and in controlling the three enable signals $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$. For each instruction, one and only one of the latter three output signals is low. If these outputs control three-state enable signals for the primary source of microprogram jumps, the three-state sources can drive the D inputs without further logic.

Four of the GP502 instructions are unconditional: their effect depends only on the instruction. Ten of the instructions have an effect which is partially controlled by an external data-dependent condition. Three of the instructions have an effect which is partially controlled by the contents of the internal register/counter.

In the ten conditional instructions, the result of the data-dependent test is applied to $\overline{CC}$. If the $\overline{CC}$ is low, the test is considered to have passed, and the action specified in the name occurs; otherwise, the test has failed and an alternate action occurs.

As an example of using the table, consider instruction CJP, Conditional Jump Pipeline. The $\overline{PL}$ output is enabled, but only if the test passes ($\overline{CC}$ is low), D is the source for the next micromemory address, and the branch is executed. If the test fails, $\overline{CC}$ is high, and the next address is selected from the program counter; i.e., the program continues with the next instruction. In either case, the contents of the stack and the register/counter are unaffected.

USE OF THE GP501 VERSUS THE GP502

The various functions of a microprogram controller can be described in terms of three classes of operation: how the macroinstruction (derived from main memory) is interpreted, how the microcommands are sequenced, and how the controller operates on external inputs unique to system

Table I - GP502 Instructions

			REG/ CNTR CON-	FAIL $\overline{CCEN}$=LOW and $\overline{CC}$=HIGH		PASS $\overline{CCEN}$=HIGH or $\overline{CC}$=LOW			
I_3-I_0	MNEMONIC	NAME	TENTS	Y	STACK	Y	STACK	REG/ CNTR	ENABLE
0	JZ	JUMP ZERO	X	0	CLEAR	0	CLEAR	HOLD	PL
1	CJS	COND JSB PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/COND LD CONTR	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	COND JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP VECTOR	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP, CNTR≠0	≠0	F	HOLD	F	HOLD	DEC	PL
			= 0	PC	POP	PC	POP	HOLD	PL
9	RPCT	REPEAT PL, CNTR≠0	≠0	D	HOLD	D	HOLD	DEC	PL
			= 0	PC	HOLD	PC	HOLD	HOLD	PL
10	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
11	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
12	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
13	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
14	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
15	TWB	THREE-WAY BRANCH	≠0	F	HOLD	PC	POP	DEC	PL
			= 0	D	POP	PC	POP	HOLD	PL

Note 1: If $\overline{CCEN}$ = Low and $\overline{CC}$ = High, hold; otherwise load. X = Don't Care.

architecture. The comparison of the GP501 and the GP502 below follows these classifications, although some overlapping of functions is unavoidable. In the accompanying figures, part (a) always represents the GP502 and (b) the GP501.

Macroinstructions and Machine Sub-Operations Mapping - Typically, the opcode of a macroinstruction is stored in the upper half of the instruction register (in a 16-bit machine), Fig. 12(a), the GP502. Since there is almost never a one-to-one correspondence between the opcode and the

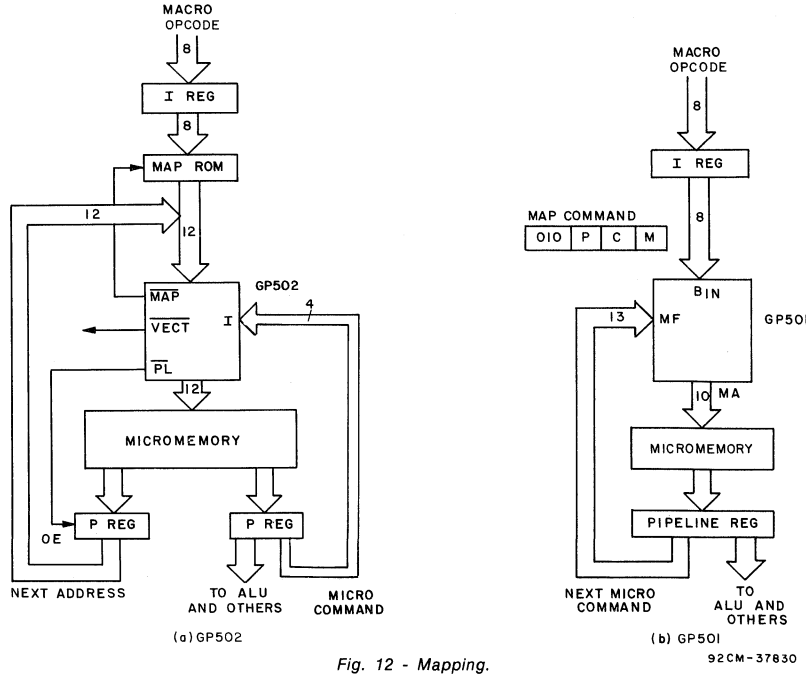

Fig. 12 - Mapping.

starting address of the microcode sequence that executes a particular macroinstruction, a mapping ROM is required to translate opcodes into microcode entry points. To input this address source, a JMAP (jump map) instruction (I=2) must be executed to enable the map control line. For all other instructions, the address is multiplexed from some other source.

For the GP501, Fig. 12(b), the newly mapped MA address can be derived from the BI input, modified as desired by map-command 2. If control C and immediate mask are zero, MA is simply equal to the bus input. However, the high and low nibble of MA can be formulated in a number of ways by combining bits from preloaded-map register R2 and a preloaded maskable address register, R3, in combination with a right-justify function applied to the low nibble. In short, masked transfer of fields from the bus input to memory address is possible without external hardware.

Temporary Storage - Fig. 13(a) shows how a 12-bit register (timeshared as a counter) is used for temporary storage in the GP502. The register can be loaded explicitly by the LDCT (load counter and continue) instruction or during any instruction by activating the $\overline{RLD}$ line.

In the case of the GP501, Fig. 13(b), the maskable address register, R3, can be loaded directly from the bus input using a suboperation of command 7. Hence, secondary and tertiary decoding of the fields in the macroinstruction is easily accomplished. Note that R3 can also be loaded by immediate data in load command 4.

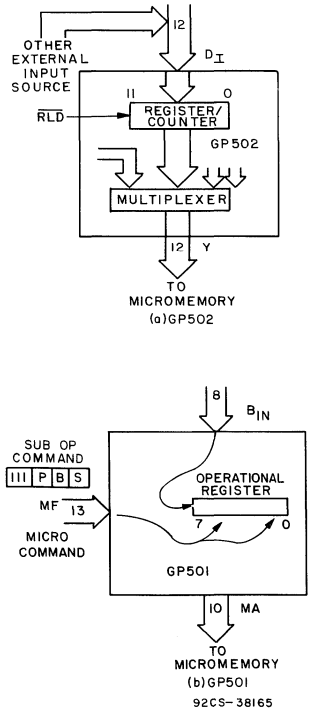

Fig. 13 - Temporary storage.

Field Extractions - As shown in Fig. 14(a) decoding of operand specifiers and fields in the macroinstruction typically requires external multiplexing in the GP502. Fig. 14(b) shows that the GP501 can extract bits from the macrofield by using only the map instruction. This situation is similar to the case described for Fig. 12(a). As an example of GP501 use, consider a bus input where only the high nibble is of interest. The GP501 user's guide[3] shows that a map instruction with control value C=0100 and immediate mask M=0000 will generate BI_{7-4}:0000 on the eight LSBs of MA.

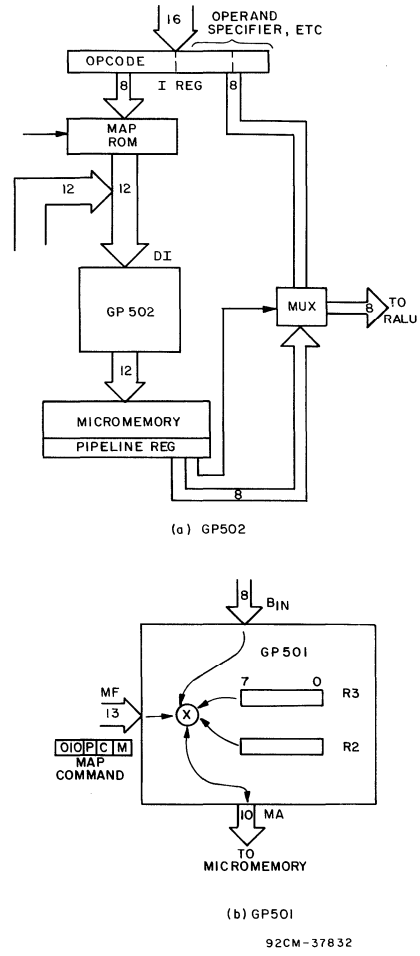

Fig. 14 - Field extractions.

External Suboperations - Assume that the sequencing of microcode addresses depends upon some external system operation. It could be I/O operation where a number of asynchronous handshaking signals are available. These signals are tested, and generally a timeout is activated, to prevent hanging up the processor if the peripherals do not respond. As indicated in Fig. 15(a), the handshake signals must be multiplexed into the standard DI inputs for the GP502.

In the case of the GP501, Fig. 15(b), four handshake signals could be input directly to discrete-interface bits D_{11-8}, and a translate instruction executed. Again, consult the user's guide, and as an example, use control value C=1110 and immediate mask=1111. If the high nibble of the internal mask register (R4) had been preloaded with zero, the newly formulated address on MA would be of the form:

$$FA = SR(SP)_{7-4} : D_{11-8}$$

This translate command inhibits updating of the program counter (SR(SP)), and the least-significant nibble of the generated next address is derived from discrete-interface bits D_{11-8}. The overall result is that the instructions will reference each other within a block without updating the stack register until the test is satisfied or timeout occurs.

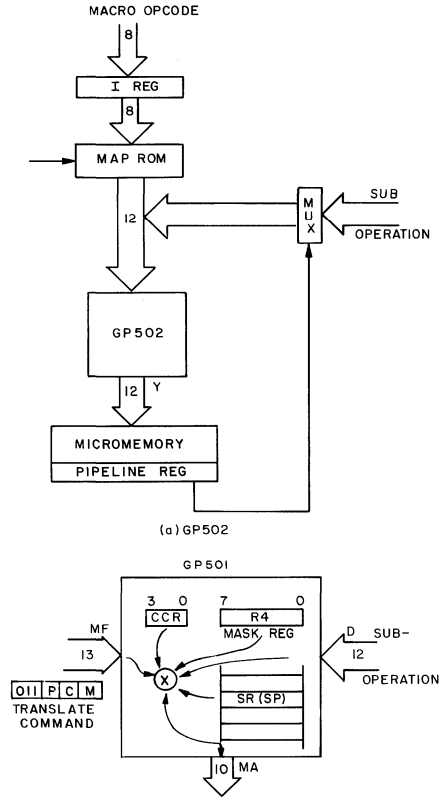

Fig. 15 - External suboperations.

The address of the bus timeout procedure could be branch-register R1. A sequence counter is used to count machine cycles. If and when that count expires, a branch via R1 is made to the timeout handler.

In the simplest case of the example above, a fixed suboperation code maps directly into a new branch address. In this case, a control-value C in the translate command is chosen that will update the stack register.

$$(SR(SP):MA_{7-0}+1)$$

Sequencing of Microcode

Capacity - The GP502 can handle 4096 words of micro-memory, while the GP501 is limited to 1024 words, Figs. 16(a), (b). Neither part is directly expandable through bit-slice organization. Note that the GP502 incorporates three-state control of the output bus. The GP502 requires 40 pins versus 48 for the GP501.

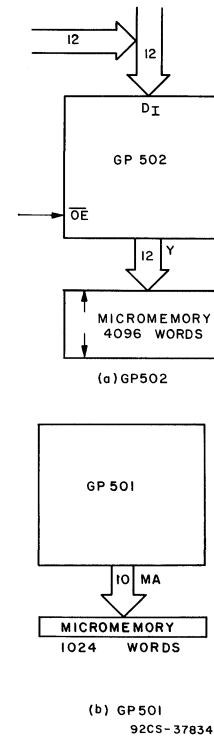

Fig. 16 - Capacity.

Counting - The GP502, Fig. 17(a), has one 12-bit counter which is also timeshared for temporary storage. The counter is used for loop counting and iteration, but requires explicit in-line testing for an end-of-loop (I=13) condition on content-equal-zero (I=9) and repeat loop (CNTR≠0).

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As shown in Fig. 17(b), the GP501 has two 8-bit counters with associated holding registers. The counters can be selected to iterate (hold same address until the count is zero) or to sequence (continue normal microcode flow until the count is zero). In both cases, the exit addresses are set up at the beginning and the branching is done automatically. The counts can be nested in an inner and outer count. Nested counts occur when one count is active and another count is pending. The dual-counter implementation allows the entering and execution of sections of microcode without the need to insert testing and exit commands.

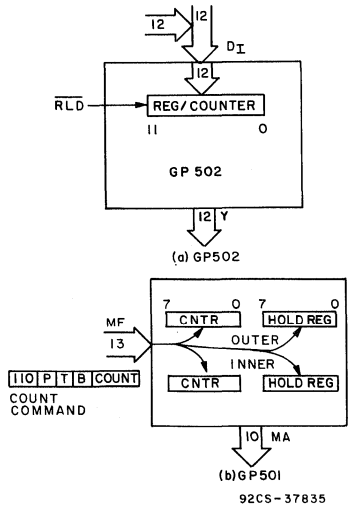

Fig. 17 - Counting.

Subroutine Management - The GP502, Fig. 18(a), has a five-word stack that provides four levels of subroutines. A full stack is indicated by the output signal "full." Any further "pushes" onto a full stack overwrites information at the top of the stack, but leaves the stack pointer unchanged. Subroutine management is done by pushing and popping the stack by using specific instructions.

The GP501, Fig. 18(b), provides only three levels of subroutines, and the stack wraps around in either direction. There is no stack-full indication.

The architecture of the GP501 EMC provides a great number of options for subroutine linkage. Opcodes 6 and 7 contain 3- and 4-bit branch fields, respectively; the options for the branch-select codes are listed in the user's guide[3] and summarized below:

1. It is possible to count sequentially and do a return when the count runs out.
2. Registers R0 and R1 can contain addresses of frequently used entry points, typically, the address of the fetch routine.
3. Conditional testing can be done within counts. A selected link option serves as a default if the count expires.
4. Sequential microcode can be counted and the return address saved while counting using a link instruction.
5. The return-and-link instruction will maintain the common return entry point.
6. The XOR of the discrete bits DO and D1 can be mapped into the least significant bit of the memory output, with $MA_{7-1} \leftarrow SR(SP)_{7-1}$ while the currently active stack pointer and stack register remain unchanged.

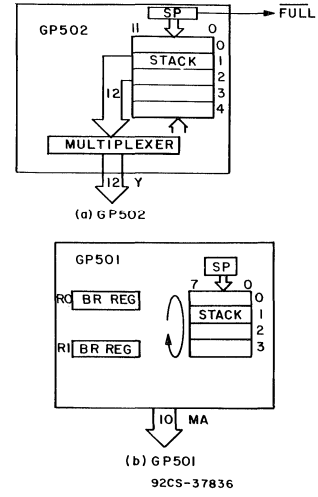

Fig. 18 - Subroutine management.

Conditional Testing - Conditional testing of status, typically such ALU statuses as carry and overflow, requires external multiplexing to the single-input $\overline{CC}$ for the GP502, Fig. 19(a).

The GP501, Fig. 19(b), accepts a number of status signals directly at the discrete interface (DI). Opcode 5 allows logical OR, AND XOR, and XNOR to be performed on any combination of these input bits by applying an immediate mask value or the contents of the prestored CCR register as a mask.

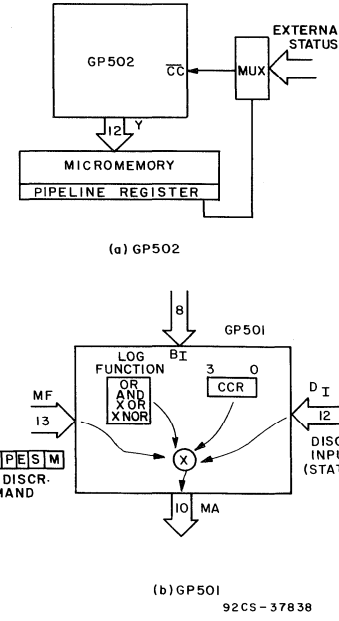

Fig. 19 - Conditional testing.

Note that opcode 5 sets up the conditional test only. The branch or no-branch operation takes place when the set-up is tested using a suboperation of opcode 7.

Set-up and testing is entirely an internal operation.

Bit Insertion - Frequently, subroutines are data dependent; for example, multiply and divide routines require bit-testing. In a GP502 implementation, this data dependence dictates that multiplexing be done to input the bits, Fig. 20(a).

In a GP501 system, Fig. 20(b), the bits are applied directly to the discrete interface (DI); the translate command allows insertion of up to four bits into the least significant bits of the address base. In one group of translate commands, the currently active stack register is not incremented. This feature allows iterative routines where one of a certain number of functions is to be executed until some specific event occurs.

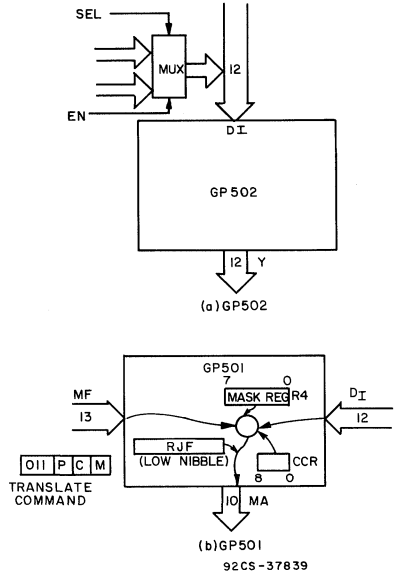

Fig. 20 - Bit insertion.

System-Related Functions

System Status - Conditional testing was described earlier. Typically, ALU status can be input directly to the GP501 via the discrete interface and operated upon either with prestored values in the CCR or an immediate-mask value. However, the contents of the CCR can also be read out over the discrete interface. This feature allows the programmer to build a machine status word from distributed status bits in the system, Fig. 21(b).

Shift and Rotate - In a GP502 system, external multiplexers are required to complete shift/rotate functions, Fig. 22(a).

The GP501, Fig. 22(b), contains internal circuitry that can be microprogrammed to complete the shift paths for the general-processor GP001 bit-slice.[4]

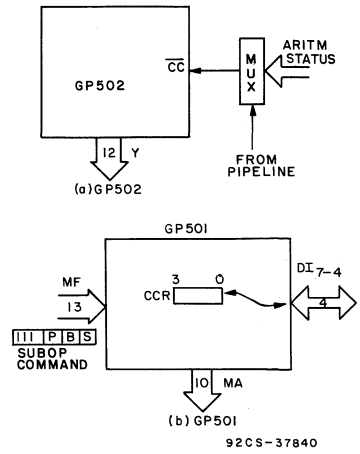

Fig. 21 - System status.

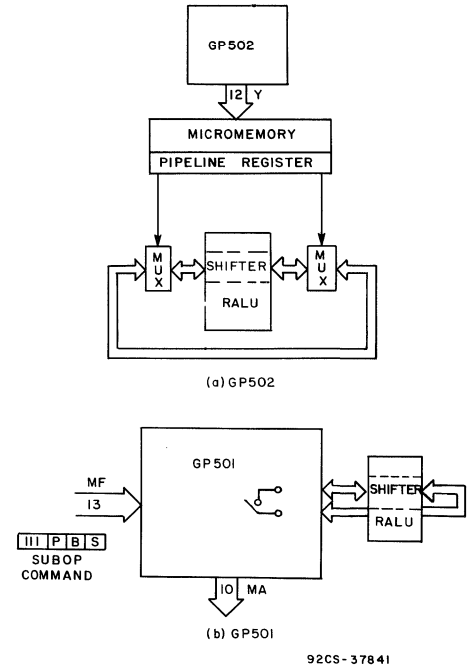

Fig. 22 - Shift and rotate.

Initialization - Initialization or restart of the GP502 requires special consideration. One way to provide this consideration is to use an external multiplexer and force the instruction I to zero, which is the jump-zero instruction, and which sets the program counter to zero, Fig. 23(a). Another method is to use pull-up resistors on the output lines of the sequencers and place a jump zero instruction at micromemory location FFF.

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The GP501, Fig. 23(b), has a reset input pin. When activated, the stack pointer and memory output is set to zero. Internal counters are deactivated and the conditional discrete flag is reset.

Note that the load command can be used in the reset state.

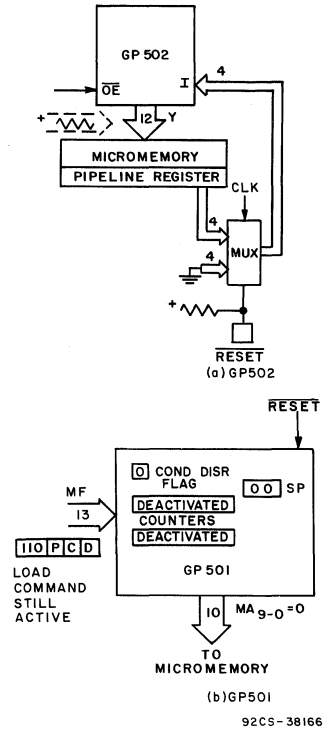

Fig. 23 - Initialization.

REFERENCES

1. "A Guide to the Emulating Microprogram Controller GP501—With Programming Examples," K. Karstad, RCA Solid State Application Note ICAN-7259.
2. GP502 Microprogram Sequencer, RCA Solid State Preliminary Data Sheet.
3. "Emulating Controller (GP501ADL) User's Guide," RCA Solid State Publication No. ECG-750.
4. "An Introduction to the Use of the General-Processor Unit, GP001," K. Karstad, RCA Solid State Application Note ICAN-7202.
   "EPIC (Emulation and Programmable IC Family), CMOS 8-Bit General Processor Unit (GPU)," RCA Solid State Data Sheet for the GP001, File No. 1324.

Reliability of CMOS/SOS Integrated Circuits

by H. Veloric, M.P. Dugan,
W. Morris, R. Denning, G. Schnable

Complementary-MOS integrated circuits based on the silicon-on-sapphire technology (CMOS/SOS) offer many advantages,[1-15] including high circuit density, very high speed, low power dissipation during high-speed operation, substrate isolation, wide operating-voltage range, freedom from latchup, designability, scalability, and testability. CMOS/SOS has been the technology of choice for a number of advanced applications, and integrated circuits based on silicon-on-sapphire (SOS) technology are being fabricated in a number of organizations.

Presently available SOS ICs have benefited from improvements in SOS substrates, designs, materials, processes, and in-process controls, and thus both yield and reliability are superior to those of devices fabricated a number of years ago. New process improvements have been evaluated and applied to developing SOS devices.

The potential advantages of silicon-on-sapphire dielectrically isolated integrated circuits for radiation-hardened applications have been recognized for some time.[16-23] Techniques have been developed that further improve the radiation hardness of silicon-gate CMOS/SOS integrated circuits.[24-30]
The CMOS/SOS technology has many features that have reliability implications. Examples include freedom from the possibility of field inversion, freedom from the possibility of punch-through or of parasitic lateral bipolar-transistor action between adjacent devices, freedom from the possibility of four-layer parasitic device latchup, freedom from problems due to vertical metal-spiking across source/drain junctions, no need for a grown field oxide, and the possibility of input-protection circuits that cannot be implemented in bulk-CMOS technologies. These CMOS/SOS-technology advantages become increasingly significant as integrated circuits are scaled to smaller dimensions.

An additional advantage of a dielectric-isolation technology is that it is easier to fabricate higher-voltage and radiation-hardened circuits because there is no possibility of field inversion, or of punchthrough to adjacent devices or to the edge of a well. By contrast, bulk-MOS processes involve a tradeoff between field-inversion voltage and avalanche-breakdown voltage. Ion implantation is used for bulk-MOS devices to increase field-inversion voltage; it is applied using a pattern that masks the channel region but allows overlap with the subsequently ion-implanted source and drain regions. This overlap is essential to achieve high-density circuits. Only SSI and MSI CMOS circuits can provide the space for a separate channel-stop diffusion that is located some distance away from source and drain regions.

The ability to fabricate integrated circuits that function at higher voltages than the intended application voltage has significant reliability implications, as it permits burn-in of circuits at high applied voltages, which in turn results in effective screening of failure mechanisms that are greatly accelerated by voltage but relatively insensitive to temperature. Two examples of failure mechanisms that are very effectively screened by high-voltage tests are time-dependent dielectric breakdown of gate oxides and hot-electron effects in short-channel MOS transistors. If CMOS/SOS integrated circuits are burned-in at 125°C and 11 V, for example, and are subsequently used in an electronic system under conservative conditions, such as 7 V at 55°C, both temperature and voltage acceleration factors can be applied to the calculation of estimated failure rate under usage conditions. If an electric-field acceleration factor of 0.06 mV/cm applies,[31] 11 V constitutes an acceleration factor of approximately three orders of magnitude compared to 7 V.

BACKGROUND

CMOS/SOS integrated circuits are produced in a pilot manufacturing line in the Government Systems Division, Solid State Technology Center (SSTC) in Somerville, N.J., and in the Solid State Division production line in Palm Beach Gardens (PBG), Florida. The SSTC pilot line has fabricated, packaged and delivered approximately 20,000 CMOS/SOS integrated circuits per year for the last four years.

Factory production of CMOS/SOS ICs was started in 1977, and production deliveries were made in 1978. By the end of 1983, more than four-million packaged CMOS/SOS integrated circuits had been produced. In 1982, CMOS/SOS microprocessors, A/D flash converters, and radiation-hardened LSI circuits were introduced. In 1983, radiation-hardened 4-kbit RAMs were introduced, and the feasibility of a 16-kbit radiation-hardened RAM was demonstrated.

CMOS/SOS PROCESSES

CMOS/SOS integrated circuits use an all-ion-implanted,[32] self-aligned, silicon-gate process, with n+ polycrystalline silicon gates for both p-channel and n-channel transistors. The basic silicon-gate CMOS/SOS process is shown in Fig. 1. Advanced processes are introduced that reflect current main-stream trends in MOS integrated circuit technology. The CMOS/SOS I silicon-gate process employs wet-chemical etching to pattern 0.6-μm thick heteroepitaxial silicon-on-sapphire islands, 1000-Å gate oxides, and 5-μm feature sizes. The process reduces the tendency for gate-oxide thinning at epitaxial silicon-island edges and, thus, provides high gate-oxide integrity. Passivation is provided by sequential deposition of a 0.2-μm-thick layer of 2% P-PSG, a 0.06-μm-thick layer of high-temperature-deposited silicon nitride (Si_3N_4), and a 6% P-PSG (or BPSG) thermally flowable layer.[33] The present processes thus provide for alkali-ion gettering of SiO_2 regions under the Si_3N_4 layer; the films are a barrier to the ingress of alkali, moisture, or other contaminants into gate-oxide regions.

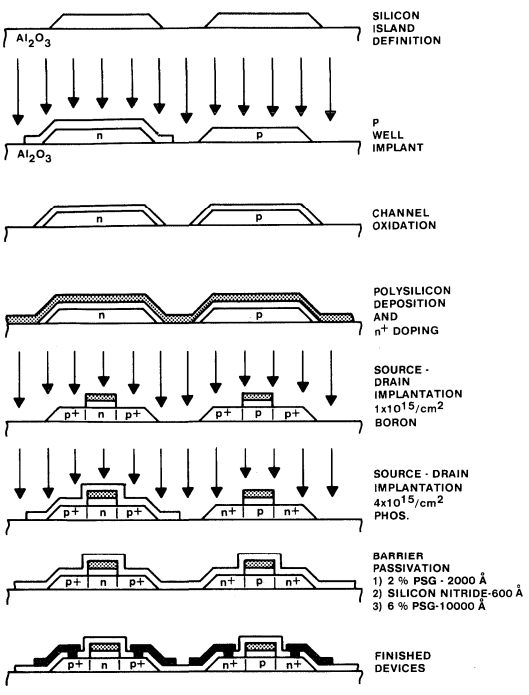

Fig. 1—Self-aligned silicon-gate CMOS/SOS process outline.

CMOS/SOS INTEGRATED-CIRCUIT FAILURE RATES

Much information has already been published on the reliability of various types of CMOS/SOS integrated circuits.[33-47] In this paper, we present recent data on the reliability of CMOS/SOS integrated circuits manufactured by RCA. Available data range from failure rates of plastic-encapsulated, commercial, CMOS/SOS integrated circuits to failure rates of high-reliability, hermetically-sealed ICs and high-performance 1-k and 4-k static RAMs. Data are also available on failure rates of CMOS/SOS RAMs during spacecraft-component burn-in and during in-flight satellite usage. Portions of the data reported have been summarized at recent technical meetings.[48-52]

RELIABILITY OF CMOS/SOS I INTEGRATED CIRCUITS — SSTC PILOT LINE

Data on results of burn-in and static-life tests have been compiled for CMOS/SOS integrated circuits fabricated in the pilot line in SSTC. During the 1982-1983 time period, a total of 2,719 integrated circuits fabricated in SSTC by the CMOS/SOS I process (5-μm feature size, 1000-Å gate oxide) were processed through static burn-in at 125°C and and 10V for 168 hours. Devices were tested at room temperature before the 168-hour static burn-in and then retested at high, low, and room temperature. Of the 2,719 devices tested after burn-in, 55 devices failed at high, low, or room-temperature, for a 98% burn-in yield. (The failed devices include those that did not initially function at high and low temperatures, as well as devices that degraded or became functional failures during the burn-in test.)

Integrated circuits that were screened by the above-described burn-in were subjected to a static-life test at 10 V at 125°C for 1000 hours.[52] Of 385 integrated circuits tested, there were no failures. The calculated failure rate for screened SOS I integrated circuits is 0.24%/1000 hours at 125°C, at a 60% confidence level. The extrapolated failure rate at 55°C (60% confidence level), calculated using a thermal activation energy of 1.0 eV, is 0.0005%/1000 hours (5 FITs).

RELIABILITY OF PLASTIC-ENCAPSULATED CMOS/SOS I INTEGRATED CIRCUITS

CMOS/SOS integrated circuits for commercial applications are usually manufactured in plastic-encapsulated packages. Cost and performance are major considerations, but high reliability is even more important. High reliability is accomplished through in-process controls. Real-time indicators (RTIs) are used to monitor the reliability in high-volume commercial production. Highly accelerated temperature-humidity-bias tests, high-temperature operating life, and in some cases accelerated mechanical tests are used. RTIs are short-duration accelerated-stress tests used to detect specific failure mechanisms that affect product reliability. RTIs monitor the reliability level to see that it meets design specifications; their use also tends to raise the level of reliability. Since they are accelerated tests, they can rapidly show the differences in lot capability and provide processing feedback.

Reliability test data are obtained from the evaulation of standard products and new-design vertification tests. The following reliablity data represent a summary of static bias-life testing in the 1982-1983 time frame.[53] The plastic encapsulated devices include the 128 x 8-bit RAM, the 1-k x 4-bit RAM, a transcoder, and a custom game IC. These devices were tested to data-sheet limits and not subjected to prescreening stress conditions, such as high-temperature-bias aging or high-voltage dynamic testing. Table 1 summarizes the accelerated-stress-test data for these plastic-encapsulated circuits.

Field data from one automotive company using the 1-k CMOS/SOS RAM circuit at the rate of 100,000 devices per year indicated one failure for the past year. With 400 hours operating time per circuit per year, the results are equivalent to 4×10^7 device-hours with one failure, which corresponds to a failure rate of 0.004% per 1000 hours. This field failure rate is consistent with predicted device-failure rates obtained by extrapolation of accelerated life-test data.

RELIABILITY OF CMOS/SOS I: HIGH-REL-PROGRAM GATE ARRAYS AND MEMORIES

CMOS/SOS integrated-circuit reliability data have been compiled during performance of the high-reliability program, which involves fabrication and packaging of gate universal arrays (GUAs) and memory devices by RCA Solid State Division. The program includes four types of 632-gate GUAs and a 1-k RAM; modified Class S screening is used. Burn-in and test includes a 240-hour dynamic burn-in, with functional exercising of devices during burn-in. With a 3% PDA, 92% of the GUA lots passed first burn-in, and 100% of the GUA lots passed with 240-hour re-burn-in. For the four CMOS/SOS types of TA11093 (632-gate GUAs) tested from 1981 until mid 1983, a total of 153 lots was dynamically burned-in at 125°C at 11 V for 240 hours. These lots contained a total of 3,839 devices, which were burned-in for 921,000 device-hours, with 48 parametric/delta post-burn-in failures and two inoperative

Table 1—Static Bias Life-Test Summary (Plastic Package)

Test Conditions	Duration (Hours)	Out of Specification	Comments
Bias Life, 125°C, 7V	1000 2000	1/143 0/20	Leakage @ 168 Hrs.
Bias Life, 150°C, 7V	1000	0/20	
Bias Life, 175°C, 7V	1000	2/13	2 Single-Bit Errors
Total Units Tested	**Total Units Rejected**	**Equivalent Device-Hours @ Temp.**	**Failure Rate† %/1000 Hrs.**
196	3	0.61×10^6 @ 125°C 15.6×10^6 @ 85°C 301×10^6 @ 55°C	0.34 @ 125°C 0.026 @ 85°C 0.0014 @ 55°C

† The failure rate for CMOS/SOS technology has been calculated to a 60% confidence limit, and extrapolated based on a 1.0 eV activation energy. The tests criteria were defined as the data sheet limits.

failures. Of the 153 lots, 13 lots (335 devices) received a second 240-hour burn-in with no failure of any kind (80,400 device-hours)

Systems-level life testing has been performed at 5.5 V for the four gate arrays and one memory device by the user. To date 1,632,000 device hours have been recorded with no rejects.

FAILURE RATES OF SCREENED HIGH-RELIABILITY CMOS/SOS ICs

In this section, screening and accelerated-life-test data are reviewed for several CMOS/SOS ICs, including 1-k RAMs, 4-k RAMs,[54] processors, controllers, and gate universal arrays. All manufactured parts were subjected to visual, mechanical, and electrical screens patterned after MIL-M-38510/50 series CMOS specifications. A simplified device-screening flowchart is shown in Fig. 2.

Table 2 is a life-test summary of screened units stressed at 125°C at 7 volts or greater. A total of 2,045 devices were stressed for over 2.5×10^6 device-hours and tested to data-sheet requirements. Two devices were out of specification for leakage current; there were no functional failures. Using an activation energy of 1.0 eV, this data extrapolates to 2.0 FITs at 5V, 55°C, for the case of the out-of-specification devices, or 0.7 FIT for no functional failures.

In 1978, life-test results of 397 CDP1821 1-k RAMs were reported.[37] The barrier layer used for these RAMs consisted of sequentially-deposited layers of chemical-vapor-deposited SiO_2, Si_3N_4, and 6% P PSG reflow glass.

An additional group of 629 RAMs, fabricated by a modified CMOS/SOS I process, were life tested in 1982. The barrier layer was modified by the addition of 2% P to the CVD-SiO_2 layer.[33]

In 1983, devices of greater complexity, such as 4-k RAMs and processors, were fabricated with the CMOS/SOS II process. This lower-temperature thinner-oxide process is required for the increased performance specified for these parts. The 4-k RAMs are fabricated using a five-transistor memory-cell design and a buried-contact process.[54]

Many MIL specifications require control of the electrical parameters and monitoring of changes in those parameters (Δ). Parameters, such as leakage current and output drive, are checked for changes. Table 3 shows the I_{DD} distribution for a 1-k RAM, 1000-hour life tested at 7 V. The I_{DD} changes were within the error of the measurement. These data are consistent with other parameters measured on many circuits. These parameters are defined in the CMM 5104/IRZ data sheet.[55]

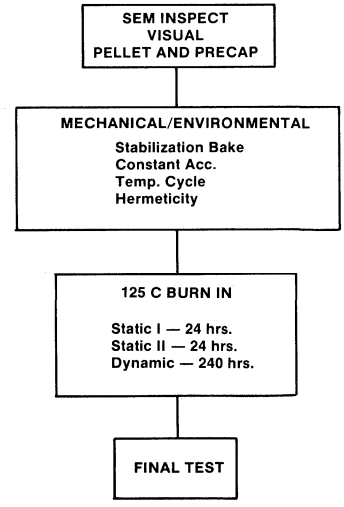

Fig. 2—Simplified device-screening flow chart.

PROCESS MONITORING AND CONTROL

Process reproducibility and control are important requirements for reliable circuits. RCA has instituted process controls for all commercial and high-reliability CMOS/SOS products. These controls exceed the requirements of MIL-STD-883C, a MIL standard establishing the requirements for lot-acceptance testing of microcircuit wafers intended for Class S use. Table 4 lists some process controls that are a standardized part of the PBG production line and the requirements of MIL-STD-883C.

Table 2—CMOS/SOS Life Test Summary for 125°C, $V_{DD} \geq 7$ Volts, Screened Units

Type	SOS Process	Quantity	Device-Hours	Out of Specifications: Leakage	Out of Specifications: Functional
1821, 1k x 1 RAM	CMOS I (1978)	397	752,000	1	0
RAMS, Controller, Arrays	CMOS I (82-83)	385	385,000	0	0
1821, 1k x 1 RAM	CMOS I (1982)	629	706,000	0	0
1821, 1k x 1 RAM	CMOS II (1982)	138	179,000	0	0
6P001 General Processor	CMOS II (1983)	35	105,000	0	0
3P502 Controller	CMOS II (1983)	45	45,000	1	0
632 Gate Universal Array	CMOS II (1983)	25	31,000	0	0
1k x 4 RAM	CMOS II (1983)	122	95,000	0	0
4k x 1 RAM	CMOS II (1983)	269	262,000	0	0
Total CMOS I and CMOS II		2,045	2,560,000	2	0
Failure Rate % per 1000 Hours, 125°C, 7V				0.12	0.035
Rate Extrapolated to 55°C, 5 V (1.0 eV), Failures per 10^9 Hour (FITs)				2.0	0.5

High-temperature/voltage stress of the gate oxide is another tool used to predict threshold stability during bias life. Fig. 3 shows a single inverter circuit that stresses the n and p gate oxide. Fig. 4 shows no threshold shift on the inverter after the gate oxide has been stressed in ceramic packages at 150°C and 7V for 500 hours. These gates were stressed with an acceleration factor of 3×10^3 relative to 55°C usage (based on a 1.0-eV activation energy). Even with this large acceleration factor, there is no measureable sodium contamination.

Table 3—I_{DD} Distribution for 1-k RAM Life Tested at 7 V

	Descriptive Statistics		
	0 Hours	500 Hours	1000 Hours
Number of Devices	77	77	77
Mean (μA)	69.36	66.94	69.40
Std. Dev.	38.98	36.88	37.99
Data Min.	11	10.5	11
Data Max.	191	192	191
Data Range	180	181.5	180
Standard Error of Mean	4.44	4.20	4.33
Maximum Allowable I_{DD} = 260 μA			

In addition to the electrical stability required, Class S requirements include SEM examination of metal step coverage consistent with MIL-STD-883. The required step coverage is achieved by proper circuit design rules and by use of a reflow-glass process that contours all steps and contacts. A 6% P PSG reflow glass, fused at 1,050°C, provides excellent step coverage in CMOS I devices. Where lower reflow temperatures, such as 950°C or 850°C, are required, borophosphosilicate glass (BPSG) provides smooth surface topology.[56] Fig. 5 is an SEM photo of a 4-k RAM's contact metal over a flowed BPSG layer. The BPSG glass provides low-temperature reflow

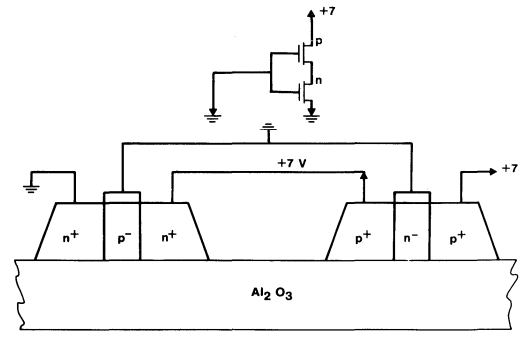

Fig. 3—Inverter bias circuit for accelerated life test.

and, thus, permits excellent step coverage with the high-performance CMOS/SOS II process. All SOS parts consistently meet this MIL-STD SEM requirement.

TIROS SPACECRAFT RELIABILITY DATA

The CMOS/SOS RAMs described in this paper have been used in spaceborne Tiros and Defense Meteorological Satellite memories since 1978. The RAMs operate at 5 V or 10 V with a maximum temperature of 30°C. In addition to in-orbit time, there is extensive testing at spacecraft levels. These data are summarized in Table 5. As of March 16, 1984, RAMs had operated more than 45-million hours with no failures.[57] Three soft errors were observed during a period of extensive solar-flare activity. This low failure rate is consistent with the inherent CMOS/SOS cosmic ray sensitivity of $<10^{-9}$ errors/bit/day.

Table 4—CMOS/SOS Process Inspection and Controls

Process	Controlled Parameters	MIL Standards 976 and 883C Requirements
Epitaxial Wafer	Crystallinity; Thickness; Flatness	NHB-5300
Photomasks	Laser inspection after specified usage	Defect level defined
Thermal Oxide	Thickness; CV shift ($V_T \leq 0.4$ V for 1000Å SiO_2)	
Polysilicon	Thickness, Grain Size	
Polysilicon Conductivity	4-Point probe	
Ion Implant	Energy; Conductance of control chip	Controls and documentation required
Reflow Glass	Thickness; EDAX composition; Flow characteristics; SEM	Controls and documentation required
Al Metallization	Thickness (>8000Å, ± 20% of design nominal, 6000 Å min); CVBT shift (evaluate sodium concentration); Metal purity	
Passivation Overcoat	Thickness; Composition	
Electrical Wafer Acceptance Test on SOS Test Key	N and P threshold voltage; Source—drain breakdown voltage; transistor gain; Device leakage current; Contact resistance to Si islands and to polysilicon	MIL Std 976
Thermal Stability	Controls at metal evaporation and oxide growth ($\Delta V_T \leq 0.4$ V normalized for 1000 Å oxide)	
SEM	All lots for military applications	Method 2018 required for class S only
Product Assurance	Quality control organization; Calibration; Process documentation	MIL-Std-Cp 45662

ACCELERATED STRESS TESTING OF ADVANCED CMOS/SOS PROCESSES (SOS III)

In parallel with the development of CMOS/SOS processes capable of fabricating VLSI arrays with increasingly finer geometries, the reliability of arrays produced with these advanced processes is constantly monitored. Since 1981, a continuing study of the reliability of advanced short-channel CMOS/SOS arrays has been carried out.

Throughout 1982, the reliability studies were concerned with arrays produced by the SOS III process.[52] This process uses 500 Å of gate oxide, a 3μm n + polysilicon gate, negative photoresist, arsenic and boron source-drain implants, and a triple layer of chemical-vapor-deposited dielectric consisting of 2% PSG/Si_3N_4/6% PSG.

An arithmetic logic unit (ALU) containing approximately 1,300 transistors was the test vehicle used in the reliability studies. These arrays were fabricated, packaged, data logged, and stress tested. Throughout 1982, static-bias accelerated stress tests were performed at 175°C and at 250°C with 6-volt bias on 52 ALU's representing three lots. The medium time to failure for each sample was 2,600 hours and 170 hours, respectively. All the devices in these tests remained fully functional; the out-of-specification arrays exceeded an arbitrary limit of $I_{DD} = 100\ \mu A$.

An additional thirty-two ALUs were subjected to an accelerated stress test at 250°C and 6 V with the input terminals dynamically exercised. Several devices experienced increases in leakage current within the first twenty-four hours; however, there were no additional increases in leakage current, and all devices were functional when the test was terminated at 456 hours. A comparison of this result with those of the 175°C and 250°C static-bias tests shows that this result is consistent with a mobile alkali-ion drift, the most common MOS device failure mode. This observation, together with analysis performed on some of the devices that displayed increased leakage currents after accelerated life tests, confirm these mechanisms.

ALUs that were fabricated during the first quarter of 1983 with the SOS III process are being subjected to static-bias accelerated stress tests at 200°C and at 225°C with 6-V bias. Seventy-three arrays are currently on test. To date, the baseline devices at 225°C have accumulated 6,900 hours, with seven devices exceeding the leakage-current limit; the devices at 200°C have accumulated 5,500 hours, with 15 out-of-specification. Ten of these occurred early in the test (within the first 144 hours) and would have been screened out with a standard burn-in. Of these, three were nonfunctional, six were the result of increases in leakage current without loss of functionality, and one was the result of electrostatically induced damage attributed to mishandling. The remaining arrays categorized as out-of-specification suffered from increases in power-supply leakage current after they had been on test in excess of 2,000 hours.

The results of these accelerated stress tests are summarized in Table 6. Extended stress test times are required to produce approximately 75% failures in each test sample. The device hours accumulated by in-specification devices are extrapolated to the operating temperatures of 55°C, 85°C, and 125°C using an activation energy of 1.0 eV. The predicted failure rate at 55°C of 1.5 FITs is consistent with the CMOS/SOS database.

The technique of characterizing the reliability of a process by static-bias accelerated stress tests is being employed to demonstrate the viability of any new CMOS/SOS process. Now that the reliability baseline is established, this technique evaluates process variations by comparing the predicted reliability of the variant with that of the baselined process. A quick and accurate appraisal of a process variant is now possible for processes such as low-temperature LPCVD polysilicon gates,[58] reactive ion etching, or double-level metal.

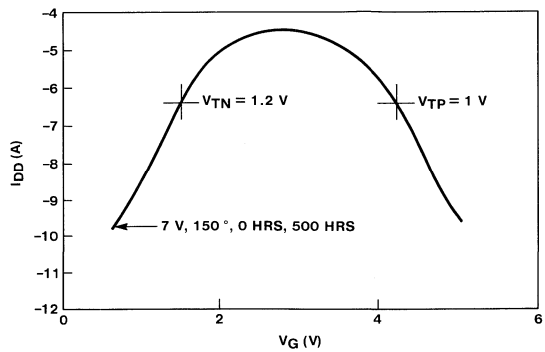

Fig. 4—Data from inverter bias circuit showing threshold stability after stress at 150°C at 7 V for 500 hours.

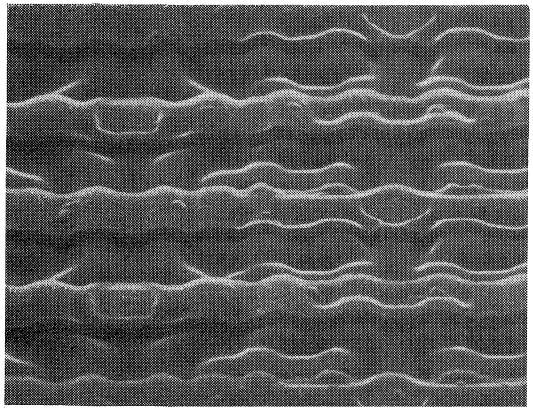

Fig. 5—SEM showing contact metal over a flowed BPSG layer for 4-k RAM (original magnification 2000 x, 55°).

DISCUSSION

Accumulated data show that the process sequence and controls used for CMOS/SOS circuit fabrication in both RCA's Palm Beach Gardens, FL, and Somerville, NJ facilities produce devices that meet all commercial and military requirements for stability and reliability.

The most common failure mechanisms for all types of silicon-gate MOS integrated circuits are alkali-ion migration effects and time-dependent breakdown of thermally grown oxides. The predominant failure mechanism of CMOS/SOS integrated circuits during high-temperature bias-life testing has been parametric, an increase in I_{DD} leakage, rather than functional, or catastrophic, failure. This type of failure is believed to be due to the motion of sodium ions in SiO_2 in an electric field and is characterized by an activation energy on the order of a 1.0 eV.

In predicting IC reliability in accordance with MIL-HDBK-217 D[59] and Notice 1,[60] a learning factor (π_L) of 10 is used for new technologies. A π_L of 1.0 is used when production conditions and controls have stabilized (after 4 to 6 months of continuous production). CMOS/SOS has been in production since 1978. The current RCA low-temperature CMOS/SOS wafer-fabrication process has been in production since August 1982; accordingly, a π_L of 1.0 is considered appropriate for use in the prediction of reliability of all RCA CMOS/SOS integrated circuits.

Table 5—DMSP and TIROS Meteorological Satellite, Spacecraft On-Orbit and Spacecraft Level Stress Testing (CDP 1821 1-k SOS RAM Survival Data)

Spacecraft	Launch Date	Days as of 3/16/84	Hours as of 3/16/84	1-k RAM Qty/SC	Part-Hours
DMSP 5D-2 S6*	12/20/82	452	10,848	952	10,327,296
DMSP 5D-2 S7	11/17/83	120	2,880	952	2,741,760
TIROS-N	10/13/78	464	11,136	306	3,407,616
TIROS NOAA-E	3/28/83	354	8,496	680	5,777,280

Spacecraft Level Testing = 22,794,960 Part-Hours
Total Part-Hours = 45,048,912, No Device Failures

* S6 exhibited three occurrences of parity errors between 21 and 58 days of operation. Source/location of errors could not be determined. Failures were not "hard".

A comparison of the observed failure rates of CMOS/SOS integrated circuits with data on failure rates of MOS integrated circuits based on bulk-silicon substrates[36,41,42,45,61–70] indicates that CMOS/SOS integrated-circuit reliability is comparable to that of devices fabricated by bulk-MOS technologies (CMOS, NMOS, PMOS).

Table 6—CMOS/SOS Static Bias Accelerated Stress Test

Test Conditions	Duration (hours)	Out of Specifications	Comments
175°C, 6V	6500	25/31	I_{DD} in excess of 100 μA. Devices are functional at final test point.
250°C, 6V	240	15/19	I_{DD} in excess of 100 μA. Devices are functional at final test point.
225°C, 6V	6900	7/22	I_{DD} in excess of 100 μA. Devices functional at 4882-hour interim test, continuing on test.
200°C, 6V	5564	15/75	I_{DD} in excess of 100 μA. All but 3 devices functional, remainder continuing on test.

Total Units Tested	Out of Spec. Devices	Equivalent Device-Hrs	Failure Rate* in FITs
147	62	86.1×10^6 (125°C)	740
		2.3×10^9 (85°C)	28.6
		43.0×10^9 (55°C)	1.5

*Failure rates for the CMOS/SOS III technology have been calculated using a 60% confidence level and extrapolated based on 1.0 eV activation energy. All devices were processed and packaged at SSTC, using commercial assembly (no screening) and hermetic ceramic packages.

CONCLUSIONS

CMOS/SOS integrated circuits have been in volume production for more than five years. Initial devices were based on 5-μm feature sizes and 1000-Å gate oxide. Newer devices have evolved to smaller feature sizes and have used thinner gate oxides and lower processing temperatures to achieve performance advantages. The failure rate at 125°C, 7V, is 0.1/1000 hours for screened parts; this number extrapolates to a failure rate for CMOS/SOS integrated circuits of one FIT at 55°C at 5 volts, to a 60% confidence level. Accelerated stress analysis of new high-performance circuits demonstrates a capability comparable to the production circuits. Analysis of failed devices from screened and plastic-encapsulated circuits indicate no new failure mechanisms attributed to the silicon-on-sapphire technology.

Analysis of field data in device applications, such as automotive and space, demonstrates low failure rates consistent with those predicted by the accelerated stress techniques reviewed in this paper.

Both the CMOS/SOS technology and the bulk-CMOS technology are evolving as design and wafer-processing trends are applied to achieve improved circuit performance and higher density. The advantages of the CMOS/SOS technology relative to the bulk-CMOS technology continue to be applicable as transistors in ICs are scaled to submicron dimensions.[71] Accordingly, it is predicted that the use of CMOS/SOS technology will continue to increase, particularly in those advanced applications in which designability, speed, density, and dielectric isolation are important.

ACKNOWLEDGMENT

The authors gratefully acknowledge the contributions of D.R. Carley, who directed most of this effort, J. Hale for the data on plastic-encapsulated CMOS/SOS, and R. Nearhoof for the High-Rel Program results.

REFERENCES:

[1] F. B. Micheletti et al., Special Issue on SOS Technology, *IEEE Trans. Electron Devices,* **ED-25,** No. 8, p. 857 (Aug. 1978).

[2] G. W. Cullen and C.C. Wang, editors, *Heteroepitaxial Semiconductors For Electronic Devices,* Springer-Verlag, New York, 1978.

[3] Y. Nishi and H. Hara, "(Invited) Physics and Device Technology of Silicon on Sapphire," *Japan J. Appl. Phys.,* **17,** Suppl. 17-1, p. 27 (1978).

[4] E. Preuss and H. Schlotterer, "Silicon-on-Sapphire Devices: Realization, Properties and Applications," pp. 7-31 in *Solid State Devices,* 1977, Inst. Phys. Conf. Ser. No. 40, Bristol and London, 1978.

[5] Y. Nishi, "Comparison of New Technologies for VLSI: Possibilities and Limitations," *Microelectronics J.,* **12,** No. 6, 5-14 (Nov.-/Dec. 1981).

[6] A. C. Ipri, "The Properties of Silicon-on-Sapphire Substrates, Devices and Integrated Circuits," pp. 253-395 in *Applied Solid State Science,* Supplement 2A, edited by D. Kahng, Academic Press, New York, 1981.

[7] Y. Okuto, Y. Ohno, H. Mizumura, and M Fukuma, "SOS/CMOS Feasability Study for Future LSI Applications," pp. 296-307 in *Semiconductor Technologies — 1982,* edited by J. Nishizawa, Ohmsha Ltd., Tokyo and North-Holland Publishing Co., Amsterdam, 1981.

[8] D. V. Pattanayak, J. G. Poksheva, R. W. Downing and L. A. Akers, "Fringing Field Effect in MOS Devices," *IEEE Trans. Comp Hybr. Mfg. Technol.,* **CHMT-5,** p. 127 (March 1982).

[9] M. H. White, "Characterization of CMOS Devices for VLSI," *IEEE Trans. Electron Devices,* **ED-29,** p. 578 (April 1982).

[10] H.-T. Yuan, Y.-T. Lin and S.-Y. Chiang, "Properties of Interconnection on Silicon, Sapphire, and Semi-Insulating Gallium Arsenide Substrates," *IEEE Trans. Electron Devices,* **ED-29,** p. 639 (April 1982).

[11] D. J. McGreivy and K. A. Pickar, *VLSI Techologies through the 80s and Beyond,* IEEE Computer Society Press, Silver Spring, MD, 1982.

[12] A. Gupta and P. K. Vasudev, "Recent Advances in Hetero-Epitaxial Silicon-on-Insulator Technology, Part I," *Solid State Technology,* **26,** No. 2, p. 104 (Feb. 1983).

[13] A. Gupta and P. K. Vasudev, "Recent Advances in Hetero-Epitaxial Silicon-on-Insulator Technology, Part II," *Solid State Technology,* **26,** No. 6, p. 129 (June 1983).

[14] L. Jastrzebski and A. G. Kokkas, "SOI by CVD: An Overview," paper presented at the Annual Meeting of the Materials Research Society, Boston, MA. Nov. 15, 1983.

[15] G. W. Cullen, M. T. Duffy and R. K. Smeltzer, "Recent Advances in the Heteroepitaxial Silicon-on-Sapphire Technology," paper prepared for presentation at the Spring Meeting of the Electrochemical Society, Cincinnati, OH, May 10, 1984 (Abstr. No. 57).

[16] K. M. Schlesier, "Radiation Hardening of CMOS/SOS Integrated Circuits," *IEEE Trans. Nucl. Sci.,* **NS-21,** No. 6 p. 152 (Dec. 1974).

[17] K. G. Aubuchon and E. Harari, "Radiation Hardened CMOS/SOS," *IEEE Trans. Nucl. Sci.,* **NS-22,** p. 2181 (Dec.1975).

[18] J. C. Peel, R. K. Pancholy, G. J. Kuhlmann, T. J. Oki and R. A. Williams, "Investigation of Radiation Effects and Hardening Procedures for CMOS/SOS," *IEEE Trans. Nucl. Sci.,* **NS-22,** p. 2185 (Dec. 1975).

[19] G. W. Hughes and G. J. Brucker, "Radiation Hardened MOS Technology," *Solid State Technology,* **22,** No. 7, p. 70 (July 1979).

[20] A. Gupta, M. F. Li, K. K. Yu, S. C. Su, P. Pandya and H. B. Yang, "Radiation-Hard 16K CMOS/SOS Clocked Static RAM," *IEDM Tech. Digest,* p. 616 (Dec. 1981).

[21] G. J. Brucker, "Exposure-Dose-Rate-Dependence for a CMOS/SOS Memory," *IEEE Trans. Nucl. Sci.,* **NS-28,** No. 6, p. 4056 (Dec. 1981).

[22] D. M. Long, "Radiation Hardness of New Technologies: State of the Art Review," *GOMAC Digest,* p. 314 (Nov. 1982).

[23] H. Hatano and M. Shibuya, "CMOS Logic Circuit Optimum Design for Radiation Tolerance," *Electronics Letters,* **19,** No. 23, p. 977 Nov. 10, 1983.

[24] J. L. Yeh and R. K. Smeltzer, "A High Density, High Yield, Radiation Hardened, Buried Contact CMOS/SOS Technology," presented as a poster paper at IEEE Annual Conf. on Nuclear and Space Radiation Effects, Las Vegas, NV. July 1982.

[25] L. Napoli, R. Smeltzer, J. Yeh and W. Heagerty, "A 200 KRad (Si) 150 nsec 5 Volt CMOS/SOS 4K RAM," paper presented at IEEE Annual Conf. on Nuclear and Space Radiation Effects, Las Vegas, NV, July 1982.

[26] L. S. Napoli, R. K. Smeltzer, J. L. Yeh, and W. F. Heagerty, "CMOS/SOS 4K RAMs Hardened to 100 KRads (Si)", *IEEE Trans. Nucl. Sci.,* **NS-29,** p. 1707 (Dec. 1982).

[27] G. J. Brucker, G. T. Caracciolo, W. F. Gehweiler and W. F. Heagerty, "Design and Performance of Two 1K CMOS/SOS Hardened RAMs," *IEEE Trans. Nucl. Sci.,* **NS-20,** p. 1920 (June 1983).

[28] J. Handen and H. Veloric, "Radiation-Hardened CMOS/SOS Chips Ideal for Space," *Defense Electronics,* **15,** No. 9 p. 86 (Sept. 1983).

[29] R. Berger, A. Shevchenko, G. J. Brucker, R. Kennerud, P. Measel and K. Wahlin, "Transient and Total Dose Radiation Properties of the CMOS/SOS EPIC Chip Set," *IEEE Trans. Nucl. Sci.,* **NS-30,** p. 4256 (Dec. 1983).

[30] I. Wacyk, L. S. Napoli, H. Veloric, W. Morris and J. Pridmore, "A 16K CMOS/SOS RAM Hardened to the Megarad Level," paper to be presented at the 1984 Nuclear Science and Radiation Effects Conference (to be held in Colorado Springs, CO, July 1984).

[31] D. L. Crook, "Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown," *17th Ann. Proc. Reliab. Phys.,* p. 1 (1979).

[32] D. S. Woo, "All-Ion-Implantation Process for Production of Integrated Circuits," *Insulation/Circuits,* **26,** No. 1, p. 39 (Jan. 1980).

[33] H. Veloric M. Feyerherm, K. K. Oey, R. R. Denning, G. Schnable and R. Smeltzer, "Reliability of Radiation-Hardened CMOS/SOS RAMs in Spacecraft Memory Subsystems," 1983 Space Electronics Conference Abstracts of Presentations, p. 51 (Electronic Industries Association, Jan. 1983).

[34] G. Caswell and S. Cohen, "A Reliability Study of CMOS/SOS Technology," *GOMAC '76 Proceedings,* p. 84 (Nov. 1976).

[35] J. S. Smith and D. D. Talada, "A CMOS/SOS Reliability Study," *14th Ann. Proc. Reliab. Phys.,* pp. 23-32 (1976).

[36] G. L. Schnable, L. J. Gallace and H. L. Pujol, "Reliability of CMOS Integrated Circuits," *Computer,* **11,** No. 10, p. 6 (Oct. 1978).

[37] E. M. Reiss and O. Shevchenko, "A High-Reliability 1K CMOS/SOS RAM," *GOMAC-78 Digest,* p. 122 (Nov. 1978).

[38] G. M. Johnson, "Reliability Investigations of Advanced Semiconductor Devices," *Solid State Technology,* **22,** No. 9, p. 95 (Sept.1979).

[39] J. Hilibrand and K. R. Anderson, "High Reliability Through Chip Complexity," *RCA Engineer,* **25,** No. 4, p. 22 (Dec. 1979/Jan. 1980).

[40] L. J. Gallace, "Predicting Solid-State Device Reliability," *RCA Engineer,* **25,** No. 4, p. 19 (Dec. 1979/Jan. 1980).

[41] L. J. Gallace, "Reliability of Plastic-Packaged CMOS Devices," *Solid State Technology,* **23,** No. 9, p. 102 (Sept. 1980).

[42] G. L. Schnable and R. B. Comizzoli, "CMOS Integrated Circuits Reliability," *Microelectron. Reliab.,* **21,** No. 1, p. 33 (1981).

[43] M. K. Ghazi, J. R. Hall and A. Y. Yahiku, "Accelerated Life Testing Effects on CMOS/SOS LSI Devices," FR-81-92-851, Final Report by Hughes Aircraft Co., Culver City, CA, on Sandia Laboratories Contract No. 28-1448, June 1981.

[44] L. J. Gallace, L. H. Gibbons and S. Gottesfeld, "Reliability Requirements of Integrated Circuits in the Automotive Environment," *Electrochem. Soc. Extended Abstracts,* **82-2,** p. 355 (Oct. 1982).

[45] R. Denning, L. Gibbons and E. Sherman, "RCA Solid State Division—IC Quality and Reliability Seminar," European Presentation, Feb. 1983..

[46] RCA Quality and Reliability," RCA Solid State, Somerville, NJ (received May, 1983).

[47] RCA, "High Reliability Radiation Hardened Solid State Devices," HR-10-3, RCA Solid State Division, Somerville, NJ (1983).

[48] H. Veloric, R. Denning, G. Schnable and J. Yeh, "Reliability of

Silicon-on-Sapphire Integrated Circuits," paper presented at the IEEE SOS/SOI Technology Workshop, Provincetown, MA, Oct. 5, 1982 (Paper No. 1.3).

[49] H. Veloric, R. Denning, G. Schnable, M. Feyerherm and J. Yeh, "Reliability of Radiation-Hardened CMOS/SOS RAMs for Spacecraft Memory Application," paper presented at GOMAC-82 (Government Microcircuit Applications Conference), Orlando, FL, Nov. 4, 1982 (Paper No. 16.7).

[50] H. Veloric M. Feyerherm, K.K. Oey, R. Denning, G. Schnable and R. Smeltzer, "Reliability of Radiation-Hardened CMOS/SOS RAMs in Spacecraft Memory Subsystems," paper presented at the 1983 Space Electronics Conference, Los Angeles, CA, Jan. 27, 1983.

[51] H. Veloric and W. Morris, "Rad Hard CMOS/SOS: An Ideal Technology for the Space Environment," invited paper presented at the 1983 IEEE SOS/SOI Technology Workshop, Jackson Hole, WY, Oct. 6, 1983 (Paper No. 4.1).

[52] M. P. Dugan, C. Benyon and G. L. Schnable, "Reliability Characterization of RCA SOS III Process," paper presented at the IEEE SOS/SOI Technology Workshop, Jackson Hole, WY, Oct. 6, 1983 (Paper No. 4.4).

[53] J. Hale, private communication, Jan. 1984.

[54] A. G. F. Dingwall, R. G. Stewart, B. C. Leung and R. E. Stricker, "High-Density, Buried-Contact CMOS/SOS Static RAM's" *IEDM Digest,* p. 193 (Dec. 1978).

[55] CMM 5104/IRZ data sheet, RCA Solid State Division, Somerville, NJ, 1983.

[56] W. Kern and G. L. Schnable, "Chemically Vapor-Deposited Borophosphosilicate Glasses for Silicon Device Applications," *RCA Review,* **43,** No., 3 p. 423 (Sept. 1982).

[57] M. P. Feyerherm, private communication, March, 1984.

[58] G. Harbeke, L. Krausbauer, E. F. Steigmeier, A. E. Widmer, H. F. Kappert and G. Neugebauer, "Growth and Physical Properties of LPCVD Polycrystalline Silicon Films," *J. Electrochem. Soc.,* **131,** p. 675 (March 1984).

[59] *Reliability Prediction of Electronic Equipment,* MIL-HDBK-217D, Department of Defense, Jan. 15, 1982.

[60] *Reliability Prediction of Electronic Equipment,* MIL-HDBK-217D, Notice 1, Table 5.1.2.5-2, π_L, Learning Factors, Department of Defense, June 13, 1983.

[61] RAC, "Microcircuit Device Reliability—Digital Failure Rate Data, 1981," MDR-17, Reliability Analysis Center, Rome Air Development Center, Griffiss Air Force Base, NY 13441 (Summer 1981).

[62] Motorola, Inc., "Reliability Report—CMOS Standard Logic Reliability—1981," Motorola Semiconductor Products, Inc., MOS Integrated Circuits Group, Austin, TX.

[63] RAC, "Microelectronic Device Reliability—Memory/Digital LSI Data," MDR-18, Reliability Analysis Center, Rome Air Development Center, Griffiss Air Force Base, NY 13441 (Winter, 1981/1982).

[64] "Motorola Reliability Report 8202—High-Speed CMOS Logic Family," Motorola, Inc., MOS Integrated Circuits Group, Motorola Semiconductor Products, Inc., Austin, TX, Jan. 1982.

[65] Intel Corp., "Intel's Reliability Monitor Program Provides Vital Information to Customers," *Solutions,* 3-5 (March/April 1982).

[66] Technical Staff, Military/Aerospace Products Division, National Semiconductor Corp., *The Reliability Handbook,* Vol. 1, Second Edition, National Semiconductor Corp., Santa Clara, CA, April 1982.

[67] D. Tovar, "Reliability of High Speed CMOS Logic," National Semiconductor Reliability Report No. PR-11, National Semiconductor Corp., Santa Clara, CA (1982).

[68] D. F. Simonaitis, "IC Failure Rate Estimates from Field Data," *Proc. 33rd Electronic Comp. Conf.,* pp. 368-373 (May 1983).

[69] RCA QMOS Reliability, QRB-510, RCA Solid State, Somerville, NJ, Sept.1983.

[70] S. Gottesfeld and L. Gibbons, "Reliability Characterization of High-Speed CMOS Logic ICs," *RCA Rev.,* **45,** p. 179, June 1984.

[71] J. Hilibrand, private communication, Jan. 1984.

Power Consumption in QMOS Logic Circuits

by R. Funk and B. Heinze

QMOS, RCA's high-speed CMOS-logic technology, offers users the best features of both CMOS and TTL technologies: the low-power consumption of CMOS and the fast speeds associated with LSTTL. This Application Note focuses on the primary QMOS feature, low power consumption. The causes of quiescent and dynamic power dissipation in HC and HCT QMOS devices are discussed. The formulas needed to compute the power dissipation in QMOS devices are presented along with sample calculations. A comparison is made of QMOS, LS, and ALS logic types relative to power dissipation.

The significant reduction in power consumption provided by a QMOS logic system compared with the equivalent LSTTL or ALSTTL counterpart design is *the* primary reason that QMOS is destined to be chosen for new designs and to replace LSTTL or ALSTTL parts in many existing designs. The replacement of LSTTL devices with HCT QMOS types[1] achieves power savings in existing designs where decreased power consumption and dissipation are a distinct advantage. In new designs, only QMOS logic lends itself to battery-operated portable equipment, such as portable (lap-held) personal computers, and the switch to QMOS is the major trend in PCs using all-CMOS RAMs, ROMs, and peripherals. All-QMOS designs can be powered down to 2-volts standby, increasing battery life. In nonportable designs, QMOS and CMOS LSI logic are also preferred to significantly reduce, in order of priority, cost, size, and weight. Cost reduction is the result of savings in the cost of supply regulators, the elimination of cooling fans and heat sinks, etc.

An equally powerful motivating force behind the use of logic components that dissipate lower power, such as QMOS, is the proven component and equipment reliability enhancement. The junction temperature of the ICs, as well as the temperature of other equipment components (resistors and capacitors), is much reduced, thereby lengthening life. QMOS failure rates are currently measured at .0015%/1000 hours at 60% UCL for operation at +55° C.

Power consumption in a logic IC must be considered in both of the IC's operating modes, i.e., under static and dynamic conditions. QMOS devices consume only minute amounts of power under static (quiescent) conditions, making power consumed in the dynamic state the major contributor to total power consumption. TTL devices, on the other hand, consume significant amounts of power in the quiescent state, so much in fact, that power consumption in the dynamic state can be masked at frequencies as high as 20 MHz, depending on device complexity. At higher frequencies, the power consumed by TTL devices increases proportionately. Since integrated circuits typically spend a significant percentage of their time either in the quiescent state or operating at average frequencies below 2 MHz, QMOS devices can provide significant and often dramatic power savings.

QUIESCENT POWER CONSUMPTION

The quiescent power consumption of a logic IC is measured when the system input voltage, V_{IN}, equals the device supply voltage, V_{CC}, or is at ground potential. Fig. 1(a) is used to illustrate this discussion. In the quiescent state, either the PMOS or NMOS transistor is fully off, and ideally no direct MOS transistor-channel path exists between V_{CC} and ground. In reality, however, thermally generated minority-charge carriers present in all reverse-biased diode junctions, Fig. 1(b), allow a very small power-supply leakage current to flow between V_{CC} and ground. In QMOS data sheets, this quiescent leakage current is specified as I_{CC}.

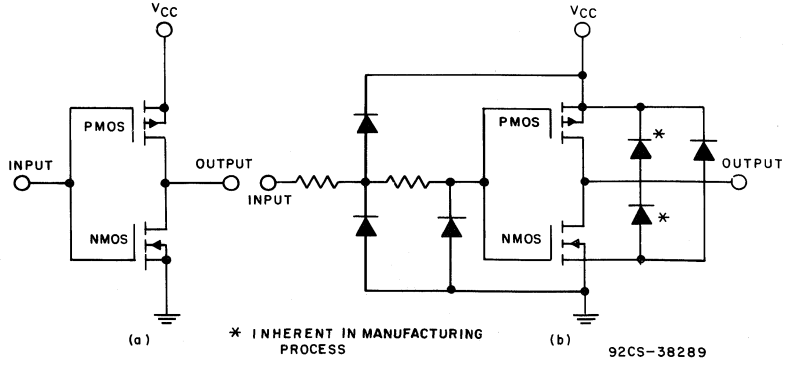

Fig. 1 - (a) Simple QMOS inverter circuit, (b) simple QMOS inverter circuit with input and output ESD protective diodes.

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Three factors affect the value of I_{CC} and, therefore, the power dissipation of a device:

Temperature:-Increasing temperature causes an increase in I_{CC} because the minority charge carriers in the reverse-biased diode junctions of QMOS devices are thermally generated.

Device Complexity:-MSI devices will consume more power than SSI devices because there exists a proportionally greater reverse-biased diode-junction area.

V_{CC}:-The minority-charge carriers are linearly related to reverse junction voltage.

Table I shows the JEDEC industry standards for 54/74 HC/HCT high-speed CMOS devices, and illustrates the effect of temperature and device complexity on I_{CC} at the maximum recommended HC operating voltage, V_{CC} = 6 V. At V_{CC} = 2 V, I_{CC} is approximately 1/3 the value shown at V_{CC} = 6 V. Typical I_{CC} values are well under the maximum specified values.

Another factor that may add to quiescent, or dc, power consumption is the through current caused by both the PMOS and NMOS transistors of the input stage, Fig. 1(a), being on, at least to some degree, at the same time. For HC devices,[1] where the switching transition occurs at a nominal $V_{CC}/2$ (see Fig. 2(a)), there is no through current and, hence, no added dc power consumption. That is, with V_{IL} and V_{IH} voltage levels (low-level and high-level input voltages, respectively) at the inputs, either the PMOS or the NMOS transistor of the HC input stage is completely off. However, for HCT devices, where the switching transition occurs at a nominal 1.3 volts, Fig. 2(b), there is a through-current component when an input high-voltage level of under 4 volts is applied to an input. With this amount of voltage applied, the NMOS transistor is fully on and the PMOS transistor not fully off. This is the situation in an HCT device when, in a QMOS/TTL interface, the input voltage of the QMOS device is the V_{OH} (high-level output voltage) of a TTL family device. The 3.5-volt typical V_{OH} output voltage will fully turn-on the QMOS input NMOS transistor (Fig. 1) but not fully turn-off the PMOS transistor. The current flow that results is specified as ΔI_{CC} in QMOS HCT data sheets.

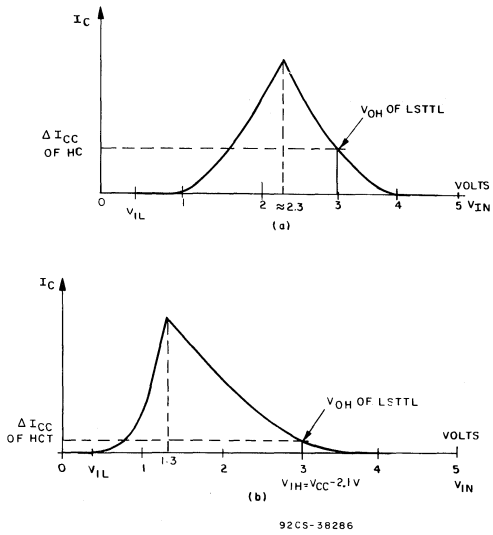

Fig. 2 - (a) HC input, CMOS interface, (b) HCT input, TTL interface.

Computing HC Quiescent-Power Consumption

Quiescent power consumption in an HC device is extremely low, typically under 10 microwatts. The ΔI_{CC} plays no part because HC I/O levels are completely compatible: V_{OL} and V_{OH} worst-case specifications are 0.1 and V_{CC} - 0.1 volt, very close to ground and V_{CC}, respectively. Fig. 2(a) illustrates that no I_{CC} will flow with these V_{OL} and V_{OH} voltage levels imposed. However, if inputs are driven beyond V_{IL} and V_{IH} toward the switching voltage (centered typically at 2.3 volts), appreciable I_{CC} will flow. Such a high-current situation exists when an attempt is made to drive an HC input with a TTL output. For example, with a TTL V_{OH} level of 3 volts driving an HC input, not only would a logic error exist, but several milliamperes of I_{CC} would flow. To overcome this problem, an external pull-up resistor could be used, as shown in Fig. 3, but the resistor would cause significant additional system power consumption because it would have to be kept small in value in order to keep system speed high. RCA HCT QMOS devices are the preferred solution when interfacing CMOS with TTL logic.

In power-critical applications, such as portable battery-operated equipment or equipment operating in a battery-powered stand-by mode, HC quiescent power consumption may be a significant component of battery drain. The following formula is used to compute HC quiescent power consumption:

$$P_{dc} = V_{CC} I_{CC} \qquad (1)$$

where V_{CC} is dependent upon the particular application, and I_{CC} is obtained from the data sheet of the particular device for a V_{CC} of 6 volts (HC types). The data sheet value given is also valid within the nominal 5 V ± 10% supply-voltage range of HCT types. The value of I_{CC} at V_{CC} = 6 V can be linearly reduced for any desired V_{CC} voltage; e.g., at V_{CC} = 2 V, use 1/3 of the limits shown in Table I.

Table I - 54/74HC Family Characteristics

Symbol	Parameter	V_{CC} (V)	Temperature (°C) 54HC/74HC 25 Min.	54HC/74HC 25 Max.	74HC -40 to 85 Min.	74HC -40 to 85 Max.	54HC -55 to 125 Min.	54HC -55 to 125 Max.	Units	Test Conditions
I_{CC}	Quiescent Supply Current									
	SSI	6	—	2	—	20	—	40	μA	V_I = V_{CC} or GND
	FF	6	—	4	—	40	—	80	μA	I_O = 0
	MSI	6	—	8	—	80	—	160	μA	

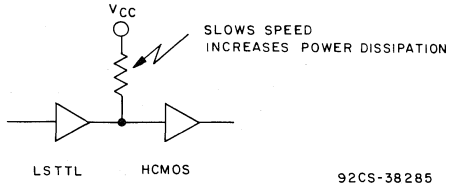

Fig. 3 - Use of pull-up resistor in LSTTL/HC interface.

Computing HCT Quiescent Power Consumption

Because HCT devices can be substituted for LSTTL devices and/or mixed with LS, ALS, AS, or FAST-TTL-family ICs in a system, their consumption of larger amounts of dc power than HC types is not significant. TTL worst-case output voltages are: V_{OL} = 0.4 V(max) and $V_{OH} = V_{CC} - 2.1$ V(min). The V_{OH} (or logic 1) voltages result in the ΔI_{CC} current flow illustrated in Fig. 2(b) and already described above. Note that only a logic-1 input causes appreciable quiescent leakage-current flow; a logic-0 input (0.4 V(max)) is close enough to ground to turn the NMOS transistor fully off. The total HCT-device quiescent power consumption is a function of the number of logic-1 inputs applied at the V_{IH} voltage level.

QMOS HCT data sheets specify ΔI_{CC} at the worst-case input voltage of $V_{CC} - 2.1$ V for V_{CC} ranging from 4.5 volts to 5.5 volts, with normalized limits as shown in Table II. ΔI_{CC} is further specified on a per-input-pin basis. This method of specification allows more accurate calculations if all the functions within a device are not being used or are being used at different input levels. For example, assume that two gates of an HCT10, a triple 3-input NAND Gate, are being driven by a TTL device with a 50% duty cycle. Given the information in Table II, quiescent power dissipation is calculated as follows:

$$P_{dc} = V_{CC}I_{CC} + V_{CC}\Delta I_{CC}(\text{percent duty cycle high}) \quad (2)$$

where ΔI_{CC} is calculated on a unit-load basis as follows:

$$I_{CC} = (360\ \mu A/\text{unit load}) \times (0.6\ \text{unit loads/input pin}) \times (6\ \text{input pins}) \quad (3)$$
$$= 1.3\ \text{mA}$$

Therefore:

$$P_{dc} = (5\ V)(2\ \mu A) + (1.3\ mA) \cong 6.5\ mW$$

Note that if all of the inputs of an HCT device are driven by HC or equivalent CMOS output levels, only equation (1) need be used to calculate its static power dissipation. Note also that if a 50% duty cycle is assumed for input signals, the average dc power is 3.25 milliwatts for the HCT type. This figure compares with 35 milliwatts for a 74LS10 IC, and shows that the HCT device still provides a big savings in power, even in the worst-case application.

DYNAMIC POWER CONSUMPTION

Three factors affect QMOS dynamic power consumption:

Load capacitance - dissipation of output state, Fig. 4.
Internal circuit capacitance
Switching transition currents (when complementary transistors used in switching are both momentarily on)

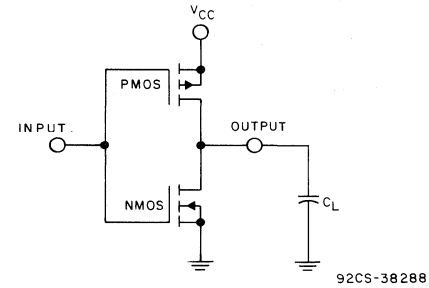

Fig. 4 - Simple QMOS inverter circuit driving a capacitive load.

For power calculation purposes, the load caused by internal device capacitance and switching transition currents is represented in one effective capacitance defined and specified as the C_{pd}, power dissipation capacitance, the effective internal device capacitance used for operating-

Table II - QMOS HC/HCT10 Static Electrical Characteristics and HCT Input Loading Table

Characteristic	CD74HC10/CD54HC10 Test Conditions V_I (V)	I_O (mA)	V_{CC} (V)	74HC/54HC Series +25°C Min.	Typ.	Max.	74HC Series -40/+85°C Min.	Max.	54HC Series -55/+125°C Min.	Max.	CD74HCT10/CD54HCT10 Test Conditions V_I (V)	V_{CC} (V)	74HCT/54HCT Series +25°C Min.	Typ.	Max.	74HCT Series -40/+85°C Min.	Max.	54HCT Series -55/+125°C Min.	Max.	Units
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	μA
Quiescent Device Current per input pin: 1 unit load ΔI_{CC}											$V_{CC}-2.1$	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.4 mA.

HCT Input Loading Table

Input	Unit Loads*
All	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. at 25°C.

power calculations. Each of the above power-consuming factors, along with C_{pd}, are explained in further detail below.

Unlike quiescent power consumption, dynamic, or operating-power, consumption is computed in the same way for both HC and HCT devices. Therefore, throughout this section, all equations presented are applicable to both HC and HCT devices.

Internal Capacitance

Inherent in any active semiconductor is internal parasitic capacitance, i.e., capacitance present in diode junctions, MOS transistor structures, and metal and polysilicon interconnections. This internal capacitance produces the same effect on internal active circuits as external capacitive loads, and varies from one device to another depending on the complexity of the device.

QMOS devices are fabricated by means of a self-aligned polysilicon gate process (3-micron gate length) to reduce this internal capacitance. This process minimizes gate-to-source and gate-to-drain capacitances. Junction capacitances, which are proportional to the junction area, are also reduced because shallower diffusions are utilized.

Fig. 5 illustrates the device parasitic capacitance present in a CMOS inverter.

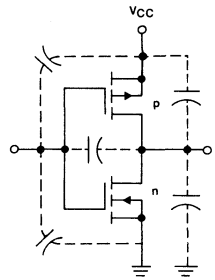

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Fig. 5 - Parasitic capacitances in a CMOS inverter.

Switching Transients

When the basic QMOS inverter circuit, Fig. 6(a), is switching states, either from a logic 1 to a logic 0 or vice-versa, both transistors will be on for a short period of time. This condition creates a momentary low-resistance path between V_{CC} and ground, Fig. 6(b). In this transient state, a momentary dc supply current flows and power is consumed. This low-resistance path is obviously a function of the number of transitions the device makes as well as the input-signal rise and fall time. In other words, power loss resulting from internal device switching is proportional to the input frequency (as is power loss due to internal capacitance).

Power-Dissipation Capacitance

Since power losses resulting from both net internal device capacitance and switching transient currents are frequency dependent, one term representing both factors is used for practical power-consumption calculations. This term is specified as C_{pd}, the no-load power dissipation capacitance.[2] C_{pd} is defined for each QMOS device in each data sheet. Further, it is specified per logic function, that is, for each gate or flip-flop within a device. This method allows for more accurate power consumption calculations when logic functions are operating at different frequencies.

Since C_{pd} encompasses both internal capacitance and switching loads, the internal device operating power per logic function is:

$$P_{pd} = C_{pd}V_{CC}^2f \quad (4)$$

where f is the operating frequency of the function.

COMPUTING HC AND HCT TOTAL POWER DISSIPATION

The formulas for total QMOS power dissipation are a combination of both static and dynamic power-consuming states. For HC devices:

$$P_{total} = V_{CC}I_{CC} + C_{pd}V_{CC}^2f_{in} + C_LV_{CC}^2f_{out} \quad (5)$$

Total HCT power dissipation, when driven by TTL logic, is computed as follows:

$$P_{total} = V_{CC}I_{CC} + \Delta I_{CC} + C_{pd}V_{CC}^2f_{in} + C_LV_{CC}^2f_{out} \quad (6)$$

For HCT devices driven by HC devices, or at equivalent I/O voltage levels, equation (5) is used because the input voltage is essentially at V_{CC}, not at V_{CC} - 2.1 V.

QMOS VERSUS LS AND ALS POWER CONSUMPTION

In any integrated circuit, there exists a balance between speed and power consumption. LSTTL logic is relatively fast, but the bipolar circuitry used consumes considerable amounts of dc power. ALSTTL improves upon LSTTL by utilizing advanced finer-line geometry designs and ap-

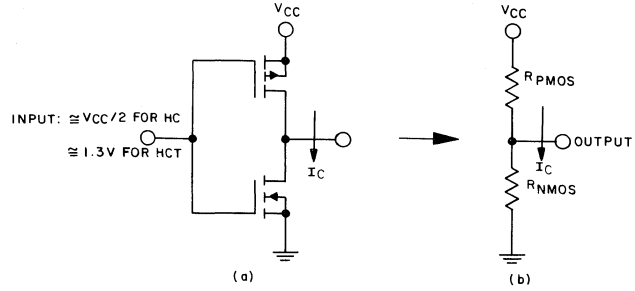

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Fig. 6 - (a) Simple QMOS inverter circuit, (b) equivalent schematic of a QMOS inverter whose transistors represent a low resistance path between V_{CC} and ground.

propriately finer fabrication techniques. These improvements both increase speed and decrease dc power consumption by about 50% total for both factors.

CMOS devices consume minute amounts of quiescent power compared to any given TTL bipolar-logic-family device. However, until the development of the QMOS line of logic devices, CMOS devices were relatively slow. Now, QMOS types, by utilizing finer-line design and fabrication techniques, not only consume the minute amounts of dc and operating power of a CMOS device (depending on operating frequency, as previously defined in equations (5) and (6)), but are fast, as described below.

A popular way to illustrate the differences between IC logic families and their technologies is shown in Fig. 7. In the figure, a 2-input NAND gate is used to illustrate the dc power consumption versus the typical propagation delay for a number of technologies.

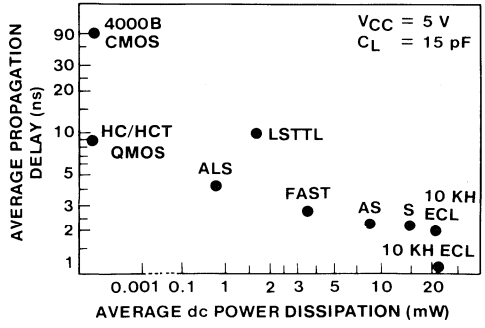

Fig. 7 - Speed/power spectrum for the popular logic technologies.

Table III is a compilation of speed/power products, in picojoules, for two CMOS-logic families and four TTL bipolar-logic families. In the table, SSI and MSI-complexity devices and those with complex flip-flop arrangements are used to illustrate speed/power differences. The major advantages of the new high-speed QMOS (HC/HCT) logic families are apparent:

- CMOS logic families have a 10^3 speed/power advantage over TTL logic families.
- Maximum dc power savings using CMOS are far greater for the more complex MSI logic functions. As shown, a TTLAS160 device consumes 5 x 10^3 times more dc power than an HC160.
- QMOS (HC) logic is approximately 10 times faster than equivalent CMOS devices; but retains the ultra-low dc power consumption of CMOS.

Fig. 8 illustrates the operating power consumption for SSI through MSI, QMOS, and LS devices. Note from the figures that CMOS devices realize their true power savings, from dc to several MHz, depending on device type and complexity. QMOS devices consume significant power only when switching, not when idling. TTL's continuous power consumption is the result of the many active bipolar transistors that must be continuously biased.

Fig. 8 also shows that as device complexity increases, the frequency at which CMOS and TTL devices consume the same amount of power increases, as would be expected.

Table III - Speed Power Comparison - Major TTL and CMOS Logic Families

Generic Type	Logic Family	Max. Prop. Delay[1] (ns)	Max. Power Dissipation[2] (mW)	Speed/Power Product[3] (pj)
Gate	**CMOS** HC00	18	.01	.18
	CD4011	250	.001	.25
	TTL ALS00	13	16.5	215
	LS00	15 (15 pF)	24	363
	AS00	4	95.7	283
	FAST00	5	51	255
FF	**CMOS** HC74	32	.022	.70
	CD4013	300	.006	1.8
	TTL ALS74	17	22	374
	LS74	40 (15 pF)	44	1760
	AS74	8.5	88	748
	FAST74	8	88	704
MSI Counters	**CMOS** HC160	35	.044	1.5
	CD40160	400	.028	11.2
	TTL ASL160	17	116	1964
	LS160	27 (15 pF)	176	4752
	AS160	6	220	1320
	FAST160	10	275	2750

1. V_{CC} = 5 V, C_L = 50 pF (15 pF for LS), T_A = 25° C, max. high or low state.
2. V_{CC} = 5.5 V - max. dc high or low output conditions.
3. Product of max. prop. delay and max. power dissipation.

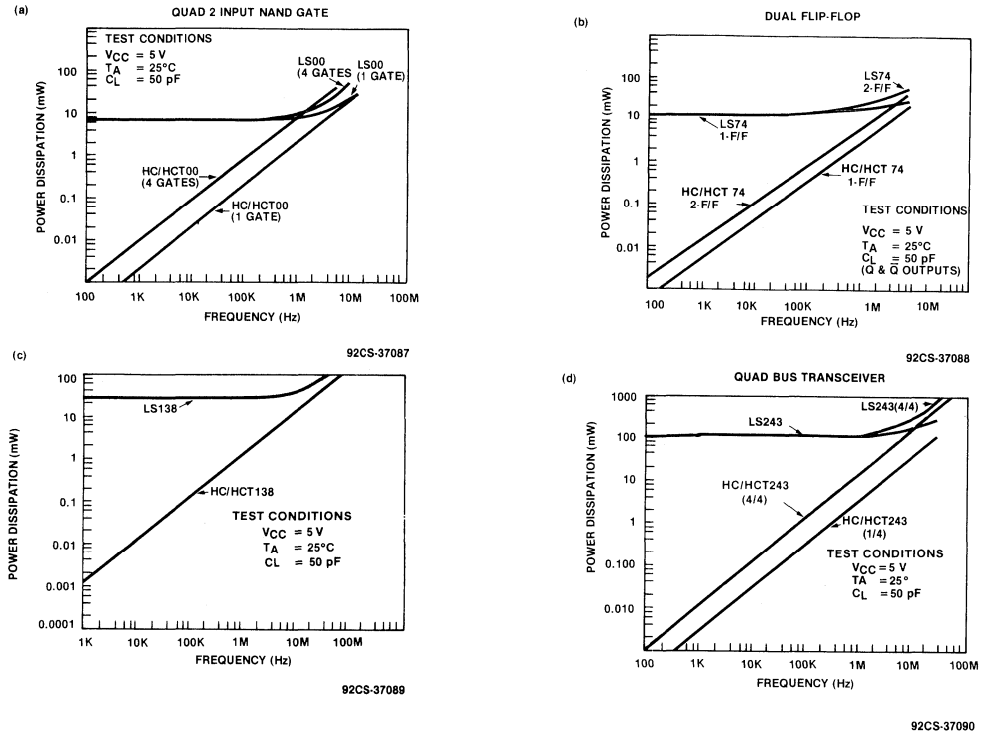

Fig. 8 - Power versus supply graphs for the (a) LS/HC00, (b) LS/HC74, (c) LS/HCT138, and (d) LS/HC243.

QMOS devices also consume more quiescent power as device complexity increases, but the leakage currents that cause the power consumption are of such small magnitude that they can (in most cases) be ignored (see Table I).

The subject figures also illustrate the operating power differences for one function or n functions in an IC package operating at the frequencies shown.

The power-consumption characteristics of these different logic families are easily translated into total system power. Fig. 9 illustrates the power consumed by the different logic families in a small logic system (one gate and two flip-flops). The figure shows that QMOS substantially outperforms TTL in power consumption at both the device and the system level.

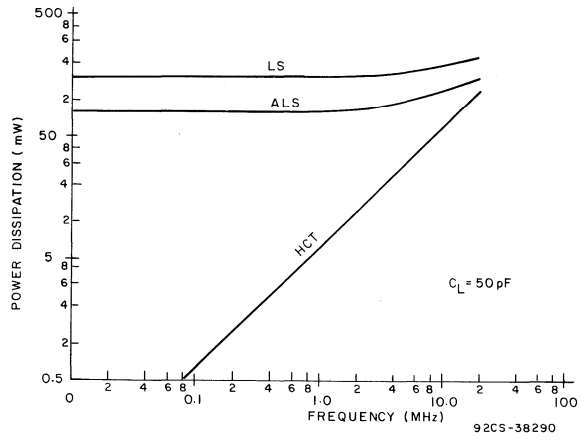

Fig. 9 - Power consumed by different logic families in a small logic system.

REFERENCES

1. The QMOS family consists mainly of two series, the HC, which features CMOS input-voltage-level compatibility, and the HCT, which features LSTTL input-voltage-level compatibility. For a review of these series, see **QMOS High-Speed CMOS Logic ICs**, RCA Solid State DATABOOK SSD-290.
2. See ref. 1 under "Description of QMOS Product Line" for discussion of C_{pd}.

The Double Register Select Unit (DRSU) - GP515

by K. Karstad

The Double Register Select Unit (DRSU), GP515,[1] is a multipurpose LSI device whose primary function is to provide the general processing section, GPU, of a computer with dual register selection. The address fields that select the registers may be derived from an instruction itself or from micromemory.

The DRSU can also generate the bit masks used by the GPU for built-in-test (BIT) setting and test operations, and can expand literal and byte data formats. It can iterate counts outside the microcontroller, a typical shift operation, and increment a selected register address and compare it in multiple load and store operations. The DRSU can also emit constants, either data or address, from micromemory. All of these functions, described more fully below, are frequently required in most computer architectures.

The GP515, available in a 64-lead LCC package, is specifically designed to be used with the 8-bit-slice general-processor unit GP001.[2] However, this does not preclude its use with any register arithmetic logic unit (RALU) that contains a two-port register file.

The DRSU is implemented in CMOS/SOS technology. The advantages of CMOS are many and well known; the SOS technology adds radiation-tolerant features, many of which are superior to those of other technologies. The GP515 is a member of the EPIC (Emulating and Programmable IC) family of bit-slice and microprogrammable parts for high-performance computers. These parts are finding wide acceptance in critical radiation-prone aerospace applications.

DRSU ARCHITECTURE

The DRSU is controlled by the three-bit control inputs, RC_{2-0}, the control enable input, RCEN, and the 12-bit microfield inputs, MF_{11-0}, Fig. 1. Generally, the RC field determines which function is performed, and the RCEN input enables or disables execution of the function. The MF inputs control the detailed operation of each function.

The DRSU handles two data sources. One is a 16-bit bidirectional data bus (BIO), which is used to both receive and transmit data. A second data source is the 12-bit microfield (MF_{11-0}), which can be used to input constants when it is not being used to control internal functions.

There are three 8-bit data registers in the DRSU, each of which can be loaded in 4-bit groups. The DRSU contains two operand registers (UOR and LOR). The third register is the source register (SR), which is shared by the two halves of the DRSU. Each of these registers can be loaded from either the data-bus or microfield data inputs.

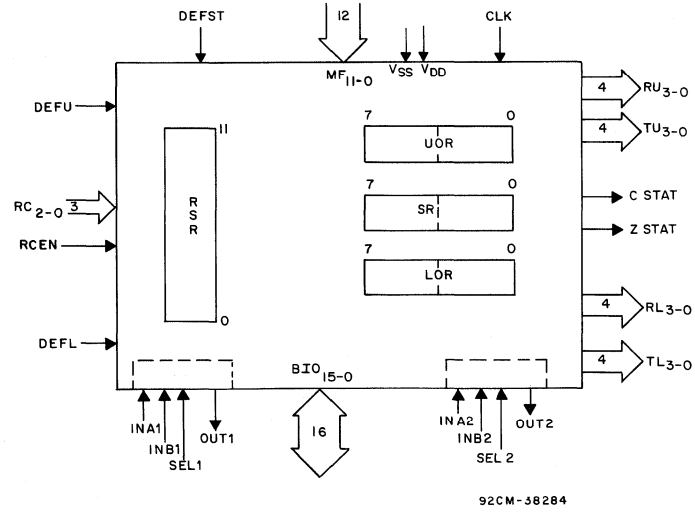

Fig. 1 - Block diagram of the Double Register Select Unit (DRSU), GP515.

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Data can be transferred from the UOR or the LOR to the SR, and from the SR to the UOR or LOR in either 4-bit or 8-bit quantities. Data may also be transferred between halves of the SR. Either half of the SR can be incremented by one, two, or three.

There are four sets of 4-bit outputs designated RU, RL, TU, and TL. The data for these outputs is selected by the 12-bit register-select-register (RSR), which contains six bits of information for each DRSU half. The RSR may be loaded with a command denoted by the RC inputs, or it may be loaded with a known constant (309_H) by using the DEFST input. RU and TU outputs are shown in Table I. RL and TL outputs are similar to those of RU and TU except that they use SR and LOR as data sources.

Table I - RU and TU Outputs

RU Outputs	TU Outputs
SR_{7-4}	SR_{3-0}
$(SR_{7-4}) + 1$	$(SR_{3-0}) + 1$
$(SR_{7-4}) + 2$	$(SR_{3-0}) + 2$
$(SR_{7-4}) + 3$	$(SR_{3-0}) + 3$
UOR_{3-0}	UOR_{7-4}
$(UOR_{3-0}) + 1$	$(UOR_{7-4}) + 1$
$(UOR_{3-0}) + 2$	$(UOR_{7-4}) + 2$
$(UOR_{3-0}) + 3$	$(UOR_{7-4}) + 3$

Either half of the RSR can be overridden by the default inputs. A logic 1 on DEFU selects SR_{7-4} as the source for RU, and SR_{3-0} as the source for TU. A logic 1 on the DEFL selects the same values for RL and TL. Except for these default cases, where the default inputs are 1, the content of RSR always affects the values of RU, TU, RL, and TL.

Note that an immediate data change on RU, RL, TU, and TL takes place when the clock is low if UOR, LOR, SR, or the RSR is changed.

As shown in Fig. 2, some additional gates are available on the DRSU for select logic use; the use of these gates does not affect any other functions of the DRSU.

MICROPROGRAMMING THE GP515

All micro-operations performable by the DRSU are summarized and detailed in the Appendix to this Note. The function to be performed by the DRSU is determined by the 3-bit RC field and the RC enable (RCEN) input. When RCEN is a logical 1, the function denoted by the RC field is executed. When RCEN is a logical 0, no operation is done. The eight possible functions controlled by the field RC_{2-0} are summarized in Table II. Below are some comments on the operation codes identified in the RC fields.

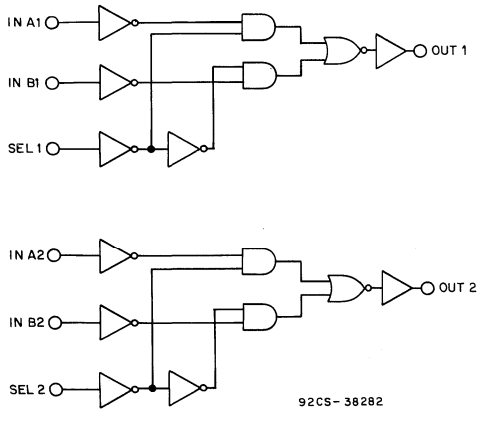

Fig. 2 - Dedicated select logic of the GP515.

Table II - The Eight Basic Functions of the GP515 When RCEN is a Logical 1

RC Field 2	1	0	Operation
0	0	0	No Op
0	0	1	Load register from BIO
0	1	0	Load register from MF_{3-0}
0	1	1	Load register from MF_{7-0}. Optional output.
1	0	0	Load register/select register
1	0	1	Output to BIO
1	1	0	Register transfer
1	1	1	Increment SR

Operation Codes

Opcode 0—A no-operation condition.

Opcode 1—The registers SR, UOR, and LOR may be loaded from either the high byte or low byte of the 16-bit bus (BIO). Any or all of the registers may be loaded from either source.

Opcode 2—Either half of registers SR, UOR, or LOR may be loaded from the 4-bits in the control field, MF_{3-0}.

Opcode 3—Eight bits in control field MF_{7-0} are used as data to be loaded into registers SR, UOR, and LOR. One option is to output the data on the low byte of BIO. Any or all of the operations may be performed.

Opcode 4—The DEFST input determines two possibilities. If DEFST is high, the register-select-register (RSR) is loaded with a constant 309_H. If the DEFST input is low, the RSR is loaded with the data in control field MF_{11-0}. Each bit in the RSR now selects part of the data source for RU, TU, RL, and TL. For example, MF_{11-0} selects the high nibble of SR as the source for the low nibble of RU. One, two, or three can be added to each data source. To add three, simply combine the expressions for adding one and two. As an example, programming $RSR_{10} = 1$ and $RSR_9 = 1$ will add 3 to the low nibble of RU. In each case, the adding of one, two, or three does not affect the source selection; it simply adds the value to the selected source.

Opcode 5—A value is output on the 16-bit bus. Control bits MF_{7-4} determine what should appear on the high byte of BIO, while bits MF_{3-0} determine what appears on the low byte of BIO. The Appendix to this Note is a list of all possible options.

Opcode 6—One of the following operations may be done:

1. *Data can be transferred from the SR to the LOR or the UOR.*
2. *Data can be transferred from the UOR or LOR to the SR.*
3. *The previous value (before change) of either half of the SR can be transferred to the other half.*

Opcode 7—The two nibbles of the SR may be incremented by one, two, or three. If MF_8 is high, the increment is conditional depending upon a comparison of SR_{7-4} and SR_{3-0}; SR_{3-0} is not incremented. If MF_8 is low, no comparison is done between SR_{7-4} and SR_{3-0}, and SR_{7-4} or SR_{3-0} may be incremented according to the values of bits MF_{7-6} or MF_{5-4}, respectively.

Note that if a comparison is done between SR_{7-4} and SR_{3-1}, the previous values (before increment) are used. Therefore, the result of an increment does not change the results of the comparison.

Status

Status information is provided at all times by the status outputs. The compare status output, CSTAT, is true (logical 1) whenever SR_{7-4} equals SR_{3-0}. The zero status output, ZSTAT, is true (logical 1) whenever SR_{3-0} is zero. These status outputs can change whenever the SR changes as a result of a register load, transfer, or increment.

Default Operation

Table III describes default operation.

Table III - Default Operation

DEFU	DEFL	Action
1		$SR_{7-4} \rightarrow RU$; $SR_{3-0} \rightarrow TU$
0		RSR determines R and T
	1	$SR_{7-4} \rightarrow RL$; $SR_{3-0} \rightarrow TL$
	0	RSR determines R and T

APPLICATION OF THE GP515

As noted above, the primary function of the DRSU is to provide register selection in RALU bit slices. Fig. 3 shows a typical system application. The GP001 in the application contains a 16 x 8 two-port register file that is addressed by two 4-bit fields, R and T. (Note that, while two registers can be read simultaneously by R and T, a write operation requires an R field.) GPU I and GPU II in the figure may be single 8-bit slices or concatenated bit-slices making up data formats in multiples of eight bits.

In most 16-bit macroinstructions, the register designators are located in the lower eight bits with the opcode located in the upper eight bits. Fig. 4 shows the instruction format for register-to-register operation in the MIL-STD-1750A instruction set. The 16-bit instruction consists of an 8-bit opcode and two 4-bit general register (GR) fields that typically specify any of sixteen general registers. In addition, these fields may contain a shift count, condition code, opcode extension, bit number, or the operand for immediate short instructions. Typically, GR1 designates the R address and GR2 the T address.

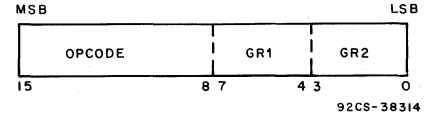

Fig. 4 - Register-to-register instruction format for MIL-STD-1750A instruction set.

When a new macroinstruction is processed, the lower eight bits are loaded into the source register (SR) and both operand registers (UOR, LOR) of the DRSU. During normal operation, the R and T output addresses are defined by the contents of the DRSU's internal register-select-register (RSR). This register is loaded by use of the macroinstruction through the MF_{11-0} control field. The functions controlled by each bit in the RSR are detailed in the Appendix. Note that multiple micro-operations can be done simultaneously depending on the contents of the RSR. It is evident that the programmer can select any of the combinations (R,T), (R,R), (T,R), or (T,T) for addressing the GPU register files.

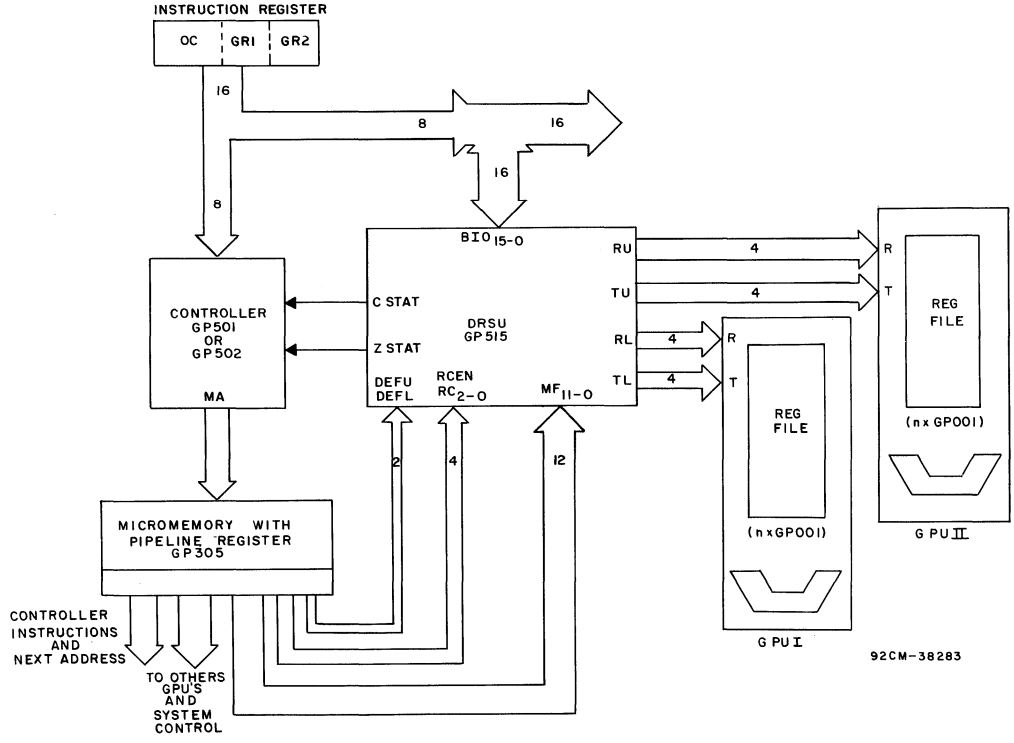

Fig. 3 - Typical system application of the GP515.

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The default inputs DEFU and DEFL play an important part in arithmetic operations. When DEFU is 1, the high nibble of SR goes to the RU output and the low nibble to the TU output. Similarly, if DEFL is 1, the high and low nibbles of SR go to RL and TL, respectively. With the sample instruction format in Fig. 4, GR1 is quickly provided as the R address and GR2 as the T address, independent of the contents of the RSR. This feature allows the storing of register-select controls for double precision, and the use of the default signals for single precision.

Another important feature of the DRSU is its ability to format data contained in the instruction format for the GPU. Many instructions reference bit, literal, and byte data. In most cases, data referenced by these operations is contained in the lower eight bits of the macroinstruction loaded into the DRSU at the beginning of each instruction cycle.

In addition to selecting register designators, the DRSU can be programmed to output either the most or least significant 16-bits of the literal expansion, byte expansion, or 1 of 16 bit masks. The device can generate a full 16-bit operand, and has the ability to read an entire 16-bit bus as well as output 16 bits at a time.

In Fig. 3 the status outputs of the DRSU go to the controller for conditional testing. If a GP501[3] is used, the outputs feed the discrete input pins directly. If the GP502[4] is selected, an external condition-code multiplexer is required between the output signals and the controller.

REFERENCES

1. GP515 Double Register Select Unit, RCA Solid State Preliminary Data Sheet.
2. "An Introduction to the Use of the General-Processor Unit, GP001," K. Karstad, RCA Solid State Application Note ICAN-7202.
3. "A Guide to the Emulating Microprogram Controller GP501 - With Programming Examples," K. Karstad, RCA Solid State Application Note ICAN-7259.
4. GP502 Microprogram Sequencer, RCA Solid State Preliminary Data Sheet.

APPENDIX - Summary of Micro-operations Performed by DRSU

Note: Unspecified bit positions are **not** always Don't Care conditions and multi micro-operations may be programmed in the same instruction.

11 10 9	MF 8 7 6	5 4 3	2 1 0	RC	ACTION
				0	NO OP
1	0			1	SR_{7-0} ←BIO_{15-8}
1	1				SR_{7-0} ←BIO_{7-0}
	1	0			UOR_{7-0} ←BIO_{15-8}
1		1			UOR_{7-0} ←BIO_{7-0}
	1	0			LOR_{7-0} ←BIO_{15-8}
	1	1			LOR_{7-0} ←BIO_{7-0}
1				2	SR_{7-0}, SR_{3-0}, LOR_{7-4}, LOR_{3-0}, UOR_{7-4}, UOR_{3-0} ←MF_{3-0}
	1				
		1			
			1		
1				3	BIO_{15-8}←00, BIO_{7-0}, SR_{7-0}, UOR_{7-0}, LOR_{7-0} ←MF_{7-0}
	1				
		1			
			1		

IF DEFST = 1;
RSR_{11-0}←309H

IF DEFST = 0;
RSR_{11-0} ← MF_{11-0}

11 10 9	RSR 8 7 6	5 4 3	2 1 0	RC	ACTION
1				4	$RU_{3-0} = UOR_{3-0}$
0					$RU_{3-0} = SR_{7-4}$
	1				$RU_{3-0} + 2$
		1			$RU_{3-0} + 1$
1	1				$RU_{3-0} + 3$
			1		$TU_{3-0} = UOR_{7-4}$
	0				$TU_{3-0} = SR_{3-0}$
		1			$TU_{3-0} + 2$
			1		$TU_{3-0} + 1$
	1	1			$TU_{3-0} + 3$
		1			$RL_{3-0} = LOR_{3-0}$
		0			$RL_{3-0} = SR_{7-4}$
			1		$RL_{3-0} + 2$
		1			$RL_{3-0} + 1$
		1	1		$RL_{3-0} + 3$
			1		$TL_{3-0} = LOR_{7-4}$
			0		$TL_{3-0} = SR_{3-0}$
		1			$TL_{3-0} + 2$
			1		$TL_{3-0} + 1$
		1	1		$TL_{3-0} + 3$
	0 0	0	0	5	$BIO_{15-8} = 0$
	0 0	0	1		
	0 0	1	0		$BIO_{15-8} = UOR_7$
	0 0	1	1		
	0 1	0	0		TEST UOR_{3-0}: IF $UOR_{3-0} > 7$, THEN $BIO_{15-8} = 0$; IF $UOR_{3-0} = 0$, THEN $BIO_{15-8} = 01$; IF $UOR_{3-0} = 1$, THEN $BIO_{15-8} = 02$; IF $UOR_{3-0} = 2$, THEN $BIO_{15-8} = 04$; IF $UOR_{3-0} = 3$, THEN $BIO_{15-8} = 08$; IF $UOR_{3-0} = 4$, THEN $BIO_{15-8} = 10$; IF $UOR_{3-0} = 5$, THEN $BIO_{15-8} = 20$; IF $UOR_{3-0} = 6$, THEN $BIO_{15-8} = 40$; IF $UOR_{3-0} = 7$, THEN $BIO_{15-8} = 80$
	0 1	0	1		TEST UOR_{3-0}: IF $UOR_{3-0} > 7$, THEN $BIO_{15-8} = 0$; IF $UOR_{3-0} = 0$, THEN $BIO_{15-8} = 80$; IF $UOR_{3-0} = 1$, THEN $BIO_{15-8} = 40$; IF $UOR_{3-0} = 2$, THEN $BIO_{15-8} = 20$; IF $UOR_{3-0} = 3$, THEN $BIO_{15-8} = 10$; IF $UOR_{3-0} = 4$, THEN $BIO_{15-8} = 08$; IF $UOR_{3-0} = 5$, THEN $BIO_{15-8} = 04$; IF $UOR_{3-0} = 6$, THEN $BIO_{15-8} = 02$; IF $UOR_{3-0} = 7$, THEN $BIO_{15-8} = 01$
	0 1	1	0		BIO_{15-8} = UOR7
	0 1	1	1		
	1 1	1	0		
	1 1	1	1		

11 10 9	MF 8 7	6 5 4	3 2 1 0	RC	ACTION
	1 0	0 0		5	$BIO_{15-12} = MF_{11-8}$ & $BIO_{11-8} = UOR_{7-4}$
	1 0	0 1			
	1 0	1 0			$BIO_{15-12} = MF_{11-8}$ & $BIO_{11-8} = UOR_{3-0}$
	1 0	1 1			
	1 1	0 0			TEST UOR_{3-0}: IF $UOR_{3-0} < 8$, THEN $BIO_{15-8} = 0$; IF $UOR_{3-0} = 8$, THEN $BIO_{15-8} = 01$; IF $UOR_{3-0} = 9$, THEN $BIO_{15-8} = 02$; IF $UOR_{3-0} = A$, THEN $BIO_{15-8} = 04$; IF $UOR_{3-0} = B$, THEN $BIO_{15-8} = 08$; IF $UOR_{3-0} = C$, THEN $BIO_{15-8} = 10$; IF $UOR_{3-0} = D$, THEN $BIO_{15-8} = 20$; IF $UOR_{3-0} = E$, THEN $BIO_{15-8} = 40$; IF $UOR_{3-0} = F$, THEN $BIO_{15-8} = 80$
	1 1	0 1			TEST UOR_{3-0}: IF $UOR_{3-0} < 8$, THEN $BIO_{15-8} = 0$; IF $UOR_{3-0} = 8$, THEN $BIO_{15-8} = 80$; IF $UOR_{3-0} = 9$, THEN $BIO_{15-8} = 40$; IF $UOR_{3-0} = A$, THEN $BIO_{15-8} = 20$; IF $UOR_{3-0} = B$, THEN $BIO_{15-8} = 10$; IF $UOR_{3-0} = C$, THEN $BIO_{15-8} = 08$; IF $UOR_{3-0} = D$, THEN $BIO_{15-8} = 04$; IF $UOR_{3-0} = E$, THEN $BIO_{15-8} = 02$; IF $UOR_{3-0} = F$, THEN $BIO_{15-8} = 01$
			0 0 0 0		$BIO_{7-0} = 0$
			0 0 0 1		
			0 0 1 0		
			0 0 1 1		
			0 1 0 0		TEST LOR_{3-0}: IF $LOR_{3-0} > 7$, THEN $BIO_{7-0} = 0$; IF $LOR_{3-0} = 0$, THEN $BIO_{7-0} = 01$; IF $LOR_{3-0} = 1$, THEN $BIO_{7-0} = 02$; IF $LOR_{3-0} = 2$, THEN $BIO_{7-0} = 04$; IF $LOR_{3-0} = 3$, THEN $BIO_{7-0} = 08$; IF $LOR_{3-0} = 4$, THEN $BIO_{7-0} = 10$; IF $LOR_{3-0} = 5$, THEN $BIO_{7-0} = 20$; IF $LOR_{3-0} = 6$, THEN $BIO_{7-0} = 40$; IF $LOR_{3-0} = 7$, THEN $BIO_{7-0} = 80$
			0 1 0 1		TEST LOR_{3-0}: IF $LOR_{3-0} > 7$, THEN $BIO_{7-0} = 0$; IF $LOR_{3-0} = 0$, THEN $BIO_{7-0} = 80$; IF $LOR_{3-0} = 1$, THEN $BIO_{7-0} = 40$; IF $LOR_{3-0} = 2$, THEN $BIO_{7-0} = 20$; IF $LOR_{3-0} = 3$, THEN $BIO_{7-0} = 10$; IF $LOR_{3-0} = 4$, THEN $BIO_{7-0} = 08$; IF $LOR_{3-0} = 5$, THEN $BIO_{7-0} = 04$; IF $LOR_{3-0} = 6$, THEN $BIO_{7-0} = 02$; IF $LOR_{3-0} = 7$, THEN $BIO_{7-0} = 01$
			0 1 1 0		$BIO_{7-0} = LOR_{7-0}$
			0 1 1 1		
			1 1 1 0		
			1 1 1 1		
			1 0 0 0		$BIO_{7-4} = MF_{11-8}$ & $BIO_{3-0} = LOR_{7-4}$
			1 0 0 1		
			1 0 1 0		$BIO_{7-4} = MF_{11-8}$ & $BIO_{3-0} = LOR_{3-0}$
			1 0 1 1		
			1 1 0 0		TEST LOR_{3-0}: IF $LOR_{3-0} < 8$, $BIO_{7-0} = 0$; IF $LOR_{3-0} = 8$, THEN $BIO_{7-0} = 01$; IF $LOR_{3-0} = 9$, THEN $BIO_{7-0} = 02$; IF $LOR_{3-0} = A$, THEN $BIO_{7-0} = 04$; IF $LOR_{3-0} = B$, THEN $BIO_{7-0} = 08$; IF $LOR_{3-0} = C$, THEN $BIO_{7-0} = 10$; IF $LOR_{3-0} = D$, THEN $BIO_{7-0} = 20$; IF $LOR_{3-0} = E$, THEN $BIO_{7-0} = 40$; IF $LOR_{3-0} = F$, THEN $BIO_{7-0} = 80$
			1 1 0 1		TEST LOR_{3-0}: IF $LOR_{3-0} < 8$, $BIO_{7-0} = 0$; IF $LOR_{3-0} = 8$, THEN $BIO_{7-0} = 80$; IF $LOR_{3-0} = 9$, THEN $BIO_{7-0} = 40$; IF $LOR_{3-0} = A$, THEN $BIO_{7-0} = 20$; IF $LOR_{3-0} = B$, THEN $BIO_{7-0} = 10$; IF $LOR_{3-0} = C$, THEN $BIO_{7-0} = 08$; IF $LOR_{3-0} = D$, THEN $BIO_{7-0} = 04$; IF $LOR_{3-0} = E$, THEN $BIO_{7-0} = 02$; IF $LOR_{3-0} = F$, THEN $BIO_{7-0} = 01$

APPENDIX - Summary of Micro-operations Performed by DRSU (Cont'd)

11	10	9	8	7	MF 6	5	4	3	2	1	0	RC	ACTION
1												6	$SR_{7-4} = SR_{3-0}$
	1	1						1					$SR_{7-4} = UOR_{7-4}$
1	1	1						0					$SR_{7-4} = LOR_{7-4}$
1	0	1						0					$SR_{3-0} = SR_{7-4}$
1			1					1					$SR_{3-0} = UOR_{3-0}$
1	1		1					0					$SR_{3-0} = LOR_{3-0}$
1	0		1					0					
0													$LOR_{7-4} = SR_{7-4}$
0				1									$LOR_{3-0} = SR_{3-0}$
0					1								$UOR_{7-4} = SR_{7-4}$
0						1							$UOR_{3-0} = SR_{3-0}$
			1									7	COMPARE SR_{7-4} & SR_{3-0}:
			1	1									IF $SR_{7-4} \neq SR_{3-0}$, THEN $SR_{7-4} + 2$
			1		1								IF $SR_{7-4} \neq SR_{3-0}$, THEN $SR_{7-4} + 1$
			1	1	1								IF $SR_{7-4} \neq SR_{3-0}$, THEN $SR_{7-4} + 3$
				0	0								NO CHANGE IN SR_{7-4}
			0										NO COMPARISON DONE:
			0	1									$SR_{7-4} + 2$
			0		1								$SR_{7-4} + 1$
			0	1	1								$SR_{7-4} + 3$
				0	0								NO CHANGE IN SR_{7-4}
			0			1							$SR_{3-0} + 2$
			0				1						$SR_{3-0} + 1$
			0			1	1						$SR_{3-0} + 3$
						0	0						NO CHANGE IN SR_{3-0}

Designing with the Microprogram Sequencer GP502

by K. Karstad

The GP502 microprogram controller or sequencer is an address sequencer designed to control the execution sequence of microinstructions stored in a microprogram memory. The GP502 is functionally equivalent to the industry's well known AM2910. Moreover, the DIL versions are pin equivalent. The GP502, however, is implemented in CMOS/SOS, with its inherent technological advantages, including excellent radiation tolerance for aerospace applications. The GP502 is one of the key building blocks in the EPIC (Emulating and Programmable IC) series of LSI parts for high-performance computers employing micro-programmable bit-slice architecture.

A microprogrammed machine is defined as one in which a coherent sequence of microinstructions is used to execute various commands required by the machine. The machine may or may not be a computer. If it is a computer, each sequence of microinstructions defines a machine or macroinstruction. All the small elemental tasks performed by the machine in executing the machine instructions are called the microinstructions. Typical elemental tasks are: enable content of the memory address register to the address lines, read program memory, load instruction register, increment program counter. Frequently, a number of these elemental tasks are performed in parallel by dedicated bits assigned in micromemory. Clearly, the wider the micromemory is (the greater the number of horizontal bits) the more tasks can be executed simultaneously by one microword. More often several microwords are required to perform one machine instruction. The storage area for these microinstructions is called a microprogram memory or control store.

It is important to distinguish between machine-level instructions and microprogram instructions. Fig. 1 shows a typical machine instruction for a 16-bit machine with an 8-bit opcode and two 4-bit register designators. The machine instruction could be a register-to-register instruction which says: read the contents of the register whose address is R1, add it to the contents of the register designated R2, and store the result in the register addressed as R1. The microinstruction can have any number of bits, but has two primary parts: the definition and control of all elemental micro-operations to be carried out, and the definition and control of the address of the next microinstruction to be executed. The various micro-operations to be carried out include ALU function selection, shift control, and data in and data out control.

In the example in Fig. 1, the 8-bit CPU slice GP001 is assumed, and the operand registers are defined in the macroinstruction by R1 and R2. Some bits in the microword instruct the GP001 to add and steer the data flow for the add operation. The two leftmost fields control the GP502 sequencer. The sequencer must be instructed what to do next. It could be a Continue instruction, which simply increments the microprogram counter to the next micro-instruction, or it could be a test of the machine's ALU status, which dictates that the microprogram jump to a branch address specified in the current microword.

For each new machine instruction the opcode is loaded into the instruction register and decoded in an instruction decoder. The output from the controller is the microprogram address where the first step of the execution sequence for

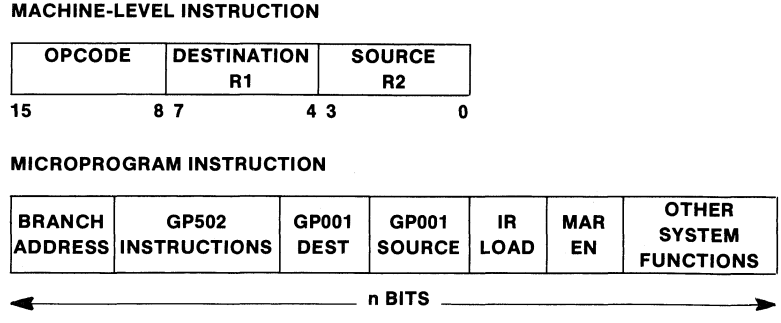


Fig. 1 - Typical machine instruction for a 16-bit machine with an 8-bit opcode and two 4-bit register designators.

that microinstruction resides in microprogram memory. The GP502 sequencer then generates the microprogram address of the next microinstruction. Note that the microprogram word supplies the control signals needed to control all parts of the computer, *including the sequencer itself*. When all of the steps of a machine instruction are executed, the microprogram fetches the next machine instruction from the computer's main memory.

ARCHITECTURE

The internal architecture of the GP502 sequencer, the center of the control section that orchestrates overall computer operation, is described in the functional block diagram in Fig. 2. The sequencer can address up to 4k words of microprogram. The microprogram address field, Y, is derived from one of four sources through the internal multiplexer. The first source is the direct input D, which is used for branching. The input may come from a mapper ROM or a field in the microword.

The second source is derived from a register/counter R. The register/counter is a 12-bit edge-triggered device. When the load control, $\overline{RLD}$, is low, new data is loaded on a positive-edge transition. The register/counter is operated during some microinstructions as a 12-bit down counter. "Content = zero" is then used as a microinstruction branch criterion. Iteration of microinstructions is thus possible. If the register/counter is preloaded with a number N, and then used as a loop termination counter, the sequence will be executed exactly N+1 times.

The third source of the microprogram address field, Y, is the stack (source F), a 5-word by 12-bit file. The stack is used to provide return-address linkage when microsubroutines or loops are executed. A built-in stack pointer always points to the last file-word written. At reset, the depth of nesting becomes zero. For each push, the nesting increases by one; for each pop, the depth decreases by one. The depth can grow to five, after which the $\overline{FULL}$ signal goes low. Any further pushes onto a full stack overwrite information at the top of the stack. (The stack pointer remains unchanged.) The stack pointer remains at zero if a pop is executed from an empty stack, although the data is meaningless. The $\overline{FULL}$ warning signal appears on the microcycle after a fifth push.

The fourth and last source for the microprogram address is the 12-bit microprogram counter, μPC. Associated with the μPC is an incrementer. When the carry-input, CI, is high, the μPC is loaded on the next clock cycle with the current Y output word plus one. Sequential microinstruction are thus executed. When CI is low, the incrementer passes the Y output word unmodified, so that the μPC is reloaded with the same Y word on the next clock cycle. The same microinstruction is therefore executed once again.

A 4-bit instruction field, I, controls the multiplexer and determines the Y output. The three enable signals, $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$ are also controlled by the I-field, and for each instruction, one and only one of the three outputs is active low. These outputs may control 3-state enable inputs for

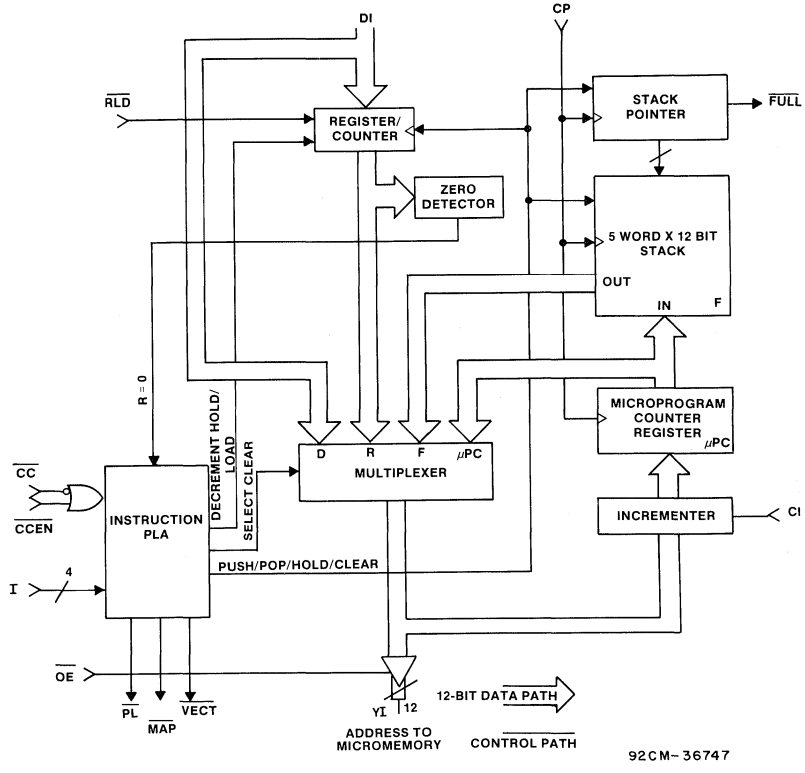


Fig. 2 - Block diagram of the microcontroller, GP502.

devices used to drive the data inputs, D. Input sources may be a pipeline register, a mapper ROM, etc.

The sequencer provides 3-state Y outputs. This feature may be useful in diagnostics. If the Y output is forced into a high-impedance state, preprogrammed sequences of microinstructions can be executed through external access to the address bus.

The $\overline{CC}$ pin accepts the condition-code signal, for example one of the ALU's status signals. If $\overline{CC}$ is low, the test passes.

$\overline{CCEN}$ is a condition-code enable input. Whenever the signal is high, the input at $\overline{CC}$ is ignored and the sequencer operates as though $\overline{CC}$ were true (low).

INSTRUCTIONS AND MICROPROGRAMMING

The 4-bit I-field designates one of sixteen unique instructions. These instructions are summarized in Table I; Table II lists the pin functions. Each instruction is described functionally below. For data flow, refer to the figures noted in the descriptions; these figures are contained in the Appendix.

Table I - GP502 Instructions

				FAIL		PASS			
			REG/ CNTR CON-	$\overline{CCEN}$=LOW and $\overline{CC}$=HIGH		$\overline{CCEN}$=HIGH or $\overline{CC}$=LOW		REG/	
I_3-I_0	MNEMONIC	NAME	TENTS	Y	STACK	Y	STACK	CNTR	ENABLE
0	JZ	JUMP ZERO	X	0	CLEAR	0	CLEAR	HOLD	PL
1	CJS	COND JSB PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/COND LD CONTR	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	COND JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP VECTOR	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP, CNTR≠0	≠0	F	HOLD	F	HOLD	DEC	PL
			= 0	PC	POP	PC	POP	HOLD	PL
9	RPCT	REPEAT PL, CNTR≠0	≠0	D	HOLD	D	HOLD	DEC	PL
			= 0	PC	HOLD	PC	HOLD	HOLD	PL
10	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
11	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
12	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
13	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
14	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
15	TWB	THREE-WAY BRANCH	≠0	F	HOLD	PC	POP	DEC	PL
			= 0	D	POP	PC	POP	HOLD	PL

Note 1: If $\overline{CCEN}$ = Low and $\overline{CC}$ = High, hold; otherwise load. X = Don't Care.

Table II - Pin Functions

Abbreviation	Name	Function
D_i	Direct Input Bit i	Direct input to register/counter and multiplexer. D_0 is LSB.
I_i	Instruction Bit i	Selects one-of-sixteen instructions for GP502.
$\overline{CC}$	Condition Code	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	Condition Code Enable	When the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	Carry-in	Low order carry input to incrementer for microprogram counter.
$\overline{RLD}$	Register Load	When LOW forces loading of register/counter regardless of instruction or condition.
$\overline{OE}$	Output Enable	Three-state control of Y_i outputs.
CP	Clock Pulse	Triggers all internal state changes at LOW-to-HIGH edge.
V_{DD}	+ Supply	
GND	Ground	
Y_i	Microprogram Address Bit i	Address to microprogram memory. Y_0 is LSB, Y_{11} is MSB.
$\overline{FULL}$	Full	Indicates that five items are on the stack.
$\overline{PL}$	Pipeline Address Enable	Can select a source (usually Pipeline Register) as direct input source.
$\overline{MAP}$	Map Address Enable	Can Select a source (usually Mapping PROM or PLA) as direct input source.
$\overline{VECT}$	Vector Address Enable	Can select a source (for example, Interrupt Starting Address) as direct input source.

I = 0: JZ — Jump Zero

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
0	0	$\overline{PL}$	X	NC	Clear

X = Don't care NC = No Change

Instruction Jump Zero, JZ, unconditionally specifies that the address of the next microinstruction is zero. It is assumed in Fig. A-1 that the hardware can reset the pipeline register, which forces the instruction I = 0. Another technique for initialization is to use pull-up resistors on the Y address bus, so that at reset the address FFF is applied to micromemory. The JZ instruction should then be located at the memory address (FFF).

I = 1: CJS — COND JSB PL

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
1	D	$\overline{PL}$	Pass	NC	Push
1	μPC	$\overline{PL}$	Fail	NC	NC

X = Don't Care NC = No Change

This instruction is a Conditional Jump to Subroutine, Pipeline, CJS, whose address is found in the pipeline register; see Fig. A-2.

Assume that the contents of memory at address 23 are in the pipeline register, and that the microword contains the CJS instruction. A test is made of the input at $\overline{CC}$, and if the test passes the next instruction to be executed, it is found at the branch address in the pipeline, for example, address 57. In this case, the value 24 will be pushed onto the internal stack, providing the return linkage for the machine when the subroutine beginning at location 57 is completed. If the test had failed (i.e., $\overline{CC}$ = H), the contents of the microprogram memory at location 24 would have been executed instead.

I = 2: JMAP — JUMP MAP

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
2	D	$\overline{MAP}$	X	NC	NC

X = Don't Care NC = No Change

The JMAP, Jump Map, instruction is normally used at the end of the machine's fetch sequence. It is an unconditional instruction, and when encountered in the pipeline register, causes the $\overline{MAP}$ output to be enabled; see Fig. A-3. The next microinstruction address is then determined by the address supplied from the mapping ROM. Again, this step would normally be the first one in a new sequence defining another macroinstruction.

I = 3: CJP — COND JUMP PL

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
3	D	$\overline{PL}$	Pass	NC	NC
3	μPC	$\overline{PL}$	Fail	NC	NC

X = Don't Care NC = No Change

Often, state machines simply execute tests on various inputs, waiting for the condition represented to be realized. When the true condition is reached, the machine branches and executes a set of microinstructions to perform some function. Usually, part of the routine is to reset the input being tested until some future time.

Fig. A-4 illustrates the Conditional Jump Pipeline, CJP, instruction. This instruction provides a technique for branching to various microprogram sequences depending upon the test conditions input at $\overline{CC}$.

If the test passes, the value currently in the pipeline register is the new microprogram address. If the test fails, the next address selected is the microprogram counter.

I = 4: PUSH — PUSH/COND LD CNTR

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
4	μPC	$\overline{PL}$	Pass	Load	Push
4	μPC	$\overline{PL}$	Fail	NC	Push

X = Don't Care NC = No Change

The Push/Conditional Load Counter, PUSH, instruction is useful for setting up loops in microprogram firmware.

Assume that the instruction is in the pipeline register; see Fig. A-5. A push is made onto the stack of the next sequential instruction address. This push is unconditional, however the counter is only loaded if the test passes. A single microinstruction can, therefore, be used to set up a loop to be executed a specific number of times. Note that Push is a set-up instruction that must always immediately precede the first statement in a loop controlled by LOOP or RFCT. (The LOOP and RFCT instructions are described below.)

I = 5: JSRP — COND JSB R/PL

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
5	D	$\overline{PL}$	Pass	NC	Push
5	R	$\overline{PL}$	Fail	NC	Push

X = Don't Care NC = No Change

I = 5 is a Conditional Jump to Subroutine, Register/Counter /Pipeline, JSRP, where the new microprogram address comes either from the pipeline register or the register /counter; see Fig. A-6. A push is always executed (same return address on top of the stack), and one of two subroutines is executed.

Assume that the JSRP instruction is located at address 32 in the micromemory, and that the instruction is currently in the pipeline register. Let two subroutines have start addresses 60 to 70. For proper operation, a load register /counter instruction must exist at address 1 (Fig. A-6), which loads one branch address, for example 60, into the register/counter. When JSRP is executed at the following address (32), the return address (33) for the subroutine is pushed onto the stack, and a test is made. If the test passes, the branch address for the subroutine comes from the pipeline register (70); if the test fails, the program jumps to a subroutine at address 60. Each subroutine must have a return instruction (CRTN) at completion that brings execution back to address 33.

I = 6: CJV — COND JUMP VECTOR

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
6	D	$\overline{VECT}$	Pass	NC	NC
6	μPC	$\overline{VECT}$	Fail	NC	NC

X = Don't Care NC = No Change

The Conditional Jump Vector, CJV, instruction is useful for performing interrupt-type branching at the microlevel. During its execution, the $\overline{VECT}$ signal goes true, and can enable another branch-address source. In Fig. A-7, the branch address is supplied by another mapping ROM where interrupt vectors are stored. The source can, of course, be any 3-state buffer or register. The CJV is a conditional instruction, and the branch is only taken if the test passes ($\overline{CC}$ = L). If the test fails, the next microprogram address is supplied by the μPC.

I = 7: JRP — COND JUMP R/PL

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
7	D	$\overline{PL}$	Pass	NC	NC
7	R	$\overline{PL}$	Fail	NC	NC

X = Don't Care NC = No Change

JRP, Conditional Jump, Register/Counter/Pipeline, signifies a conditional branch via the address in the register/counter or the pipeline register; see Fig. A-8. The instruction is similar to I = 5, Conditional Jump to Subroutine, except that no push operation is done. Proper use of JRP assumes that the register/counter is preloaded with a branch address. When JRP is in the pipeline register, a test is made. If the test passes, the next micromemory address comes from the pipeline register. If the test fails, the branch address is supplied by the contents of the register/counter.

I = 8: RFCT — REPEAT LOOP, CNTR ≠ 0

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
8	Stack	$\overline{PL}$	X	≠0	NC
8	μPC	$\overline{PL}$	X	=0	POP

X = Don't Care NC = No Change

The RFCT, Repeat Loop, Counter ≠ 0, instruction utilizes the decrementing feature of the register/counter; see Fig. A-9. Proper use of RFCT requires that the register/counter be preloaded with a count value and that an address be pushed onto the stack. When RFCT is executed, it determines whether the counter has a nonzero value. If it does, the counter is decremented and the next microprogram memory address is taken from the top of the stack. If the counter contains zero, the loop exit condition has been reached and control falls through to the μPC, which supplies the next sequential microprogram address; at the same time the stack is popped; i.e., the stack pointer is decremented.

An example will illustrate how the RFCT can be used to execute a loop (or a specific microinstruction) a fixed number of times. Assume that a loop from address 12 to 18 is to be repeated four times. A push instruction with a 3 in the branch address field is placed at address 11. The count value is always one less than the number of repeats. When the push is executed, the counter is loaded with 3, and the next sequential address, 12, is pushed on top of the stack as the start address of the loop. When the RFCT instruction at address 18 is in the pipeline register, the counter content is tested. If it is not zero, the next address, 12, comes from the top of the stack, and the loop is repeated. When the counter = 0, the program will exit to the next sequential address, 19, held in the microprogram counter. The stack pointer will also be decremented. A total of 4096 loops can be repeated.

I = 9: RPCT — REPEAT PL, CNTR ≠ 0

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
9	D	$\overline{PL}$	X	≠0 DECR	NC
9	μPC	$\overline{PL}$	X	=0 NC	NC

X = Don't Care NC = No Change

The Repeat Pipeline Register, Counter ≠ 0, instruction, RPCT, is similar to I = 8, the Repeat Loop Register instruction, RFCT. The difference is that the branch address comes from the pipeline register rather than the stack file. In addition, no pop is executed when the test condition is met since the stack is not used; see Fig. A-10.

As an example of how the Repeat Pipeline Register instruction works, assume that one single instruction at address 31 is to be repeated 8 times. An LDCT, Load Counter and Continue instruction (I = 12), must be placed at location 30. This instruction loads the register/counter with a specific value, 7 (one less than the repeat value); control then goes to the next sequential address, 31. The RPCT instruction at address 31 tests for a nonzero value in the counter. If the test fails, the counter is decremented and the branch address 31 in the pipeline register is the next address. When counter content is zero, the control falls through to the next sequential address, 32, which now comes from μPC. Multiloop instructions are performed in the same way.

I = A_H: CRTN — COND RETURN

GP502 Instruction	Address Source	Enable Single	$\overline{CC}$	Reg/ Cntr	Stack
A_H	μPC	$\overline{PL}$	Fail	NC	NC
A_H	Stack	$\overline{PL}$	Pass	NC	Pop

NC = No Change

CRTN is a Conditional Return from Subroutine instruction. It provides a means for conditionally returning from a subroutine to the address following the subroutine call; see Fig. A-11.

As an example of instruction operation, assume that a subroutine call (CJS) is executed at micromemory address 62. The return address, 63, is pushed onto the stack and execution continues at the subroutine's start address, for example, 80. The subroutine ends at address 88, but a CRTN instruction is located at address 84. A test is made, and if it fails, execution continues at the next sequential address, 85. If the test passes, the return address, 63, is popped from the stack and the stack pointer is decremented, whereupon normal program flow continues from address 63. If the test had failed at address 84, an unconditional return would have to be executed at the subroutine's last address, 88. The CRTN instruction could be used here again by programming input $\overline{CCEN}$ high. This programming has the effect of forcing a true condition or passing test.

I = B_H: CJPP — COND JUMP PL and POP

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
B_H	μPC	$\overline{PL}$	Fail	NC	NC
B_H	D	$\overline{PL}$	Pass	NC	NC

NC = No Change

The CJPP, Conditional Jump Pipeline and Pop, instruction is used to exit from a loop that uses the stack; see Fig. A-12. A typical example would be the testing of several inputs in a microprogram loop, and waiting for one of them to occur before proceeding to another program section.

Assume that the program loops between addresses 40 and 44, and that CJPP instructions are located at addresses 42 and 43. A push instruction must be located at address 3F; this instruction pushes the return address 40 onto the stack. At address 42, the CJPP instruction tests the $\overline{CC}$ input. If the test fails, the next sequential instruction is executed at 43. The same test is made again, and if it fails, the next instruction at 44 (LOOP) returns the flow to address 40, and another loop is started. However, should one test pass, at any time, the next address is taken from the branch value in the pipeline. At the same time the stack is properly maintained by a pop. This technique allows a jump table to be set up at the firmware level.

I = C_H: LDCT — LD CNTR and CONTINUE

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
C_H	μPC	$\overline{PL}$	X	Load	NC

NC = No Change

The Load Counter and Continue instruction, LDCT, simply allows the counter to be loaded with a value at its parallel inputs. As shown in Fig. A-13, this input can be supplied from the branch address field in the pipeline register. The field may contain either a counter value or a branch address. Execution continues, with the next instruction determined by the control of the μPC.

The counter may be loaded explicitly by instruction I = C_H, conditionally by I = 4, or along with any instruction by using the $\overline{RLD}$ input. If the RLD line is held low, any count or decrement operation called for by an instruction is overridden and the counter is loaded.

I = D_H: LOOP — TEST END LOOP

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
D_H	Stack	$\overline{PL}$	Fail	NC	NC
D_H	μPC	$\overline{PL}$	Pass	NC	Pop

NC = No Change

The Test End-of-Loop instruction provides a means for conditionally exiting from the bottom of a loop; see Fig. A-14.

Assume a loop programmed between addresses 36 and 40. The return address, 36, must have been pushed onto the stack by a push instruction located at address 35. When the Loop instruction is reached at address 40, a test is made. If the test fails, the next address is taken from the top of the stack (36). If the test passes, the stack is popped, for proper maintenance, and the program continues with the next sequential instruction located at address 41.

I = E_H: CONT — CONTINUE

GP502 Instruction	Address Source	Enable Signal	$\overline{CC}$	Reg/ Cntr	Stack
E_H	μPC	$\overline{PL}$	X	NC	NC

NC = No Change

As Fig. A-15 shows, the CONT, Continue, instruction is a simple instruction that causes the microprogram counter to increment, so that the next sequential microinstruction is executed.

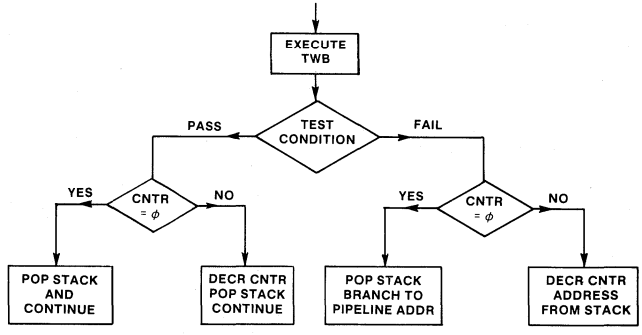
I = F_H: TWB — THREE-WAY BRANCH

The Three-Way Branch instruction, TWB, tests both a data-dependent condition and the counter during one microinstruction, and provides for the selection of one of three microinstruction addresses as the next microinstruction to be executed; see Fig. A-16.

The TWB is similar to instruction I = 8 in the sense that a return address must first be pushed onto the stack and the register/counter loaded with a count value. When the TWB instruction is reached, a test is made. If the test fails and the contents of the counter is nonzero, the counter is decremented and the next address is taken from the top of the stack. This action continues until the count reaches zero, then the next address comes from the branch field in the pipeline register.

If at any time the test passes during the execution of I = F_H, the microprogram counter furnishes the next address. If at any time the loop is exited, either by the count becoming zero, or by passing the test, the stack is popped; i.e., the stack pointer is decremented. This instruction is useful when a time-out function is required. Typical examples of the use of the instruction would be normalization of a floating-point number or a machine-level memory-search instruction which should be terminated either by finding the contents of a desired memory location or by reaching the search limit.

Fig. 3 shows a flowchart for alternatives leading to three different branch addresses.



GP502 Instr	Address Source	Enable	Reg/ CC	Cntr	Stack
F_H	μPC	$\overline{PL}$	Pass	≠0 Decr	Pop
F_H	μPC	$\overline{PL}$	Pass	=0 NC	Pop
F_H	Stack	$\overline{PL}$	Fail	≠0 Decr	NC
F_H	D	$\overline{PL}$	Fail	=0 Decr	Pop

Fig. 3 - Flowchart of alternatives leading to different branch addresses.

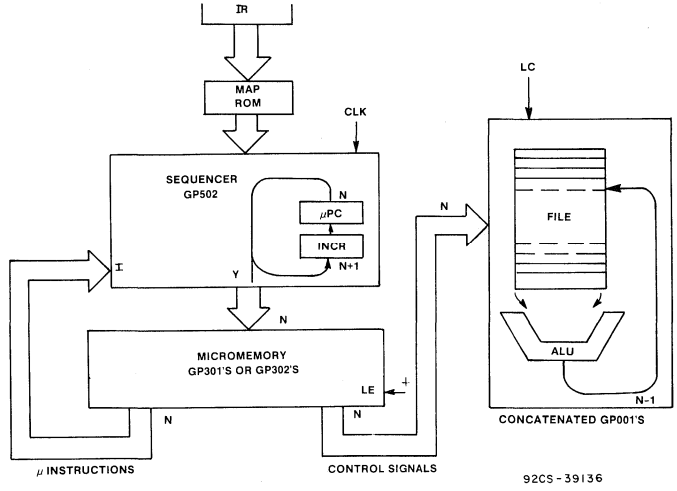
SYSTEM OPERATION

Pipeline Versus Nonpipeline Operation

The GP502 sequencer represents a state machine and can, with a control store, be programmed as a stand-alone system for a great number of complex high-speed controller applications. The most typical application for a microprogrammed control section is, however, as a controller for a minicomputer. The function of the microprogrammed controller is then to fetch and execute machine-level instructions. It is important to keep in mind the distinction between microinstructions in micromemory and machine-level instructions in main or program memory.

Fig. 4 shows a very basic structure of a control section and an execution section in a mini/micro computer. The control unit simply fetches machine instructions and decodes them so that the original instructions can be executed. This cycle of fetch and execute is repeated over and over again. There are many ways to implement the fundamental structure shown in Fig. 4, and within the overall machine architecture, the control section can also be designed in a number of ways. A major effect on overall system performance is obtained with a pipeline register in the control unit.

Consider first the case of a simple micromemory, for example one built from the GP302 (256 x 16), where the



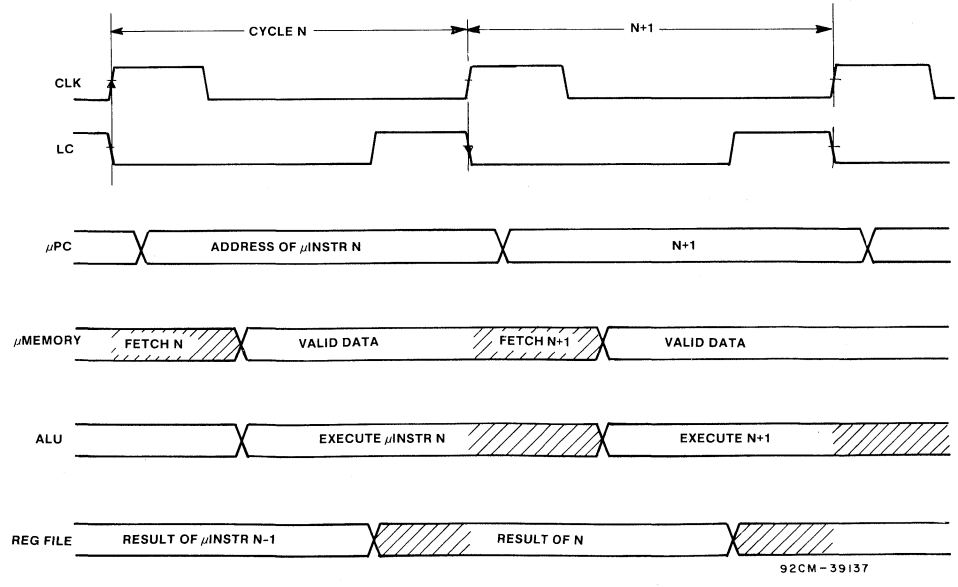


Fig. 4 - Basic structure of a control section and an execution section in a mini/micro computer.

latch enable input is held high so that the memory is transparent. The timing diagram (Fig. 4) shows that in an arbitrary cycle, N, the contents of the microprogram counter address the micromemory and, some time later in the cycle, data is valid on the output. The micromemory's output controls the GP001s and executes microinstruction N. For example, two operands are read from the register file and added. When the GP001's clock goes low at the end of the cycle, the result is stored in one of the registers. The microprogram counter now issues a new address (N+1) and operation continues. The important thing to notice is that the data paths of the control section and the ALU are in series. The ALU is idle temporarily and must wait for command N from the control section before it can execute that command. The same microinstruction N is fetched and executed in the same basic cycle.

Contrast the operation just described with the system in Fig. 5. The only difference is in the micromemory which, using GP305s (512 x 16), has on-chip an edge-triggered register at the output. On the rising edge of the clock, valid data from the memory is clocked into the register. The register contents cannot be changed until the next clock edge, thus permitting a new microinstruction to be fetched while the previous one, now in the register, provides control bits to the bit-slices of the GP001. The timing diagram shows that while microinstruction N is in the pipeline register and is being executed, the next microinstruction, N+1, is being fetched, and the result of the previous one, N-1, is being stored. This overlap of fetch and execute phases is vital for increased throughput in the system.

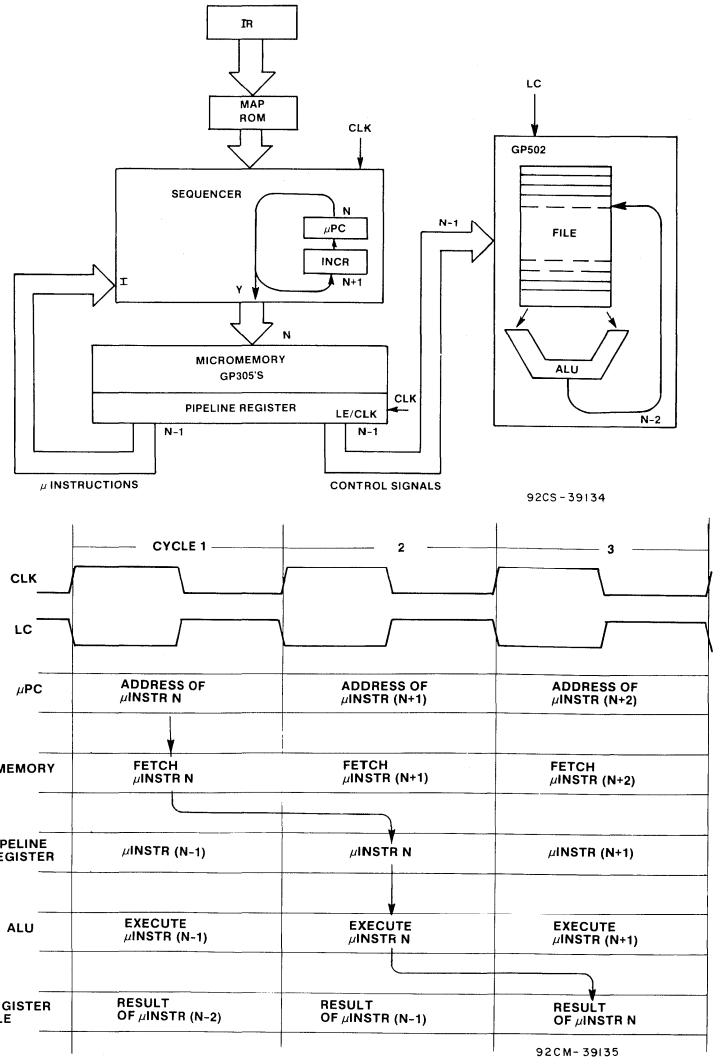


Fig. 5 - Variation of the basic structure of Fig. 4 using a micromemory with an on-chip edge-triggered register at the output.

DESIGN EXAMPLE

An actual design of a system illustrating the use of the GP502 sequencer in a microprogrammable control section that employs GP305s in the control store with an on-chip pipeline register is shown in Fig. 6. The overall system is tied together with MSI parts from the RCA HC line of high-speed CMOS parts. These parts restrict the system to 5-volt operation, which does not permit exploitation of the speed capabilities of the EPIC family (GP) ICs. However, the principles and approaches are independent of the chosen V_{DD} voltage.

The microprogram memory is arranged so that the 12 leftmost bits are the branch address field, which is enabled by the $\overline{PL}$ signal to a 3-state input. The rest of the control bits in the pipeline register are permanently enabled. Notice that the status information from the ALU (or other resources) is also clocked into an output register, part of the condition-code multiplexer.

Fig. 7 shows a timing diagram for this architecture applicable to the control section. At the rising clock edge new data is entered into the pipeline register. After a short delay, three bits address the condition-code multiplexer, and after another delay, valid data is input to $\overline{CC}$. Following a delay through the sequencer ($\overline{CC}$ → Y), the micromemory is addressed. The access time of the micromemory plus the set-up time of the pipeline register determines how early the next clock pulse can be applied. (Set-up time for the pipeline applies strictly only where a dedicated IC is used. Where the register is on-chip, memory access time includes this time.)

Determination of the worst-case cycle time for the control section is only half of the story. The longest delay path through the execution portion of the cycle must also be considered. In the architecture under discussion, the result of an ALU execution must be available before the next clock edge arrives. The two data paths are in parallel; the longest determines the minimum cycle time in system operation.

A specific example of how the GP502 can be initialized and programmed to implement two machine instructions, LDI (Load Immediate) and ADD, is shown in the Coding Table, Appendix B.

The hardware forces the output of the sequencer to address FFF, the location of the JZ instruction. This action initializes the output address Y and sets the microprogram counter to zero. The Continue instruction (I = E_H) is at address zero, and the program goes to the first microword of the fetch sequence. During fetch, the memory address register is loaded and the contents of the addressed main memory location are loaded into the instruction register. The main program counter is also updated. At micromemory address 3, a JMAP instruction is executed, enabling the mapping ROM's output, which is 4. This address is the start address of the decoded machine instruction if LDI is the first instruction in the main program.

Two more Continue instructions step the sequencer until CJP is encountered at micromemory address 6. The I = 7 instruction is conditional, but since $\overline{CCEN}$ is programmed high, the $\overline{CC}$ input is ignored and the GP502 operates as though $\overline{CC}$ were true. The next sequencer output is taken from the pipeline (Y = 01), which initiates another fetch sequence. All execution sequences in this example end with a forced CJP instruction that branches to another fetch operation.

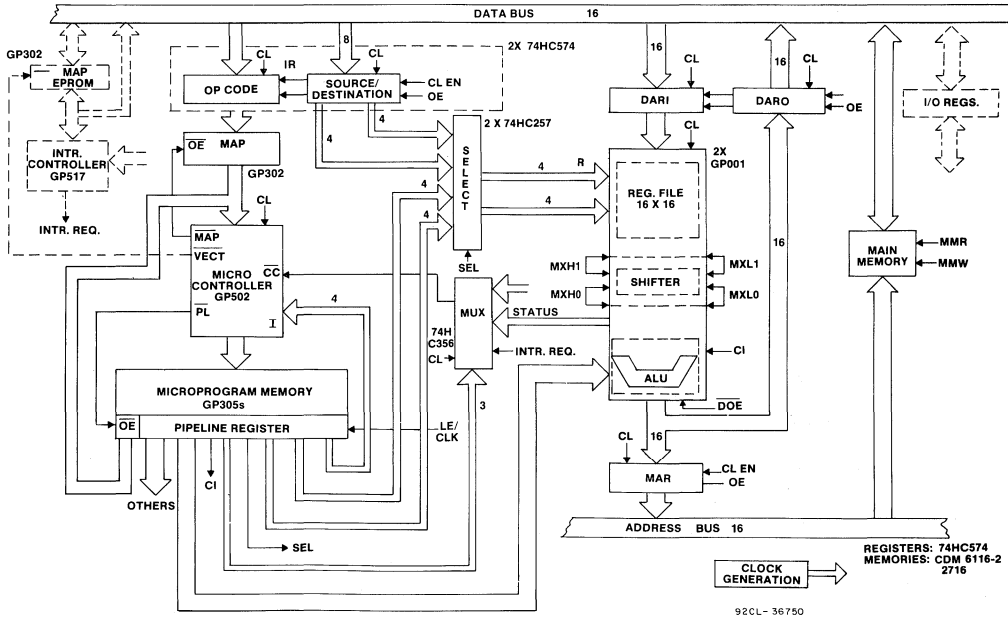
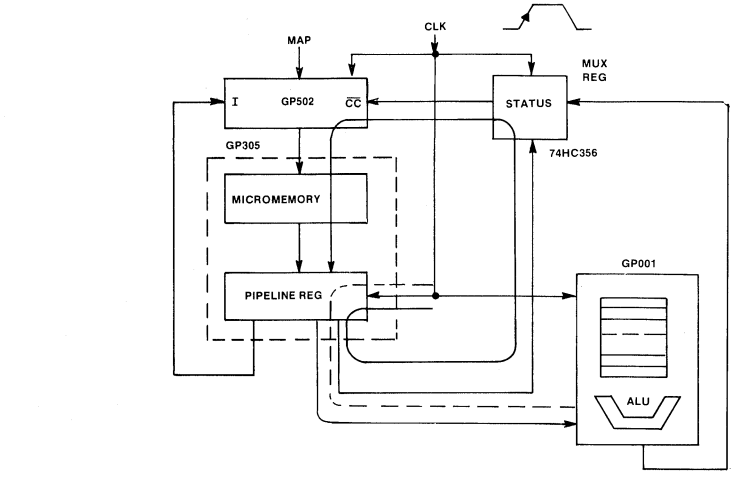


Fig. 6 - A 16-bit microprogrammable bit-slice microcomputer.



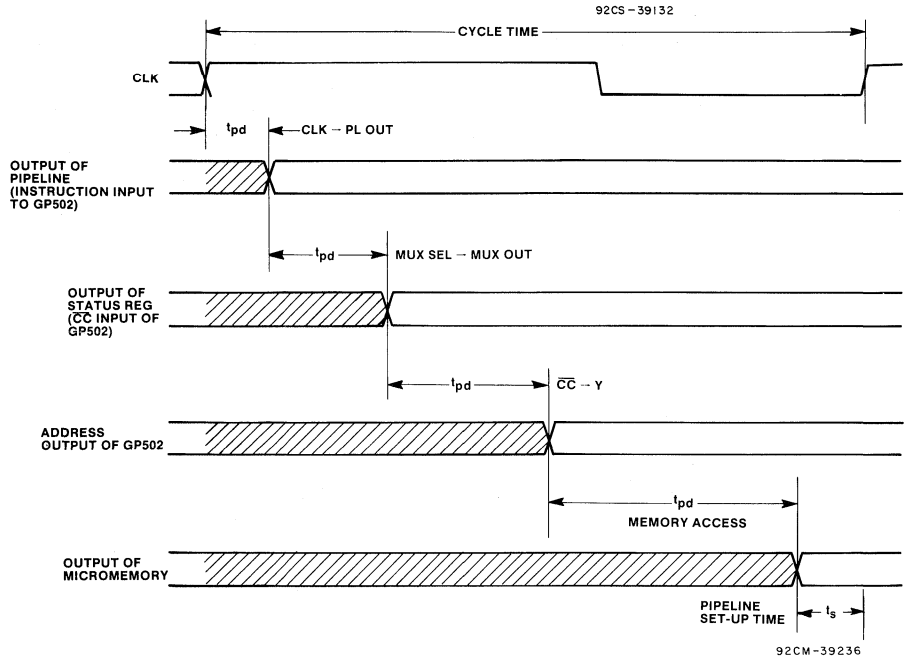


Fig. 7 - Timing diagram for the control section of the architecture of Fig. 6.

MICROCYCLE TIMING ANALYSIS

The performance of any control unit for a given sequencer is determined by its speed of operation. A primary objective is always to determine the minimum clock period or maximum clock rate for a given design. Each design is different and requires detailed analysis. The speed is determined from timing of the individual components in the design. Note that maximum or worst-case delay times and set-up times should always be used.

The fundamental approach to analysis is straightforward: find all paths from one defined start point, for example the pipeline register, and back to the same register; then calculate the path time using worst-case numbers. The longest path determines the minimum clock period. It is evident from a study of the GP502 instruction set that there are a great number of different delay paths through the sequencer itself. With a little experience, the longest route can be found quickly.

The architecture of Fig. 8 can be used to demonstrate the general analytical approach. Assume that the delay through the IR register, the access time and output enable time of the mapping ROM, the access time of micromemory to clock input and delay from clock to pipeline output, and all the delay paths through the sequencer, depending on the selected instruction, are known. Assume further that the same clock is used and that changes occur on the low-to-high transition of the clock. The problem now is to identify the flow between clock transitions.

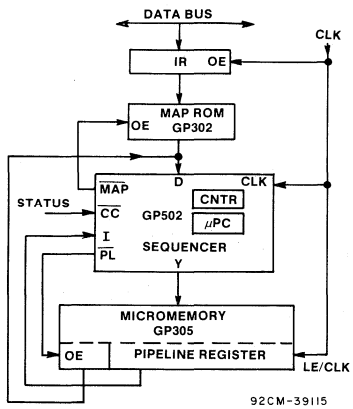


Fig. 8 - Block diagram demonstrating the general analytical approach to microcycle timing.

Typically, a cycle is started by a clock edge at one device, for example the pipeline register. The signals begin to flow from one device to the next until a set-up time for the next clock edge results. Then the next microinstruction occurs. A Pert-chart type of timing analysis is useful; this method is illustrated in Fig. 9 for two instruction only, Continue and Jump Map. Similar charts could be drawn for other instructions.

Consider first the Continue instruction on the right-hand side. Timing starts when a word is clocked into the pipeline. After a short delay the data is available at the output of the register, and the GP502's instruction I is available. The sequencer generates a new micromemory address, and after an access time in the GP305, the new microword is ready to be clocked into the pipeline on the next clock edge. In parallel is a path that includes set-up time for the microinstruction program counter. If Continue instructions are executed sequentially, the delay path includes only CLK → Y and the access time of the micromemory.

Next consider the control section when the Jump Map instruction is used. The pipeline register is clocked and JMAP is input to the sequencer, generating the MAP enable signal after a delay. The contents of the addressed map ROM are available after another delay at the D input of the sequencer. This is the micromemory address Y after some time. Then, after the GP305's access time, new data is ready to be strobed into the pipeline register.

For each identified path, the delays are added; the longest path determines the minimum clock period.

Note that this calculation represents only the worst-case period for the control unit, and that the final system cycle time depends upon the rest of the hardware. A similar analysis should be made for the ALU portion of the system.

The analysis above assumes that the minimum clock period is based on the longest propagation path. A technique frequently used is to microprogram the clock so that the period can be stretched for slow instructions. When these slow instructions occur infrequently, a substantial increase in throughput is achieved.

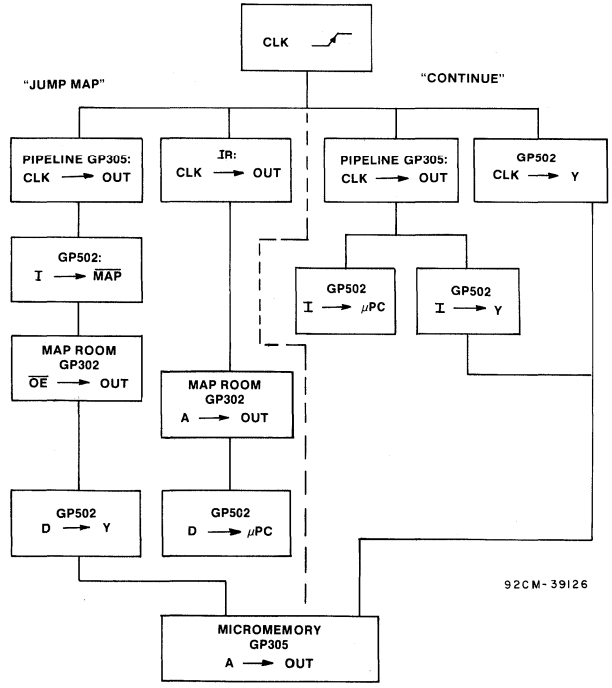


Fig. 9 - Pert-chart type of timing analysis.

APPENDIX A
INSTRUCTION DATA-FLOW DIAGRAMS

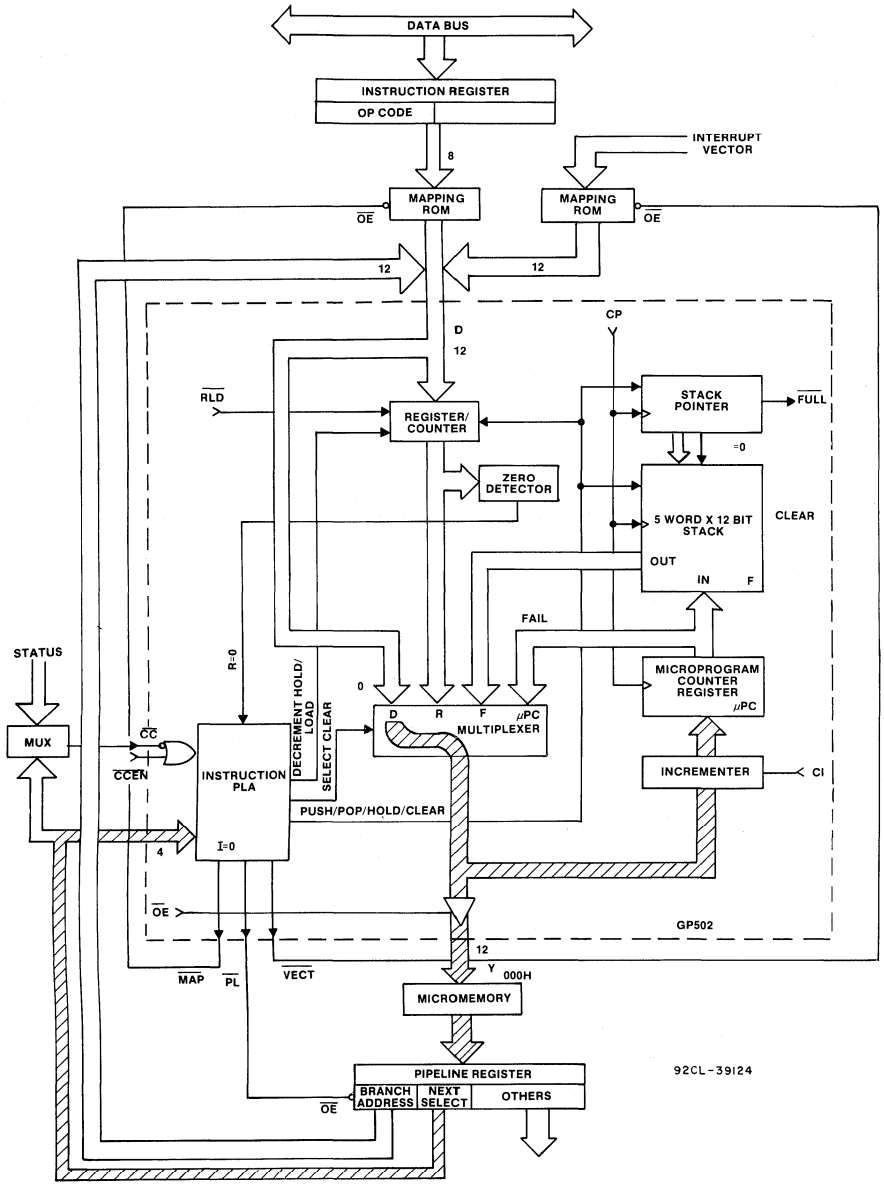


Fig. A-1 - Data flow diagram for the Jump Zero, JZ, instruction.

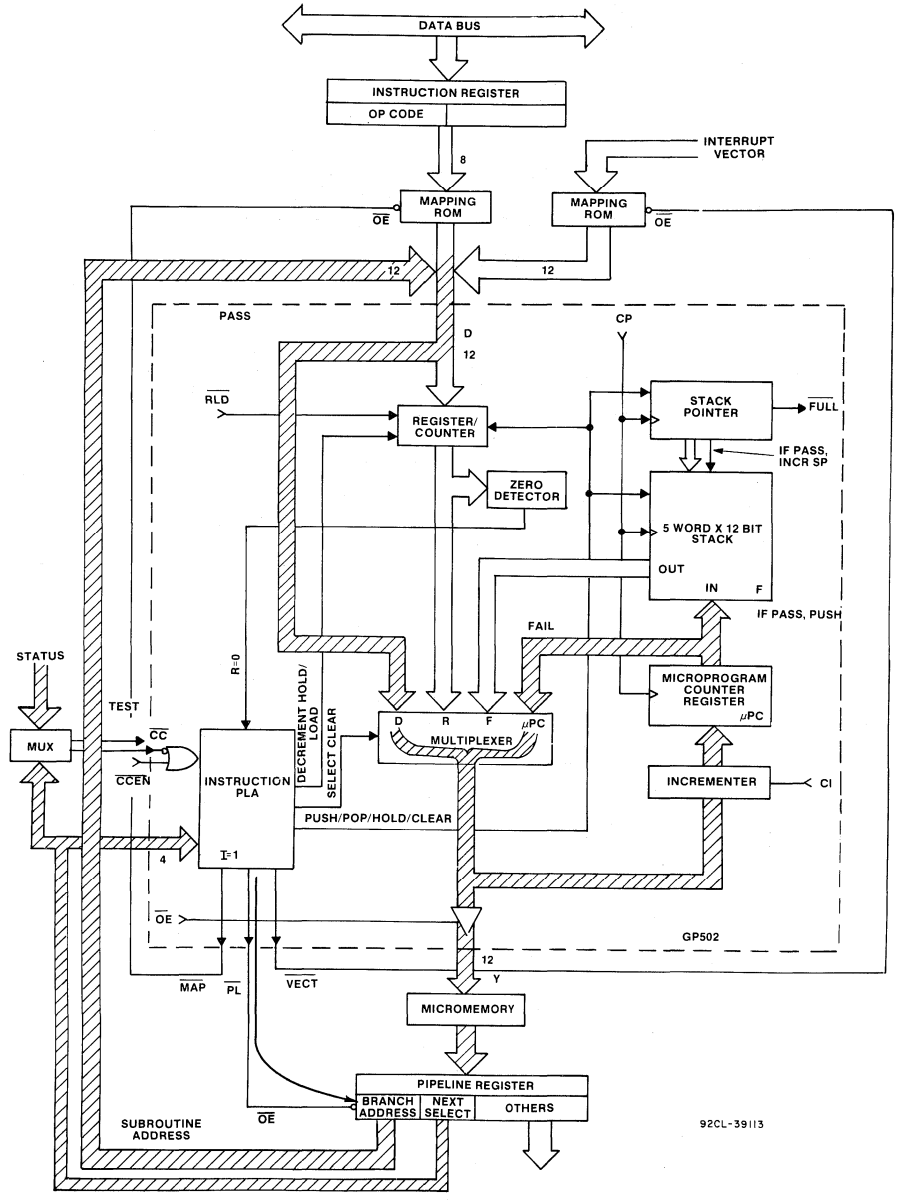


Fig. A-2 - Data flow diagram for the Conditional Jump to Subroutine, Pipeline, COND JSB PL, CJS, instruction.

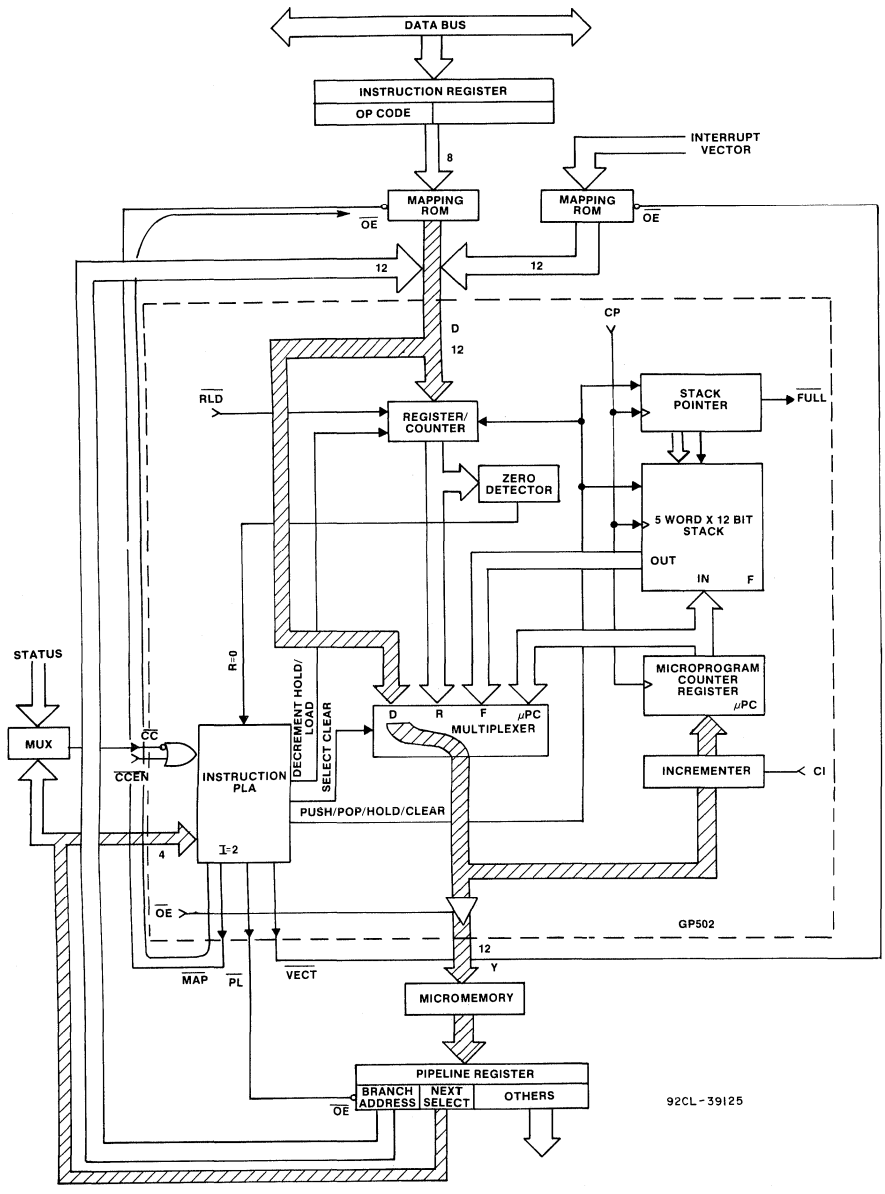


Fig. A-3 - Data flow diagram for the Jump Map, JMAP, instruction.

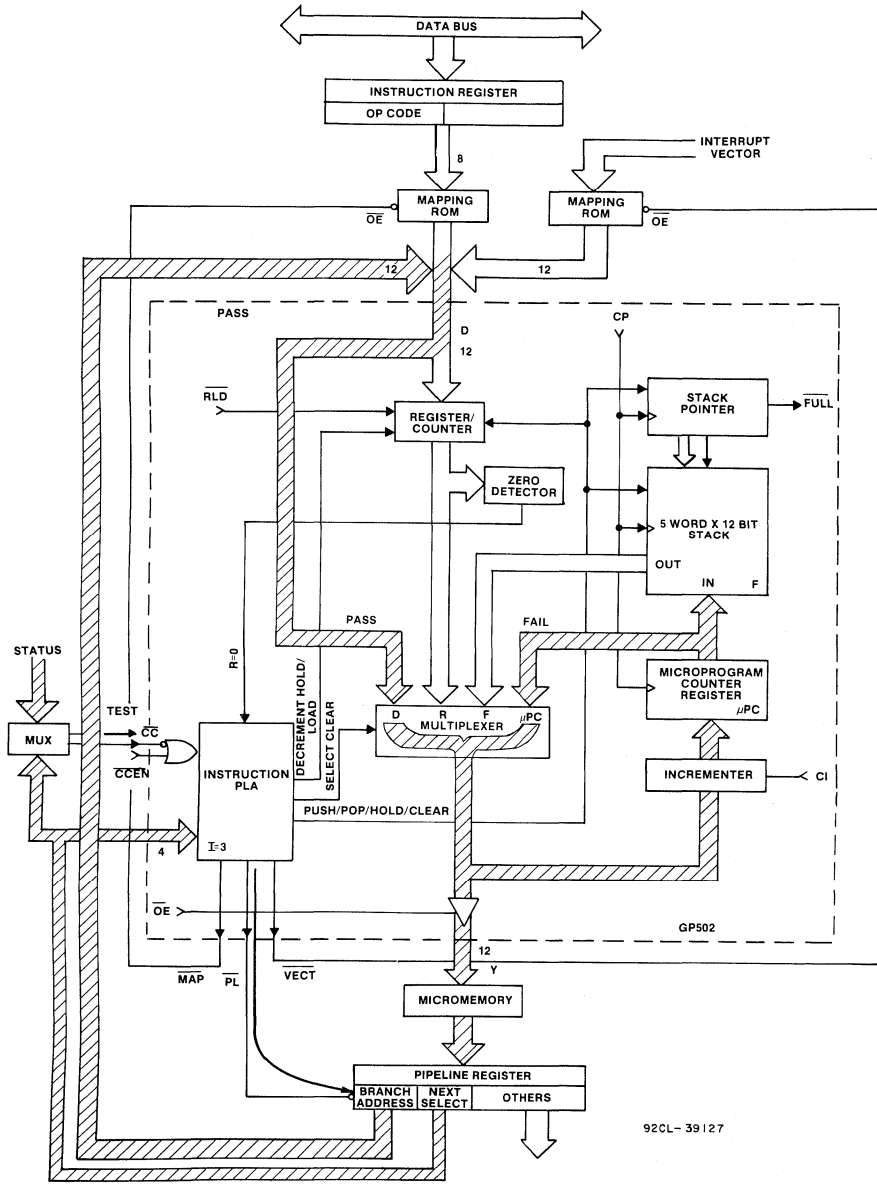


Fig. A-4 - Data flow diagram for the Conditional Jump Pipeline, COND JUMP PL, CJP, instruction.

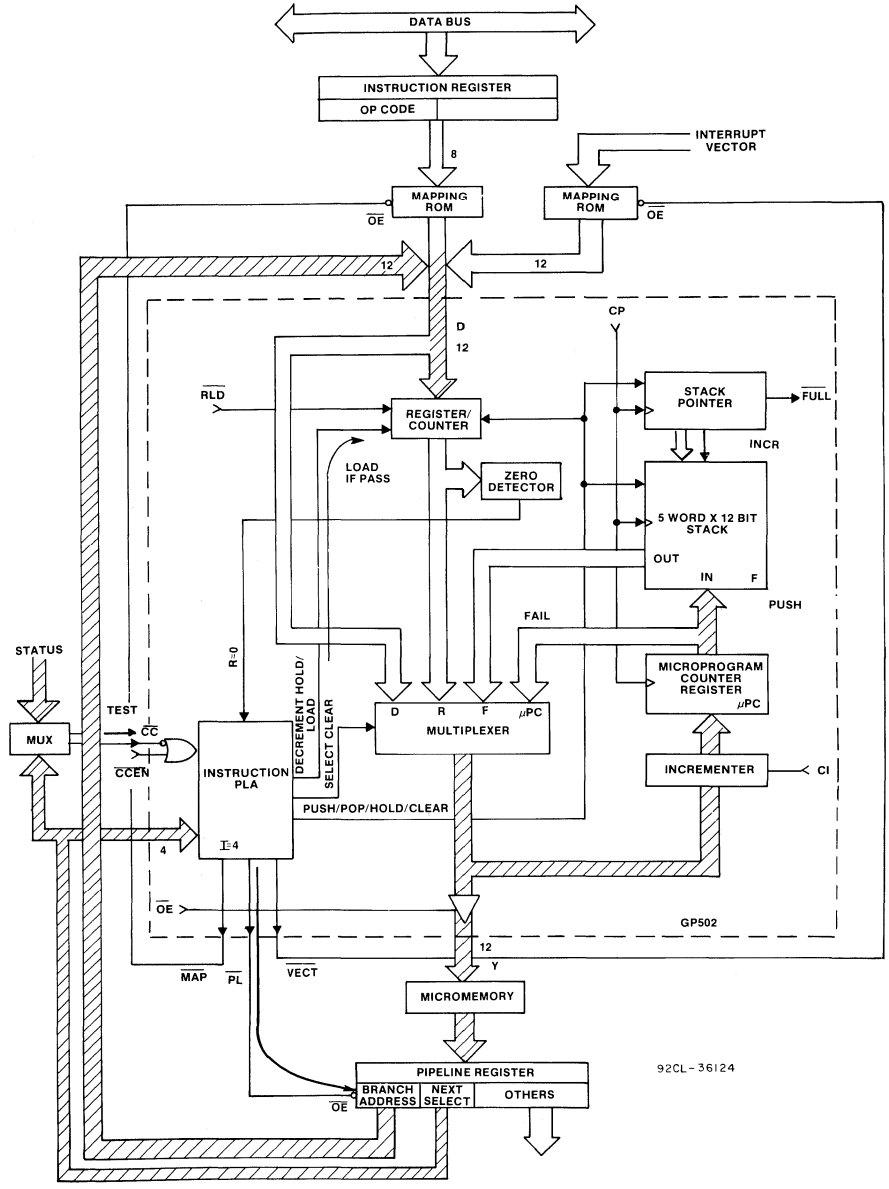


Fig. A-5 - Data flow diagram for the Push/Conditional Load Counter, PUSH/COND LD CNTR, PUSH, instruction.

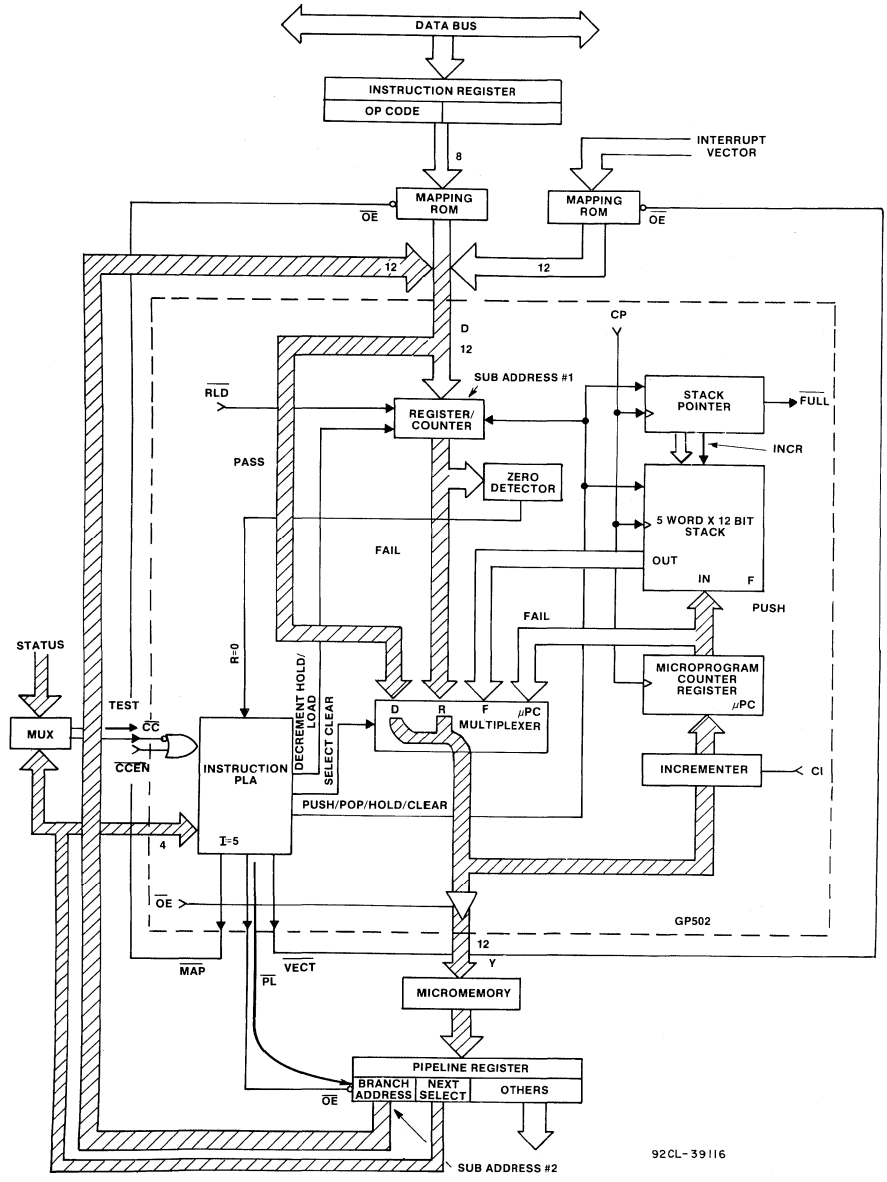


Fig. A-6 - Data flow diagram for the Conditional Jump to Subroutine Register/Counter/Pipeline, COND JSB R/PL, JSRP, instruction.

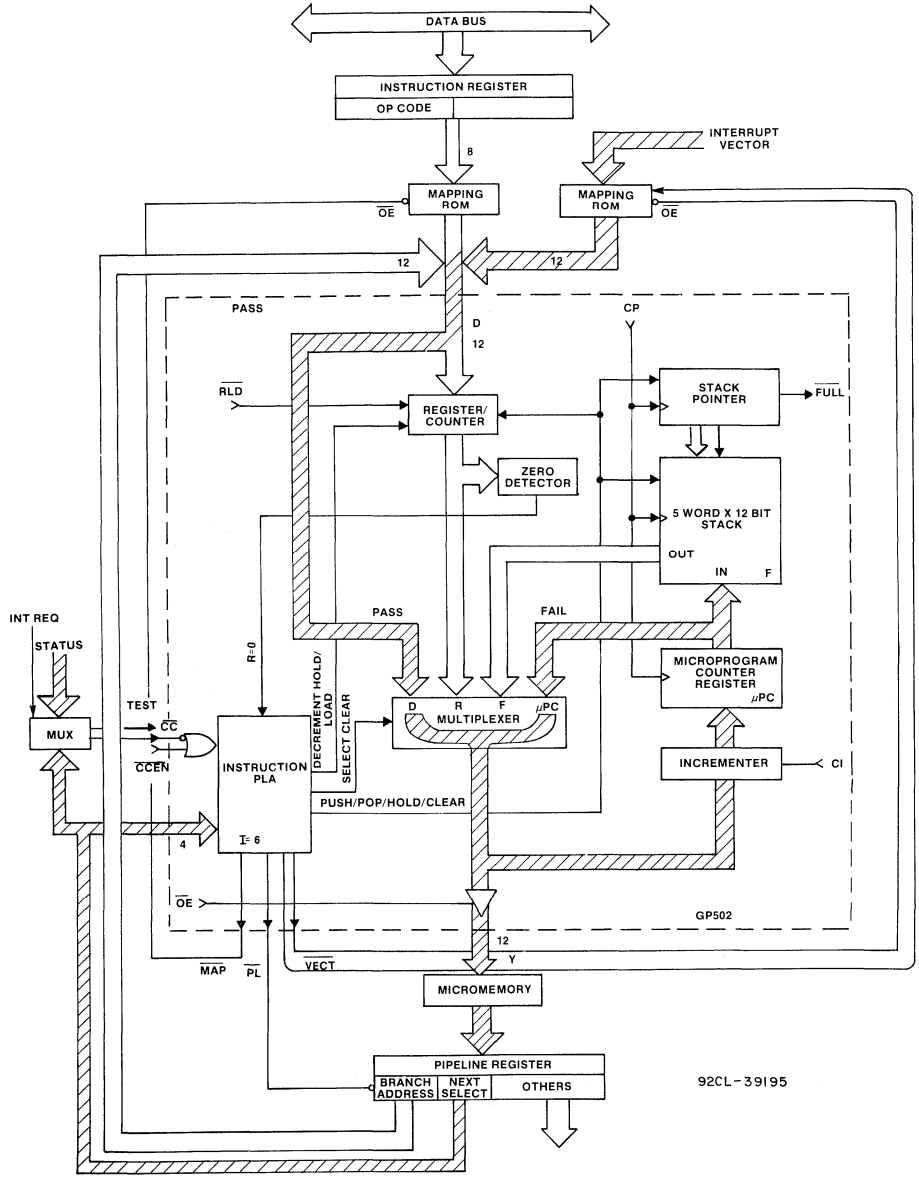


Fig. A-7 - Data flow diagram for the Conditional Jump Vector, COND JUMP VECTOR, CJV, instruction.

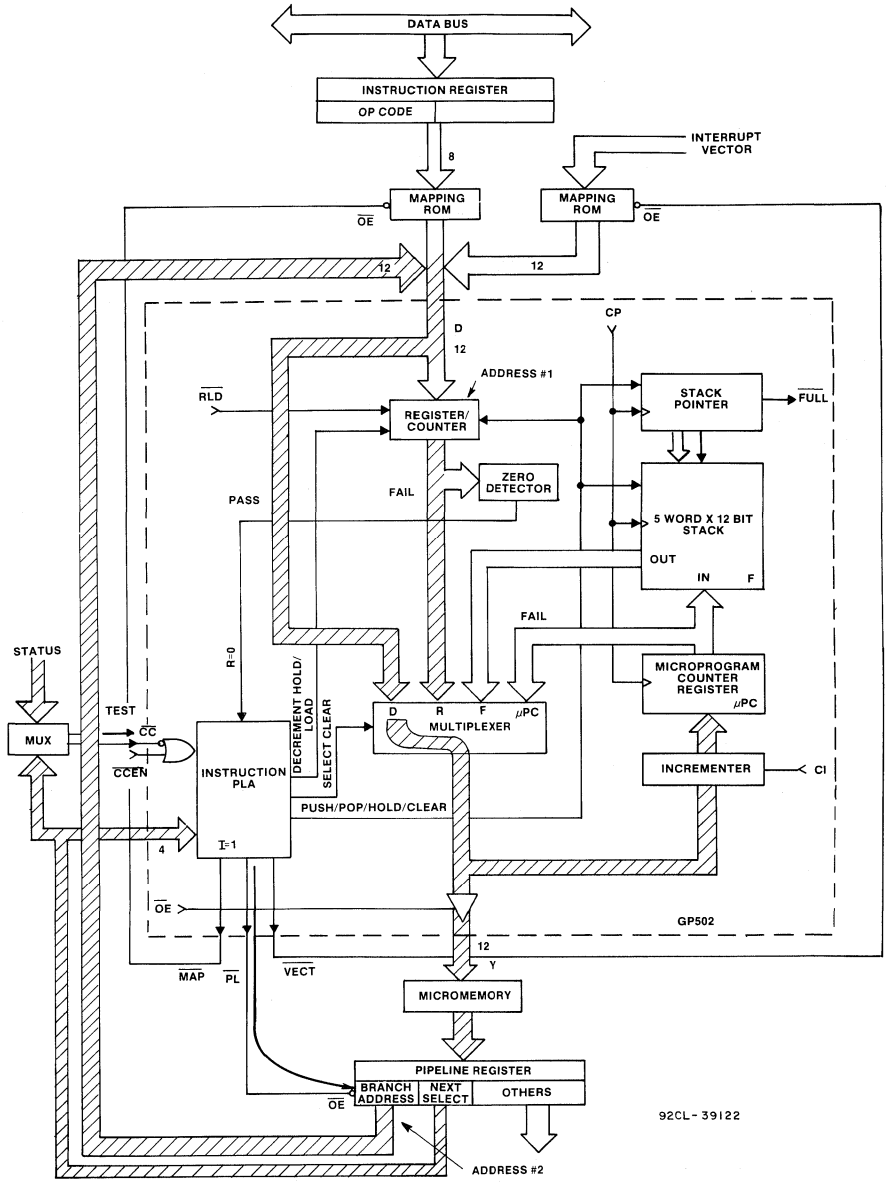


Fig. A-8 - Data flow diagram for the Conditional Jump Register/Counter/Pipeline, COND JUMP R/PL, JRP, instruction.

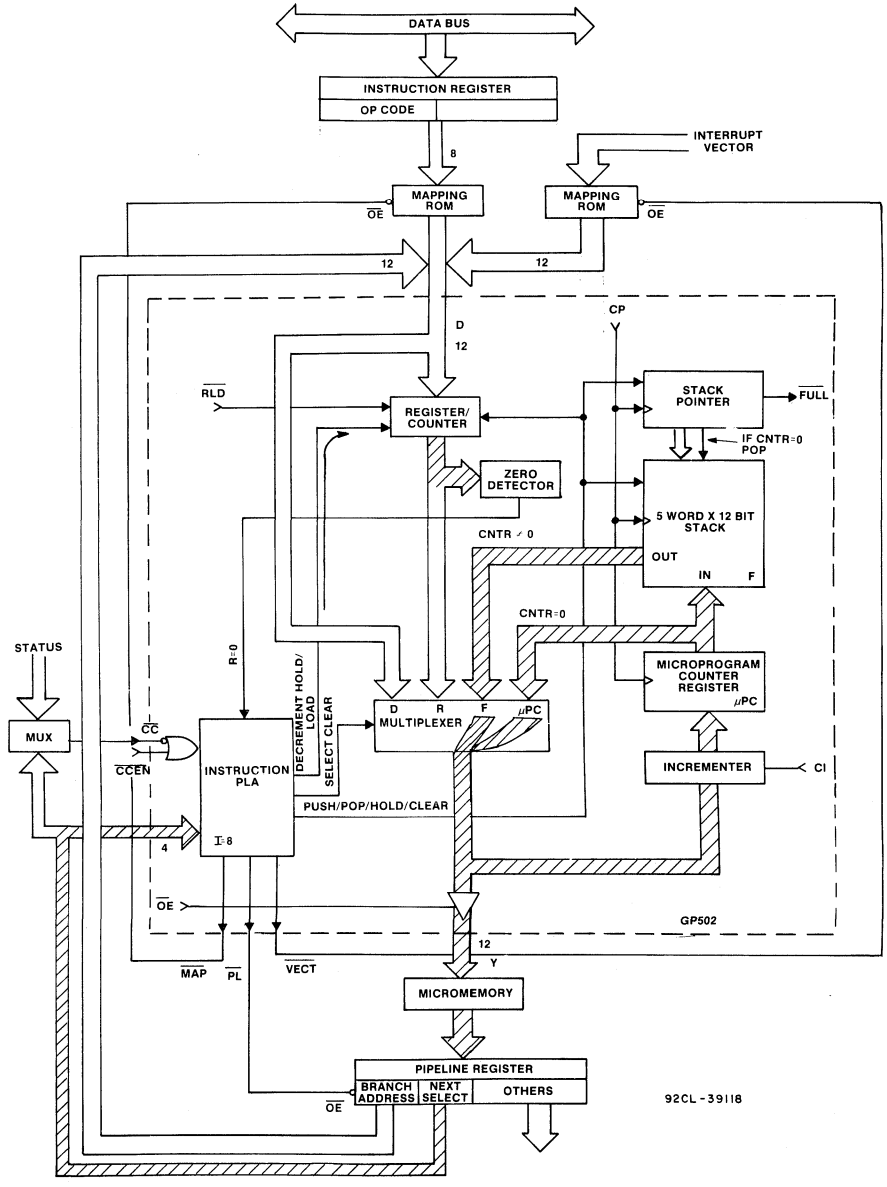


Fig. A-9 - Data flow diagram for the Repeat Loop, Counter=0, REPEAT LOOP, CNTR=0, RFCT, instruction.

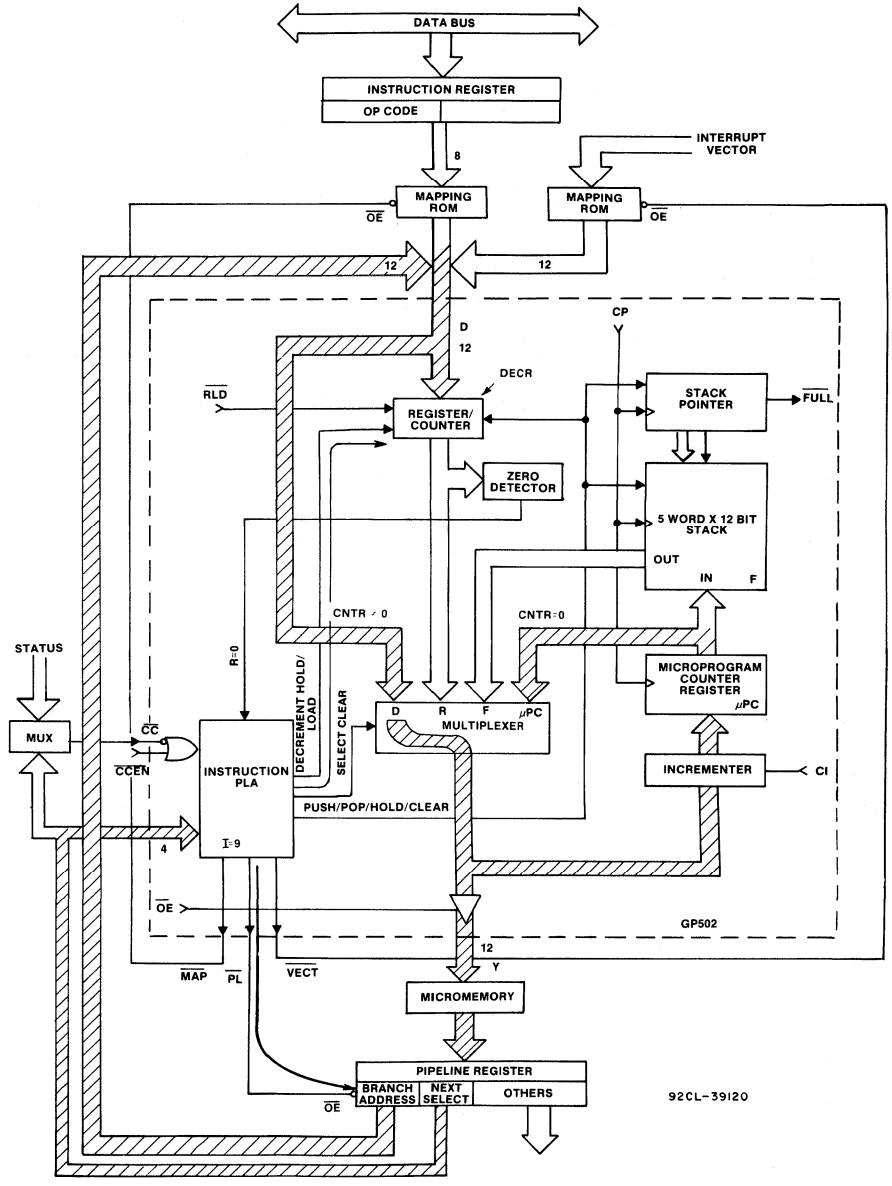


Fig. A-10 - Data flow diagram for the Repeat Pipeline Register, Counter=0, REPEAT PL, CNTR=0, RPCT, instruction.

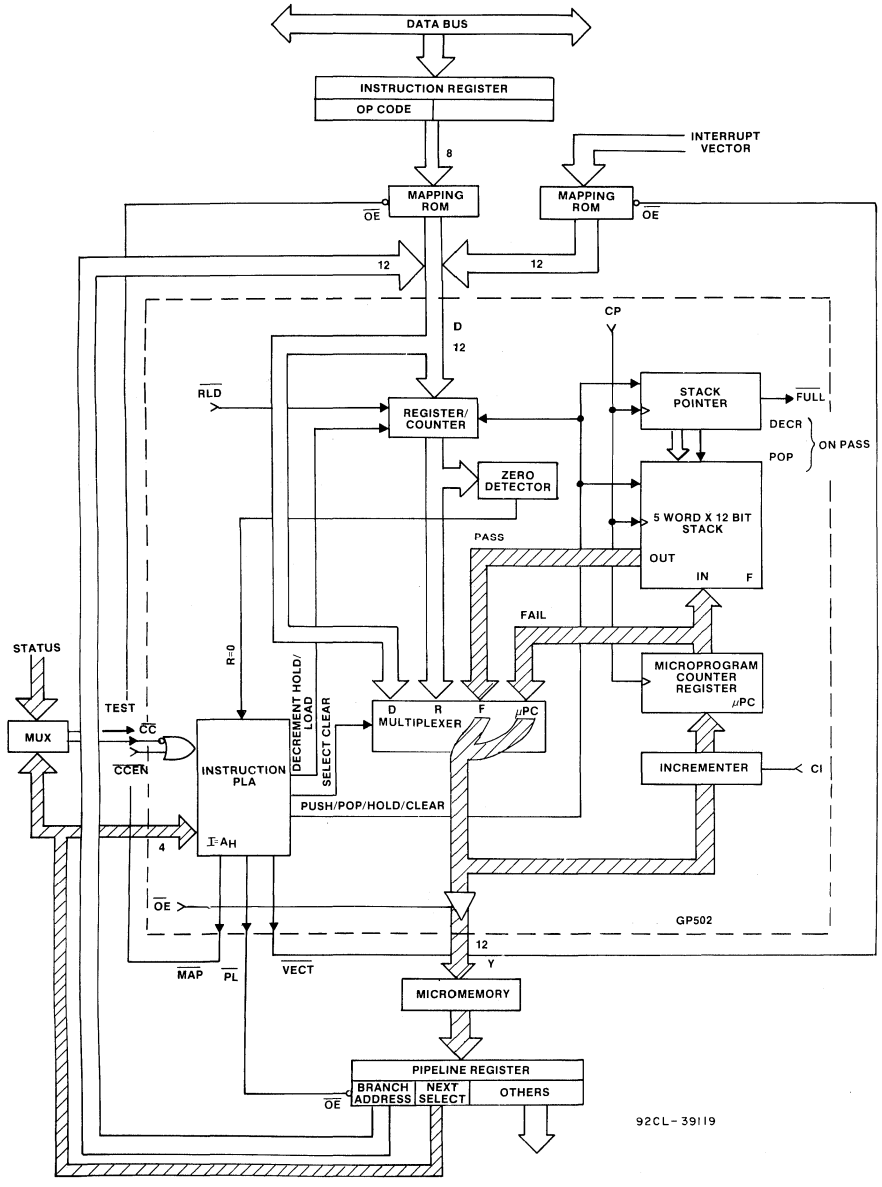


Fig. A-11 - Data flow diagram for the Conditional Return from Subroutine, COND RETURN, CRTN, instruction.

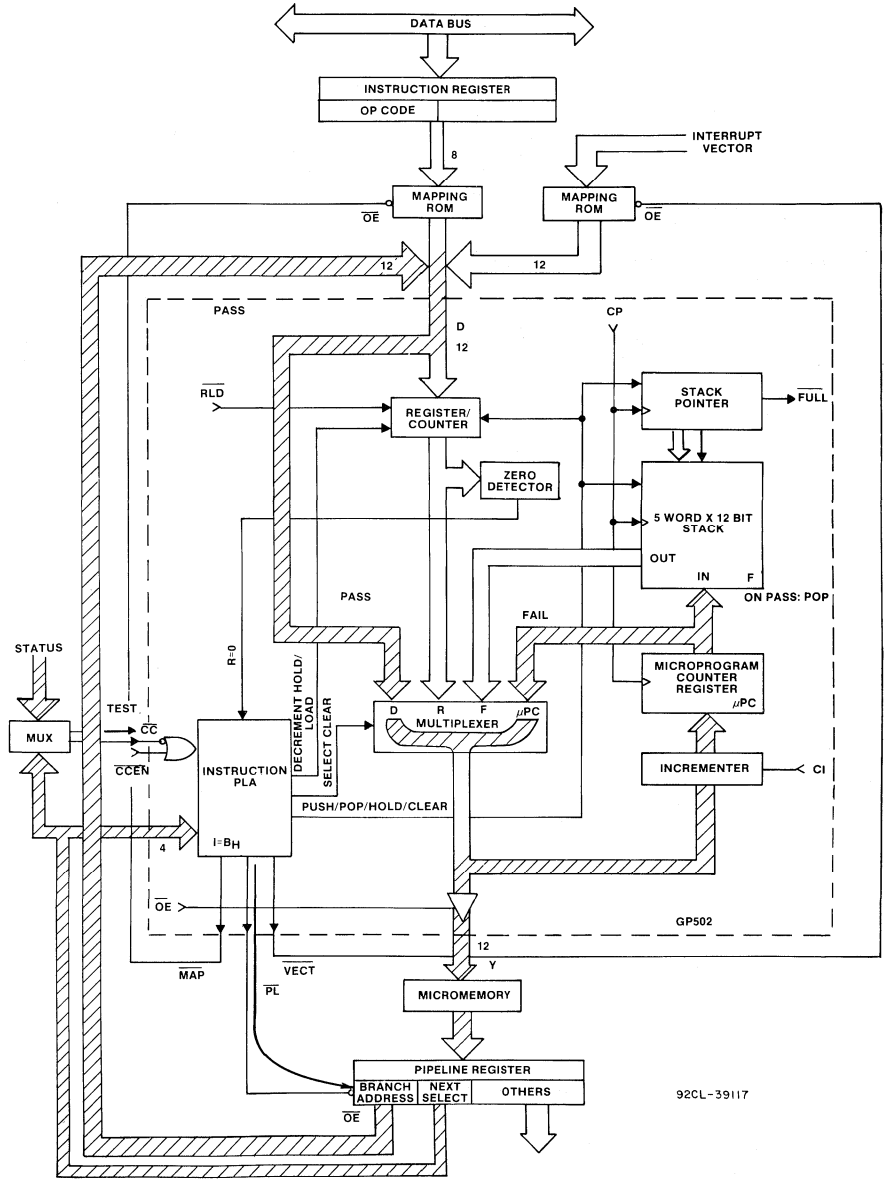


Fig. A-12 - Data flow diagram for the Conditional Jump Pipeline and Pop, COND JUMP PL and POP, CJPP, instruction.

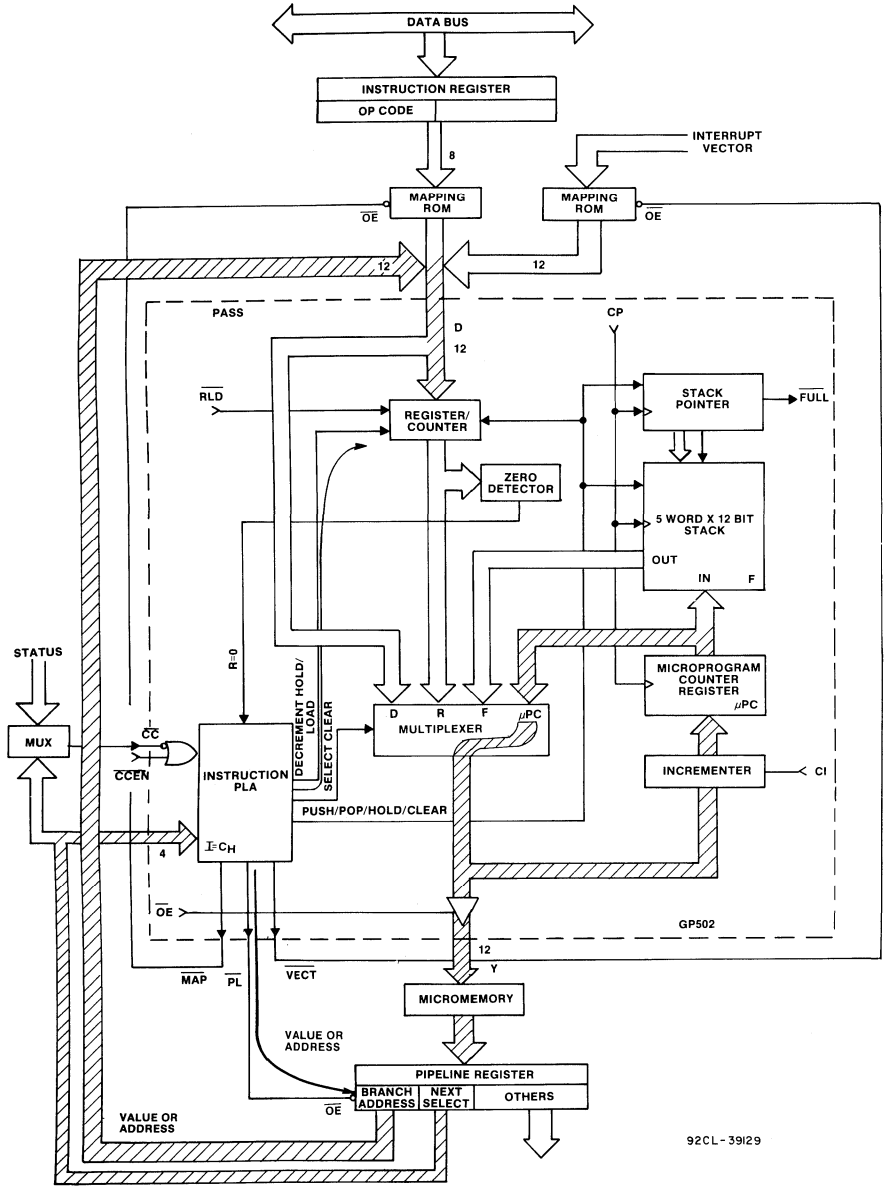


Fig. A-13 - Data flow diagram for the Load Counter and Continue, LD CNTR and CONTINUE, LDCT, instruction.

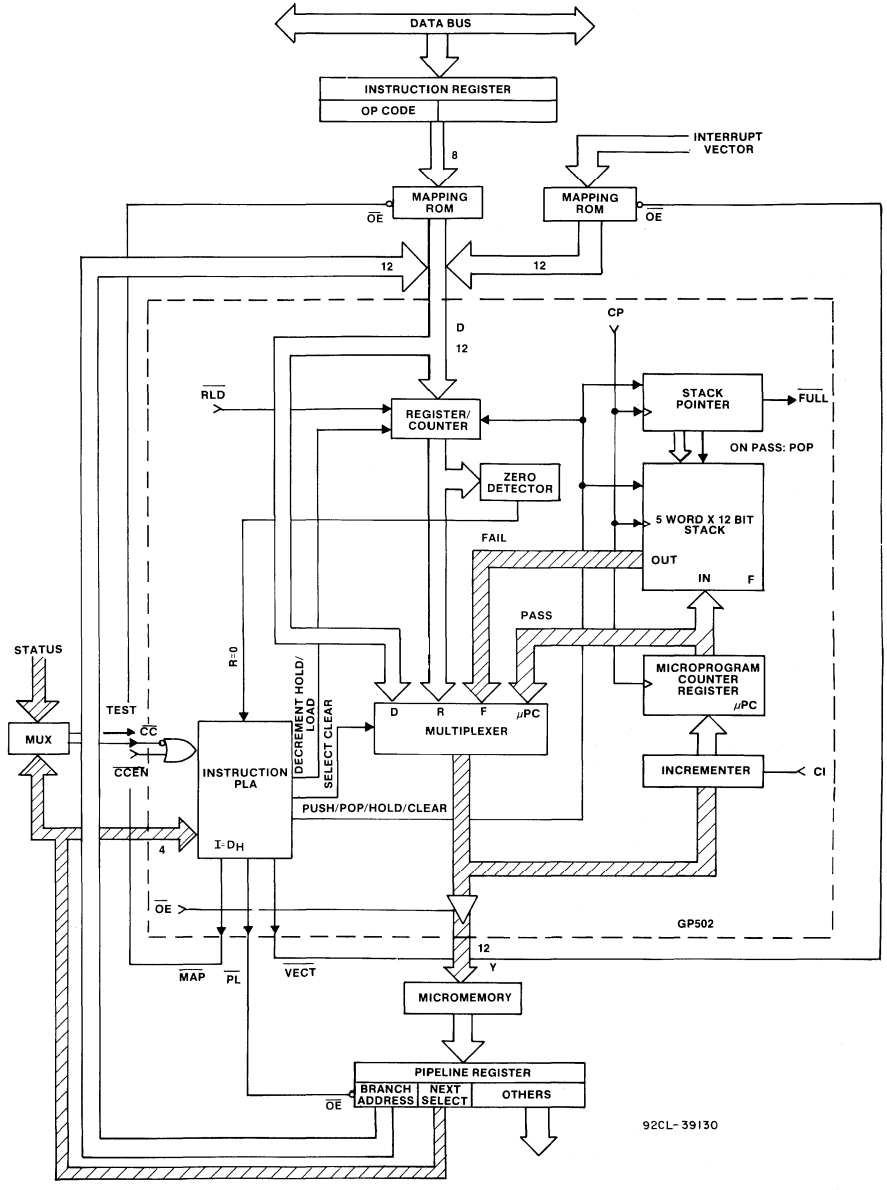


Fig. A-14 - Data flow diagram for the Test End of Loop, TEST END LOOP, instruction.

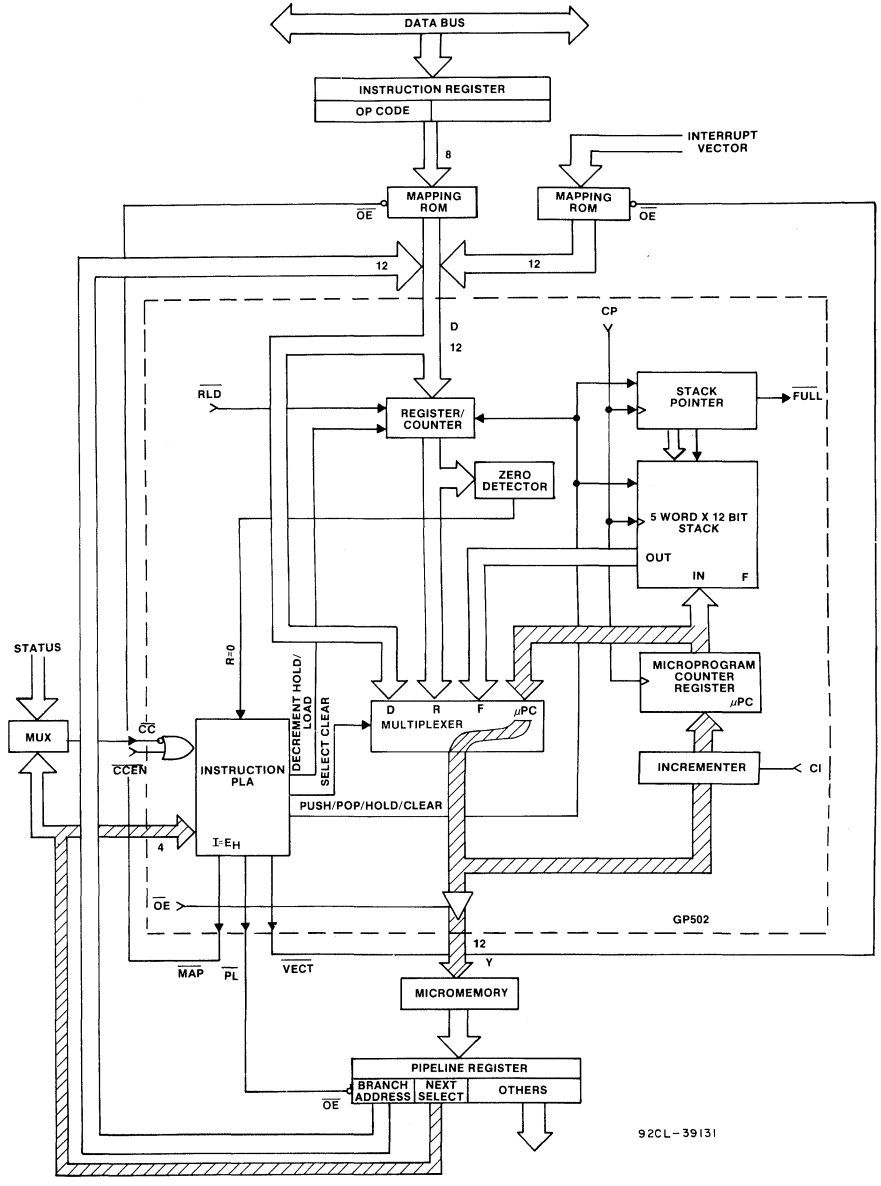


Fig. A-15 - Data flow diagram for the Continue, CONT, instruction.

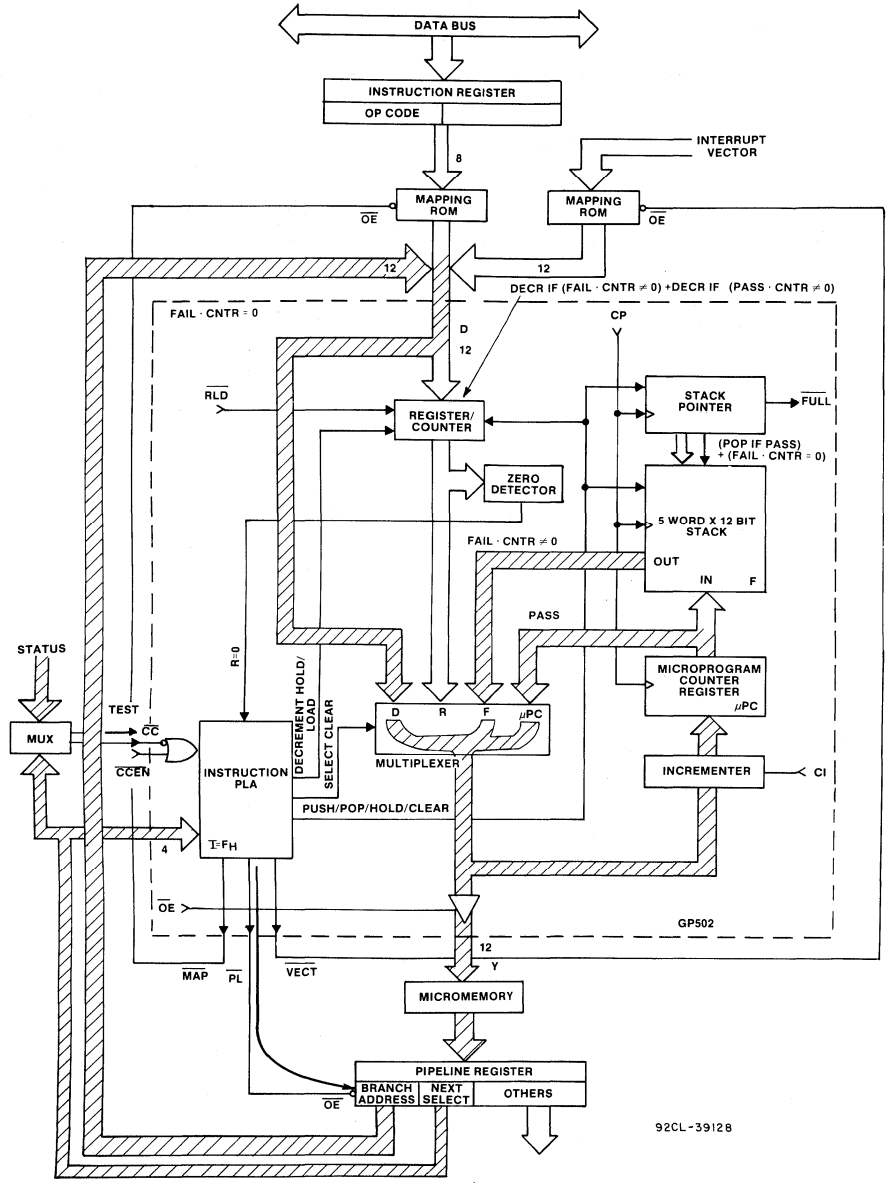


Fig. A-16 - Data flow diagram for the Three-Way Branch, TWB, instruction.

APPENDIX B
CODING TABLE

		NEXT ADDRESS								GP502	CC SEL			GP502 CONTROL INSTRUCTION				RT SEL	GP502		IR CLEN	MAR CLEN	DAO CLEN	DAI CLEN	C/CL	CC MUX EN	MEM W	MEM R	DAO OD	DAI OD
										CCEN	CCS2	CCS1	CCS0	I3	I2	I1	I0		RLD	FCL										
PIPELINE BITS		63	62	61	60	59	58	57	56	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27
	ADDR																													
INIT																														
CONTR 502 : 00→µPC	FF	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1
GPU 001 : 00→PC	00	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	1	1
FETCH																														
PC→MAR ; PC + 1→PC	01	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	1	1	0	1	0	0	0	0	0	0	1	1
MAR→BUS ; M(MAR)→IR	02	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	1	1	1	0	0	0	0	0	0	1	1	1
DECODE ; JMAP	03	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	1	1
LDI																														
PC→MAR ; PC + 1→PC	04	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	1	1	0	1	0	0	0	0	0	0	1	1
MAR→BUS ; M(MAR)→DAI	05	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	1	1	1
DAI→R1	06	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	0
ADD																														
R1 ← T2 + R1 ; STATUS→CC MUX	07	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0	1	0	0	1	1

		GP001 DEST CONTROL			MAR OD	DOE	G MS SLICE			P LS SLICE			U T ADDRESS				GP001 R ADDRESS				CARRY IN	DATA SEL			ALU FUNC		SOURCE SEL	
		M2	M1	M0			C2	C1	C0	C2	C1	C0	T3	T2	T1	T0	R3	R2	R1	R0	CI	D2	D1	D0	A1	A0	S1	S0
PIPELINE BITS		26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADDR																											
INIT																												
CONTR 502 : 00→µPC	FF	1	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPU 001 : 00→PC	00	1	0	1	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0
FETCH																												
PC→MAR ; PC + 1→PC	01	1	1	1	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
MAR→BUS ; M(MAR)→IR	02	1	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DECODE ; JMAP	03	1	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LDI																												
PC→MAR ; PC + 1→PC	04	1	1	1	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
MAR→BUS ; M(MAR)→DAI	05	1	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAI→R1	06	0	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
ADD																												
R1 ← T2 + R1 ; STATUS→CC MUX	07	1	0	1	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0

Power-Supply Distribution and Decoupling For QMOS High-Speed-Logic ICs

by R. Funk

The HC and HCT high-speed QMOS IC logic families available from RCA offer the user many advantages over TTL logic families. These advantages include much lower power consumption, better noise margin (mainly in the HC devices), wider operating-voltage range, wider operating-temperature range, lower input current, lower three-state current, superior high-to-low and low-to-high output transition time and propagation delay balance, and better reliability. However, HC/HCT CMOS does share one common liability with LSTTL: switching transients generated on the ground and supply rails can dangerously reduce logic noise margin if not compensated.

Higher speeds, faster edges, and higher output-drive currents cause higher-frequency current transients to be imposed on ground and V_{CC} rails of an IC. The familiar L di/dt voltage transient is developed, its value depending on the inductance in the ground or V_{CC} connection from chip to IC lead. For octal bus-driver types, one volt of L di/dt is possible depending on inductance, device decoupling, and power-supply decoupling. This Note focuses on power-supply distribution and decoupling to reduce switching noise. One source of this noise, an important system factor relative to IC switching, is rf radiated noise, noise that can interfere with communications in the local area. Some general ways to reduce L di/dt rf noise, i.e., voltage generation on ground and supply lines, are described below.

POWER DISTRIBUTION

Before decoupling can provide any noise reduction, there must first be a good power-distribution network. A good ground connection is vital, and so a good connection pattern is required.

The commonly accepted ground pattern shown in Fig. 1 can cause problems. In the figure, an output from device 1 drives an input to device 2, and an output from device 3 drives an input to device 4. Since the signal path 1 to 2 and 3 to 4 are not coupled, there should be no crosstalk. However, devices 1 and 3 share the crosshatched part of the ground line, as shown, and switching of the output of device 1 could produce a spike on the ground of device 3, causing the input to device 4 to switch. It is, therefore, advisable to reduce the single ground path on a double-sided board by using links, as shown in Fig. 2. This advice is especially true for boards

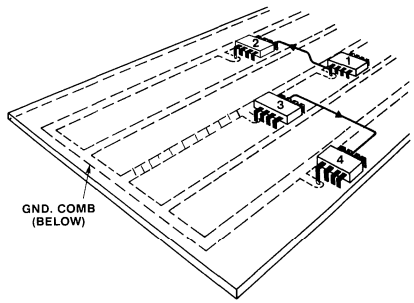


Fig. 1 - Common ground path on two-sided board.

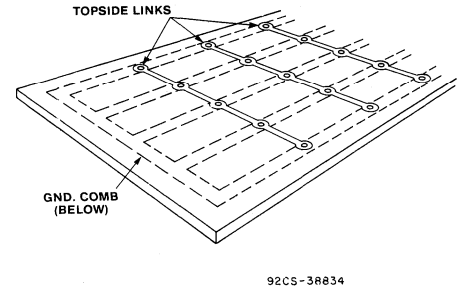


Fig. 2 - Reducing ground paths on two-sided board.

where high currents are switched. Avoid using jumpers like the one shown in Fig. 3 for ground and power line (V_{CC}) connections. Jumpers are unlikely to be used in production printed-circuit boards, but they should also be avoided on prototype and single boards because the inductance they introduce into the lines permits coupling between outputs. Printed-circuit boards equipped with premanufactured ground connections or copper strips to connect the pins to ground should be used.

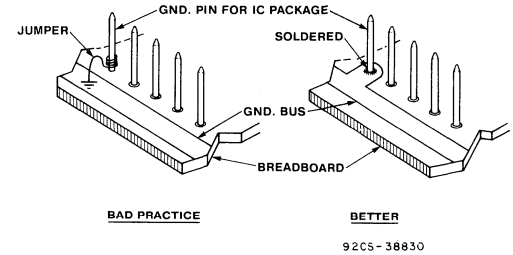


Fig. 3 - Ground connection on a logic board.

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An even better solution is to use multilayer printed-circuit boards, where different layers can be used for the supply rails and the copper interconnections. The capacitive coupling between ground and V_{CC} is essential for high-frequency noise-pulse reduction. The capacitive coupling has the distinct advantage of being free from the inductive effects of the interconnections and, therefore, acts like a discrete decoupling capacitor.

Even with double-sided boards, it is advisable to have the V_{CC} and ground lines on opposite sides of the board wherever possible. A less expensive alternative to multilayer boards is the multiwire board, which offers the same high-frequency noise characteristics.

No matter what type of board is used, it is recommended that it have at least five ground pins per connector to assure ground-current distribution. The precautions taken with ground lines also apply to the V_{CC} line. Power-line stability is a must, a difference of only 0.5 V between V_{CC} lines can produce unwanted effects. It is advisable to provide separate power stabilization for each board to isolate noise sources and to eliminate large stabilizer circuits with their heavy-gauge (low-impedance) wiring to each board. However, care must be taken in designing power stabilization because a fault on a board's stabilizer circuit may be transmitted via the HC/HCT input structure to other boards, possibly causing damage.

DECOUPLING

No matter how good the V_{CC} and ground connections, all line-inductance effects cannot be avoided. This is where decoupling plays its part. Ceramic capacitors are the nearest approximation to ideal decoupling capacitors since they have almost no series inductance. But the advantage of using inductance-free capacitors is lost if long connections to the capacitor are used. These over-long connections can result in a tuned LC-circuit with a very high Q factor. The oscillations produced would have a worse effect on the circuit than if there were no decoupling at all. If it is not possible to make the decoupling connections shorter than 20 mm, place tracks in parallel, with a separation of at least one track width, as shown in Fig. 4. Making the connections thicker will have almost no effect.

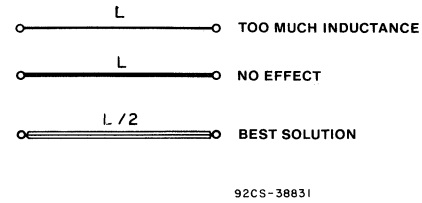


Fig. 4 - Comparison of decoupling tracks.

The capacitors to be used should be carefully selected. Many capacitors are produced with leads bent, as shown in Fig. 5(a); these may introduce unwanted inductance. The best capacitors are those with leads shaped as in Fig. 5(b).

In tests, good decoupling was obtained by using a minimum of:

- one 47 μF bulk capacitor per standard IC card
- one 1 μF tantalum capacitor per 10 packages of SSI logic
- one 22 nF ceramic capacitor for each octal bus-driver circuit and for each counter/shift register (MSI logic)
- one 22 nF ceramic capacitor per four packages of SSI logic

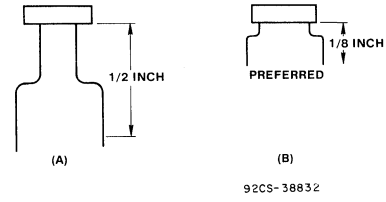


Fig. 5 - Optimum capacitor lead shape.

Replacing LSTTL with QMOS High-Speed Logic ICs

by J. Nadolski

Until the development of RCA HC and HCT high-speed-CMOS logic ICs, high-speed logic devices were available only in the high-power-consuming bipolar technology. The HC/HCT QMOS family features LSTTL speed along with many performance features superior to LSTTL. HCT CMOS ICs have TTL-compatible input-voltage levels and are intended to be CMOS substitutes for bipolar LSTTL logic ICs of the same type. HC CMOS ICs have CMOS voltage-level input compatibility and feature high noise immunity in all-CMOS system designs.

Replacement of an LSTTL IC with an HCT IC provides the identical logic function, same pin out, same speed, and same general-purpose logic fanout of 10 LSTTL loads, but with much less power dissipation. LSTTL bus-driver types can drive 100-ohm transmission-line terminations, but at a huge sacrifice in system power consumption. Techniques that can be used to terminate 100-ohm lines, and other types of low-power terminations involving LSTTL and QMOS ICs, are presented in this Note.

PERFORMANCE COMPARISON

Of paramount importance in the comparison of LSTTL and QMOS (HCT) performance are the identical input-voltage specifications of the two technologies:

V_{IL}(max) = 0.8 V
V_{IH}(min) = 2 V

Table I is a comparison of all applications-related parameters. It is evident from this table that not only does HCT QMOS substitute easily for LSTTL, but system performance is enhanced through such characteristics as better signal transition time and propagation delay balance, better noise margin, and lower supply and signal-line currents. The comparisons below follow the organization of Table I.

Power Consumption-(dc)—HCT power consumption is essentially zero in comparison to LSTTL. **ac (operating)**—HCT power is frequency dependent and comparable to LSTTL at continuously high operating frequencies. Generally, HCT power is much lower because average logic data rates are under 1 MHz.[1]

Voltage—HC/HCT CMOS requires much less voltage regulation than LSTTL. HCT devices can actually operate at 2 to 6 volts, although they are specified for 4.5 to 5.5 volts.

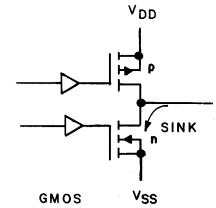
Temperature—Commercial-grade HC/HCT CMOS is more realistically rated than LSTTL, -40° C to +85° C, not the very limiting 0 to +70° C of most LSTTL 74 families.

Noise Margin—HCT interfacing with HCT or with LSTTL provides improved noise margin, particularly at the high end of the operating range where outputs swing to 5 volts.

Stability—The CMOS input PMOS/NMOS pair has less switching-voltage shift with temperature variation than LSTTL, an inherent circuit advantage compared to the LSTTL diode input design with its temperature sensitivity. This HCT advantage provides better noise margin over the device operating-temperature range and better stability of RC astable multivibrators with temperature variation when these circuits employ HCT ICs.

Output Drive Current—HC/HCT CMOS has better source current than LSTTL and sufficient sink current for LSTTL interfacing requirements. Sink current is lower than in LSTTL; this characteristic minimizes current spiking and EMI generation in RCA QMOS devices. This Note will delve into line terminations relative to sink current, the one area where differences in equipment design may exist depending on the high-speed logic family used.

Timing—The HC/HCT output-stage PMOS/NMOS transistors are designed for balance at saturation in order to provide balanced output transition times. All logic stages employ PMOS/NMOS transistor sizing, Fig. 1, to balance propagation delays, Fig. 2.



SINK AND SOURCE = 4 mA (STANDARD) IO LSTTL LOADS
CURRENT = 6 mA (BUS) I5 LSTTL LOADS

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Fig. 1 - Logic stage PMOS and NMOS transistor sizing to balance propagation delays.

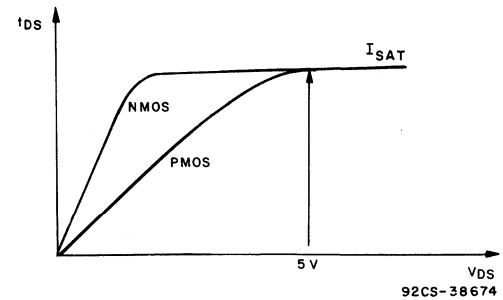

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Fig. 2 - Balanced output transition time and propagation delay.

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Table I - Comparison of Characteristics of HCT and LSTTL Circuits

Characteristic	QMOS CD74HCTXXXX			74LSTTLXXXX	
Quiescent Power					
Per Gate	0.025 mW			5.5 mW	
Per Flip-Flop	0.05 mW			10 mW	
4-Stage Counter	0.4 mW			95 mW	
Per Transceiver/Buffer	0.1 mW			60 mW	
Operating Power	Frequency In			Frequency In	
	0.1 MHz	1 MHz	10 MHz	0.1-1 MHz	10 MHz
Per Gate	0.2 mW	2 mW	20 mW	5.5 mW	≅20 mW
Per Flip-Flop	0.15 mW	1.5 mW	15 mW	10 mW	≅15 mW
4-Stage Counter	0.24 mW	2.4 mW	24 mW	95 mW	≅120 mW
Per Transceiver/Buffer	0.25 mW	2.5 mW	25 mW	60 mW	≅90 mW
Operating Supply Voltage	(HCT) 4.5 V to 5.5 V (HC) 2 V to 6 V			4.75 V to 5.25 V	
Operating Temperature Range	-40°C to +85°C			0°C to +70°C	
Noise Margin					
LS to LS	—			0.7 V/0.4 V	
HC to HC (High/Low)	1.4 V/0.9 V			—	
HCT to HCT	2.9 V/0.47 V			—	
Input Switching Voltage Stability over Temp.	$V_S \pm 60$ mV			$V_S \pm 200$ mV	
Output Drive Current					
Source Current at V_{OH}=2.4 V	-8 mA			-400 μA	
Sink Current					
Std. Logic V_{OL}=0.4 V	4 mA			4 mA	
Bus Logic V_{OL}=0.4 V	6 mA			12 mA	
V_{OL}=0.5 V	12 mA			24 mA	
Output Transition Time*					
T_{TLH}	6 ns			15 ns	
T_{THL}	6 ns			6 ns	
Typical Gate Propagation Delay:*					
t_{PHL}/t_{PLH}	8 ns/8 ns			8 ns/11 ns	
V_{CC}=5 V, C_L=15 pF					
Typical Flip-Flop Propagation Delay:					
V_{CC}=5 V, C_L=15 pF					
t_{PLH}	14 ns			15 ns	
t_{PHL}	14 ns			22 ns	
Typical Clock Rate of a Flip-Flop	50 MHz			33 MHz	
Input Current					
I_{IL}	-1 μA			-0.4 to -0.8 mA	
I_{IH}	1 μA			40 μA	
3-State Output Leakage Current	±5 μA			±20 μA	
Reliability					
%/1000 Hours at 60% Confidence	0.0019 (RCA Report)			0.008 (RADC Report)	

*Temperature Coefficient = 0.04 ns/pF for both QMOS and LSTTL.

Frequency—QMOS clock rates are often higher than LSTTL clock rates.

Input Current—A big difference between the two technologies is the relatively large continuous dc current that flows in LSTTL interconnect wiring. Essentially no dc input current flows in HC/HCT CMOS. Typically, a few picoamperes of input back-diode current flows. This HCT advantage means better buffering and a wider frequency range in RC oscillators.

Leakage Current—Bus designs are enhanced by a four-times-lower high-Z output leakage current in HC/HCT CMOS as compared to LSTTL. For low-power designs, larger values of terminating resistors can be used.

Reliability—Reliability at 85°C junction temperature is four times improved with HC/HCT CMOS ICs. In fact, since the higher internal IC dissipation of LSTTL raises junction temperature an average of 10°C per IC, reliability improvement is even greater than the four-times improvement indicated.

INPUT/BUS/TRANSMISSION-LINE TERMINATION

Termination at inputs and outputs may be different for HCT and LSTTL devices. It is good design practice to properly terminate all unused LSTTL inputs. HCT devices can then be substituted directly, provided the unused input is returned to V_{CC}, ground or through a 1.2 kilohm or higher pull-up resistor. Output terminations are handled differently.

A discussion of termination follows. It is primarily in I/O terminations that differences in circuit design could exist and, hence, require design changes when HCT is substituted for LSTTL.

INPUT TERMINATION

The termination of unused inputs in LSTTL is not absolutely necessary because of the internal pull-up of 1.2 kilohms; however, it is good design practice to terminate all unused inputs to prevent linear operation of input circuitry. Such operation causes the circuitry to draw more power than it would under normal operation. The typical resistor values used for pull-up in termination of LSTTL are between 220 ohms and 1.2 kilohms; typical pull-down values are between 680 ohms and 1 kilohm. Unlike the case with LSTTL devices, unused HCT inputs must be terminated since the input is a very high impedance and, if left open, could cause the input circuitry to float into a linear mode of operation, thus drawing excessive current or causing oscillation. HCT devices **must** be terminated to V_{CC} or ground or with a pull-up or pull-down resistor with a value of 1 kilohm to 1 megohm, as shown in Fig. 3. The large-value resistors reduce the power dissipation of the driving devices.

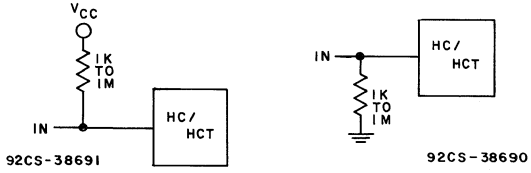

Fig. 3 - Methods of terminating HCT devices: (a) pull-up, (b) pull-down.

If an HCT device is to be used in a plug-in card system, all of the inputs from the card to the system **must** be terminated with pull-up resistance of a minimum value of 10 kilohms. In equipment designs using HC or HCT CMOS devices, where the inputs may be terminated to V_{CC}, there is an inherent current when V_{CC} is momentarily at ground.

One of the major uses of LSTTL is in computer and microprocessor-based systems. Parts such as bus drivers, transceivers, octal latches, and line drivers are widely used. All of these parts have three-state outputs. Three-state outputs allow a large number of circuits to connect to the same data bus by creating an open circuit on the device's output when it is not being accessed or utilized. The buses are usually terminated by a pull-up or a pull-down resistor. This resistance is necessary to prevent noise from being picked up on the bus. For LSTTL, the value of the pull-up resistor ranges from 330 ohms to a maximum of 100 kilohms. The choice of a pull-up or pull-down resistor will depend on whether a high or low state is required on the bus during the high-impedance state.

Termination resistors are usually placed at the most distant point from the bus-driving device. Multiple termination can be used, but these terminations must be individually high enough in resistance value so that the parallel resistive load on the bus driver is not too low; this load should be approximately 100 ohms minimum theveninized R for LSTTL bus drivers.

The typical values of pull-up for HCT bus drivers range from a minimum of 750 ohms to a maximum of 1 megohm. The choice of the resistor value involves a tradeoff between power and bus speed. A larger value of resistance will save power but will slow down the bus; a smaller value of resistance will speed up the bus, but will waste power. Typical values of pull-down resistance range from 680 ohms to 1 kilohm. A bus termination is a **must** for HC/HCT devices if the bus is to be in the high-impedance state for more than 100 microseconds. However, it is usually a good idea to terminate the three-state bus in case the system stops momentarily in the high-Z state or there is noise due to crosstalk in the system.

In any bus-driving configuration, all ICs must be by-passed with ceramic by-pass capacitors of at least 0.01 microfarad, as shown in Fig. 4. The capacitor is placed as close as

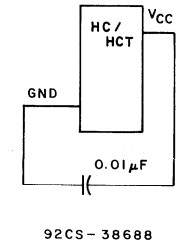

Fig. 4 - IC by-passing arrangement in a bus-driving configuration.

possible to the ground pin to minimize inductance and, hence, ringing in the ground of the IC. Where HC/HCT is driving a terminated line and some slight ringing into ground exists, and this ringing or noise is above or near the input switching voltage of 1.3 volts, the receiving IC should be an HC CMOS type, which has an input switching point of approximately 2.3 volts (1 volt more than LSTTL or HCT).

In some critical applications where almost no noise can be tolerated, the board or card can be bypassed with a 10-ohm or lower value resistor of the proper power rating in series with the supply line, and a 33 microfarad or larger capacitor across the supply, as shown in Fig. 5. This RC combination is placed at the point where the power supply comes into the board or card.

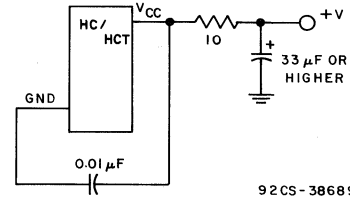

Fig. 5 - By-passing the board or card in a critical operation where almost no noise can be tolerated.

DRIVING TRANSMISSION LINES

Another type of termination required is that for transmission lines. This type of termination is used where data must travel over long distances in a system, in a large backplane, over coaxial cable, or in twisted-pair lines. This termination creates a low impedance that prevents noise and crosstalk from generating false data. Typical LSTTL systems use

nominal 100-ohm twisted-pair, strip-line, or coaxial transmission-line impedances. This low impedance is necessary to the transmission of signals at high speeds without data degradation due to line capacitance or inductance. Fig. 6 shows a common LSTTL type of transmission-line termination. In order to drive this 120-ohm load, the LSTTL output sink current is required to be at least 24 milliamperes at a V_{OL} of 0.5 volt.

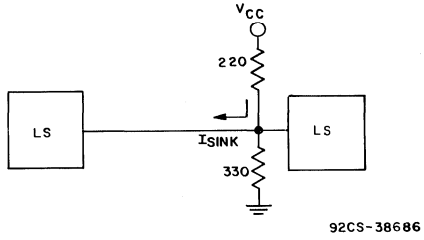

Fig. 6 - Common LSTTL transmission-line termination.

There are two powerful arguments for not duplicating this same 24 mA/0.5 V output specification in a well-designed HC or HCT bus-driver output stage:

1. 0.25 watt per output, 2 watts per octal driver, is high-power design, not moderate or low-power equipment design.
2. A CMOS output sink current of 24 milliamperes at 0.5 volt will give rise to an objectionably high transient current when switching, and will produce EMI which is objectionably large, much larger than the LSTTL output with the same current/voltage level. Fig. 7 shows the much higher I_{sat} in an NMOS output sink transistor versus an n-p-n output sink transistor. I_{sat} is twice as large, as are dv/dt and EMI, in CMOS as in LSTTL devices.

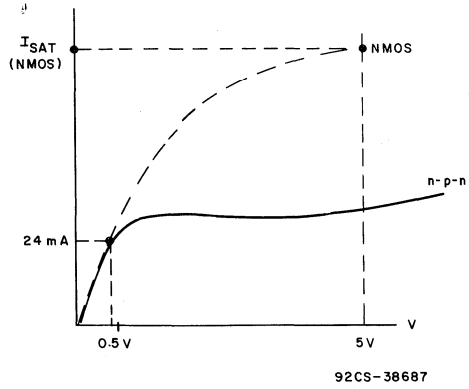

Fig. 7 - Comparison of I_{sat} in an n-p-n transistor and an NMOS transistor.

The RCA QMOS-device output stage is designed to provide typically more than 12 milliamperes at 0.5 volt. The QMOS I_{sat} is, then, similar to the LSTTL I_{sat}. The all-important noise-generation factor (EMI) is also similar at this current/voltage level.

The lowest impedance that an HCT/HC device can drive in the ac/dc termination described above is approximately 700 ohms, as shown in Fig. 8. This impedance is created with a

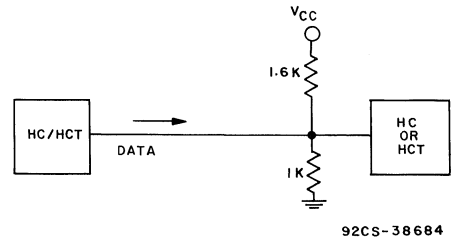

Fig. 8 - Lowest-impedance arrangement in transmission-line termination.

1.6 kilohm pull-up and 1 kilohm pull-down resistor, a combination that retains the 1/3 pull-down to 2/3 pull-up terminating-resistance design criteria. The terminators should be placed as close as possible to the receiving circuit. Higher values of transmission-line impedance can be used to save power, but the advisability of this choice will be determined by the speed of the data on the transmission line and the distance the data must travel.

More than one termination of the type described can be used on the same line if required because of long line length or a very noisy environment; but the designer must remember that the worst-case sinking limit is still 12 milliamperes at 0.5 volt, and should treat these terminating impedances as being in parallel and limited to 700 ohms, as shown in Fig. 9.

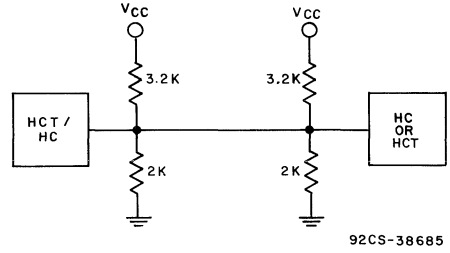

Fig. 9 - Multiple terminations on the same transmission line.

The above termination is useful for both dc and ac transmission-line terminations. With HC/HCT devices, a dc termination is not necessary, but an ac termination is a must. If the designer must have a transmission-line termination in an HC/HCT system, or must intermix families, then a variation on the voltage-divider termination can be used, as shown in Fig. 10.

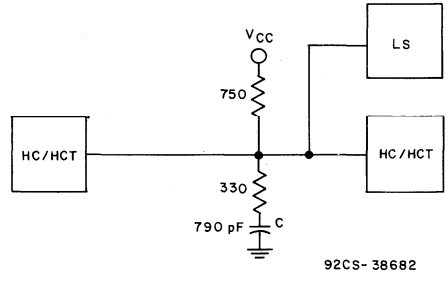

Fig. 10 - Transmission-line termination in HCT system or when families are intermixed.

Capacitor C is used to create a low impedance during switching. HC/HCT outputs can deliver up to 70 milliamperes during switching on bus types and up to 50 milliamperes on standard types. The value of C depends on the maximum frequency, f, of the bus. This value can be determined by the formula:

$$C = \frac{(\frac{1}{2}f_{min})}{Xc} \quad (1)$$

$$\frac{1}{(2\pi f_{min})}$$

where Xc is approximately 50 ohms.

A typical value for C when f_{max} is 4 MHz or greater is 790 picofarads. When there is no switching, the only dc current present comes from the pull-up resistor. This configuration not only saves power but allows HC/HCT to drive a modified low-impedance transmission line. The configuration in Fig. 11 pulls the bus into the high state when it is in the high-impedance mode. If a low state is required on the

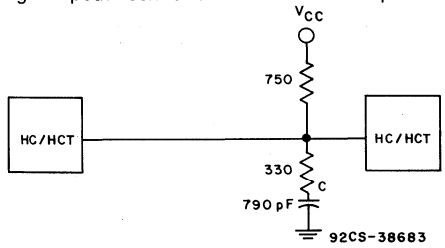

Fig. 11 - Configuration used to pull the bus into the high state when it is in the high-impedance mode.

bus, the configuration in Fig. 12 can be used. If more than one of these terminations are required on the same line, the designer must treat the terminations as being in parallel, and should adjust the values of R and C to comply with the maximum dc sink current of 12 milliamperes at 0.5 volt, as shown in Fig. 13.

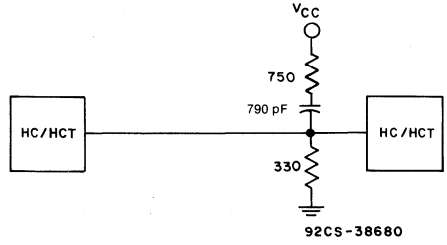

Fig. 12 - Configuration used to pull the bus into the low state when it is in the high-impedance mode.

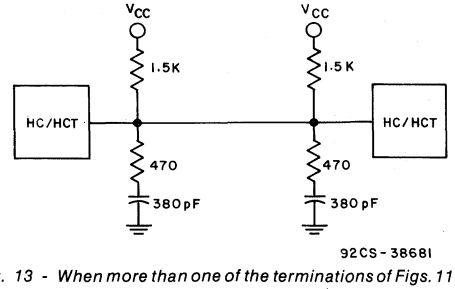

Fig. 13 - When more than one of the terminations of Figs. 11 and 12 are needed, the terminations are adjusted and treated as if they are in parallel.

DRIVING COAXIAL CABLE

LSTTL ICs can drive transmission lines using coaxial cable. Various types of coaxial and triaxial cable are available, but the most commonly used is the 75-ohm RG-59/59U, which has an impedance of 75 ohms at its nominal operating frequency. LSTTL bus drivers can directly drive almost all of the popular terminations used with coaxial-cable drive. One of the most commonly used is shown in Fig. 14. An

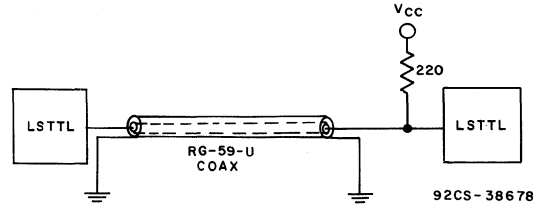

Fig. 14 - A commonly used LSTTL coaxial-cable termination.

HC/HCT device cannot drive any of these terminations without exceeding its maximum sink current. However, HC/HCT devices can drive coaxial cable by using the modified transmission-line termination shown in Fig. 15 or a modified resistor terminator, as shown in Fig. 16. The coaxial cable should be terminated at both ends in cable runs over 50 feet, again keeping in mind the maximum limits of HC/HCT sink current. Equation 1 can be used, with the addition of the figure for the capacitance of the coaxial cable, per foot, to calculate the correct value of capacitance C in Fig. 17.

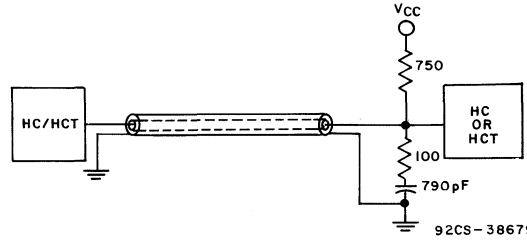

Fig. 15 - Modified transmission-line termination used with HCT devices driving coaxial lines.

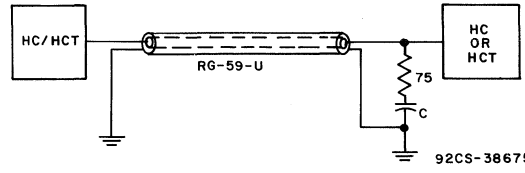

Fig. 16 - Modified resistor termination used with HCT devices to drive coaxial lines.

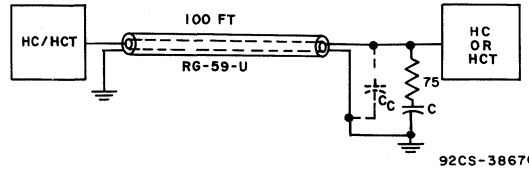

Fig. 17 - Effect of cable capacitance on termination.

ICAN-7330

By using a modified transmission-line termination for HC/HCT devices, and depending on the maximum frequency to be driven, coaxial cables of various lengths can be CMOS driven. A typical example is shown in Fig. 18, where an HC/HCT device drives more than 50 feet of RG-59U coaxial cable with a modified termination of 75 ohms. A series capacitor in the resistor leg that goes to $+V_{CC}$ is placed at the receiver end of the cable to eliminate degradation which could cause false data to be received.

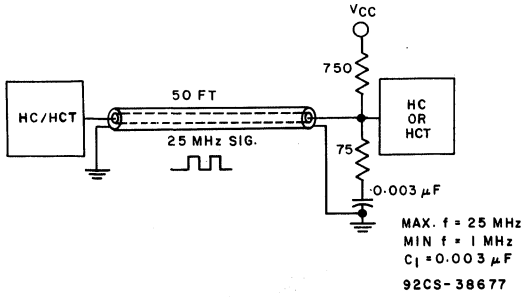

Fig. 18 - Termination configuration used to eliminate possibility of false data at receiver.

DRIVING RIBBON CABLE

When using HC/HCT ICs to drive signals over ribbon cable, there are length limitations resulting from the high impedance of the CMOS input. The drive limit is two feet maximum at normal data rates when driving without any termination and without the use of an alternate ground scheme (alternating signal carrying and grounded wires, as shown in Fig. 19) in the ribbon cable. Beyond two feet, crosstalk between signal lines can cause errors in data. If the receiving IC is an HC type, the maximum drive lengths can double.

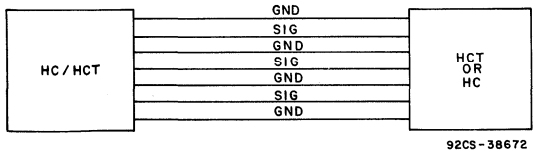

Fig. 19 - Alternate ground arrangement of ribbon cable.

When driving with no termination but with the alternate ground method, the maximum drive length before crosstalk between signal lines can cause errors in data is six feet at normal data rates.

HC/HCT devices can drive longer ribbon cable by using various terminations: pull-up, pull-down, or one of the modified transmission-line terminations. When using a 1-kilohm pull-up resistor per wire as a termination, the maximum length without alternate ground before crosstalk can become a problem is four feet at normal data rates. When using the same setup with an alternate ground scheme, as shown in Fig. 20, the maximum length of drive is seven feet at normal data rates. The maximum drive limit is six feet, as shown in Fig. 21, when a modified transmission-line termination with an impedance of approximately 100 ohms and no alternate ground scheme is used at normal data rates. More than 15 feet can be driven at a data rate of 10 MHz when the alternate ground scheme is employed along with the termination of Fig. 21. The length can be extended by using any of the above terminations at both the receiving and transmitting ends of the cable.

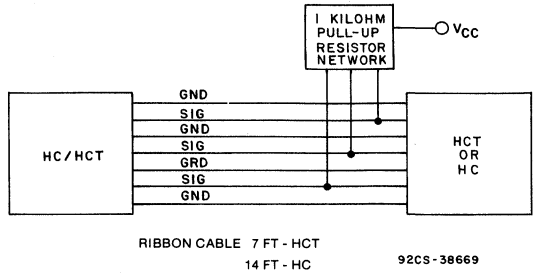

Fig. 20 - Ribbon-cable termination using 1-kilohm pull-up resistor and alternate ground arrangement.

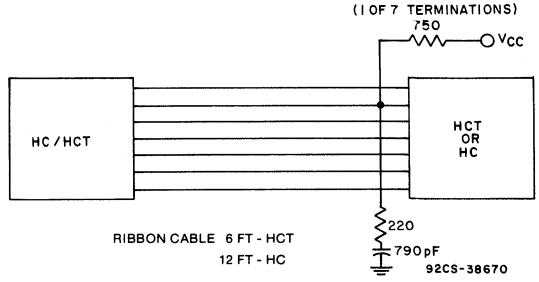

Fig. 21 - HCT ribbon-cable termination for normal data rates using impedance of approximately 100 ohms and no alternate ground system.

There are many other types of transmission-line terminations, but those shown above are the most commonly used with HCT/HC devices. When contemplating terminations of any sort, the designer must remember that HCT/HC devices have a current-sinking limit at 0.4 volt of 6 milliamperes, and at 0.5 volt of 12 milliamperes. These limits **must** be observed. By following the termination criteria described above, system power consumption is reduced, reliability is greatly improved, and system cost is decreased.

REFERENCES

1. For a full discussion of HC/HCT power consumption and how to calculate it, see RCA Solid State Publication ICAN-7315, "Power Consumption in QMOS Logic Circuits," by R. Funk.

Abstracts of Other Application Notes

ICAN-6315 ..... 8 pages
COS/MOS Interfacing Simplified

COS/MOS with its wide range of operating supply voltages, low input current, and low power consumption, interfaces easily with many electronic devices. In addition, COS/MOS circuitry can easily be added to a system and can often be operated from the existing power supply. Examples of practical circuits for a wide variety of interfacing situations are given in this Note; design constraints are included in each case.

ICAN-6558 ..... 8 pages
Understanding Buffered and Unbuffered CMOS Characteristics

Both buffered and unbuffered CMOS B-series gates, inverters, and high-current IC products are available from RCA; each product classification has application advantages in appropriate logic-system designs. Recently, many CMOS suppliers have been concentrating on promoting buffered B-series products with applications literature focusing on the attributes and use of the buffered types. This practice has left an imbalance in the understanding and application of **both** buffered **and** unbuffered gates and, in many instances, customers are not using unbuffered products when they are the best for the intended application. This Note narrows the misunderstandings involved in this issue by presenting and discussing the relative merits of the buffered and unbuffered CMOS devices.

ICAN-6563 ..... 4 pages
Radiation Resistance of the COS/MOS CD4000A and CD4000B Series

Complementary MOS (COS/MOS) integrated circuits possess many advantages which recommend their use in radiation-susceptible space and military environments. Several of the most significant of these advantages are: ultra-low standby-power consumption, high noise immunity, extremely high packaging density, and inherently high reliability. This Note discusses two additional advantages—permanent-radiation resistance and transient-radiation resistance.

ICAN-6572 ..... 4 pages
COS/MOS Electrostatic-Discharge Protection Networks

RCA's two families of CMOS devices, the standard A series (3 to 15 volts) and the high-voltage B series (3 to 20 volts), are equipped with networks to protect the gate oxide of the devices against damage resulting from discharge of electrostatic energy between any two pins. This Note evaluates and characterizes the various protection networks incorporated in all CMOS product.

ICAN-6576 ..... 6 pages
Power-Supply Considerations for COS/MOS Devices

RCA COS/MOS Digital Integrated Circuits operate at extremely low power dissipation levels. They function reliably with high noise immunity over a wide operating-voltage range. The RCA COS/MOS product line includes a standard line designed to operate with voltage supplies from 5 to 15 volts and a low voltage "A" series line designed to operate from 3 to 15 volts. These properties enable system designers to operate RCA COS/MOS devices from unregulated, poorly-filtered supplies, or from a wide variety of single- or multiple-cell battery sources. This Note describes the salient features of COS/MOS devices which permit operation from such a wide range of power sources and provides the system designer with the necessary information to permit him to design the most economical power source for his COS/MOS system. This Note is applicable to both COS/MOS product lines mentioned above.

ICAN-6587 ..... 16 pages
Noise Immunity of COS/MOS B-Series Integrated Circuits

The excellent noise-immunity characteristics of COS/MOS (complementary-symmetry/metal-oxide-semiconductor) digital ICs is a paramount reason for their preferred and successful use in high-noise automotive, process-control, production-monitoring, and similar harsh-noise-prone applications. The introduction of the RCA B-series COS/MOS devices furthers the well-known noise immunity advantages of the COS/MOS technology. Included in this Note are brief discussions of logic-system noise and rejection concepts, COS/MOS dc/ac noise-immunity specifications and definitions, and dc/ac noise-immunity performance data for several B-series COS/MOS gates, inverters, and high-current drivers.

ICAN-7323 ..... 4 pages
Modification of LSTTL Test Programs to Test HCT High-Speed-CMOS Logic ICs

The QMOS HCT family of high-speed logic ICs is designed and specified not only to replace LSTTL devices having the same type numbers, but to interface with all TTL, CD4000B CMOS, and QMOS HC logic families. As such, it is indeed one of the more, and perhaps the most, interface-flexible logic family. In existing and new-equipment designs where LSTTL devices are, or could be, used, these devices are easily replaced by RCA's HCT logic family because of the several advantages its QMOS technology has over LSTTL. But the switch from LSTTL to QMOS has made it necessary for test personnel to switch from the testing of LSTTL functions to the testing of the identical HCT functions; this Note has been written to make that switch as easy as possible. The widely used Teradyne J283 test system is used as a basic frame of reference in this Note; however, the test information given is applicable to most other test equipment and bench-test situations.

Abstracts of Other Application Notes

ICAN-7325 ..... 8 pages
Interfacing HC/HCT QMOS Logic with Other Families and Various Types of Loads

This Application Note describes the interface capability of the new high-speed CMOS CD54/74HC/HCT logic families, probably the most interface-capable families yet devised. The low dc power consumption and high speed of the HC/HCT families are both prime qualities for interfacing flexibility. Several characteristics, along with HC/HCT-family static and dynamic noise immunity, are discussed in this Note. The Note describes in detail HC/HCT interfaces with LSTTL, CMOS CD4000B-series, NMOS, and ECL devices, and interfaces with terminated buses, displays, and relay or stepping-motor coils, including interfaces with nonstandard output levels.

ICAN-7337 ..... 6 pages
Astable Multivibrator Design Using High-Speed QMOS ICs

This Note describes the design of astable multivibrators using RCA high-speed-CMOS (QMOS) integrated circuits (CD54/74 HC, HCU, HCT04 and 132), and multivibrator performance at frequencies up to 10 MHz. Algebraic equations permit the values of R and C for a given oscillator frequency to be quickly determined. The effect of supply voltage and temperature variation on multivibrator performance is discussed along with the inherently low power consumption of QMOS relative to LSTTL. In addition to much lower power dissipation than other technologies, a distinct advantage of QMOS RC multivibrator design is the choice of a very wide range of R_xC_x, which leads to an exceptional frequency range.

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KANSAS

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Overland Park, KS 66212
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Lyons Corporation
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MANITOBA

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RCA Solid State

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